DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC T42 ELECTRONIC CIRCUIT & ANALYSIS NOTES

II YEAR/ IV SEM

<center>**UNIT– I**</center>

Transistor Low Frequency Analysis: Definition of h–parameters – Small signal low frequency h-parameter model –Mid band analysis of CB, CE and CC amplifier to obtain gain, input impedance and output impedance – Analysis of CE amplifier with an emitter resistance – Low frequency FET model – CS, CD and CG amplifiers.

Transistor High Frequency Analysis: Hybrid pi CE transistor model – Hybrid pi conductances and capacitances – CE short circuit current gain using Hybrid pi model - Current gain with resistive load.

HYBRID PARAMETRS

The hybrid parameters are generally used to determine amplifier characteristic parameters such as voltage gain, input and output resistance etc. we have already know that amplifier characteristic parameters may be determined by using current gain(β) and values of other circuit components. Hybrid methods had the following advantages:

1. Value of circuit components are easily available, and
2. The procedure followed is quite simple and easy to understand.

H-PARAMETERS OF LINEAR CIRCUIT

Every linear circuit having input and output can be analyzed a s two port networks. In these networks there are four parameters called hybrid or h-parameters. Out of these four parameters, one is measured in ohm, one in mho and other two are dimension less. Since these parameters hae mixed dimension, so they are called hybrid parameters.

Consider a linear circuit shown in Figure (a). in this circuit when input voltage 1 is applied, input current i_1 flows. Then output voltage V_2 and current i_2 appears. Both currents i_1 and i_2 are assumed to flow inside the box of the linear circuit. Both voltages V_1 and V_2 are assumed to be positive from the upper to lower terminals.
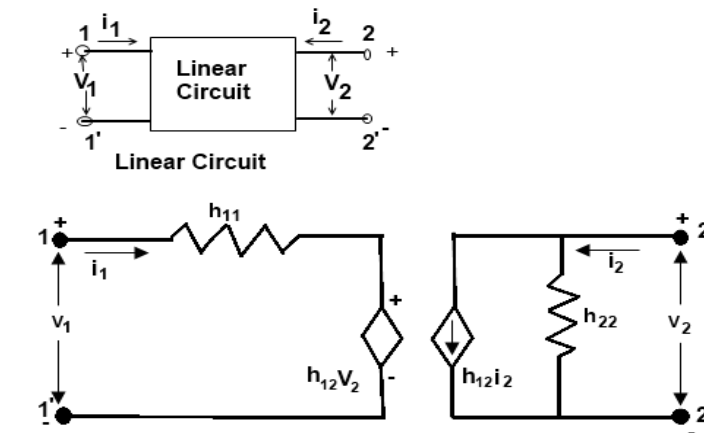

Figure (a) **Hybrid model for a Linear Circuit**

The linear circuit may be replaced by an equivalent circuit as shown in Figure (a). the equivalent circuit is called hybrid model of a linear circuit. In such as circuit, the input and the output voltages and currents (called variables) may be related by the set of the following two equations:

$$V_1 = h_{11}.i_1 + h_{12}.V_2$$
$$I_2 = h_{21}.i + h_{22}.V_2$$

Where,

V_1 = input voltage
V_2 = Output voltage
I_1 = input current
I_2 = output current

And h_{11}, h_{12}, h_{21} and h_{22} are hybrid parameters.

DETERMINATION OF H-PARAMETERS

The parameters h_{11} and h_{21} may be determined by short circuiting the output terminals of a given circuit. On the other hand, h_{12} and h_{22} may be determined by open circuiting the input terminals of the given circuit.
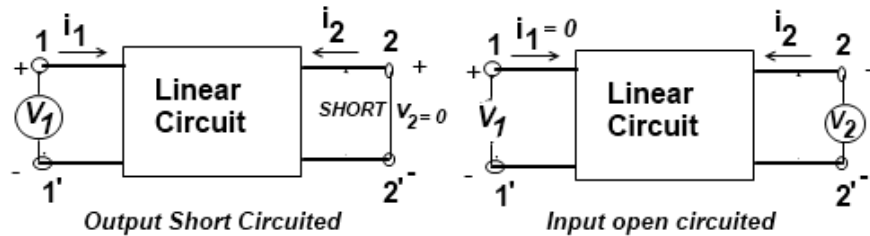

Output Short Circuited   Input open circuited

Figure (b)

Determination of h_{11} and h_{21}

These are determined by short circuiting the output terminals of a given circuit as shown in Figure (b). a shot circuit at the output terminal makes the voltage v2 equal to zero. Input voltage is given by relation,

$$VI = h_{11}.i_1 + h_{12}.V_2$$

Putting the value of V_2 (equal to zero) in the above equation, the input volage,

$$V_1 = h_{11}.i_1 \text{ or } h_{11}=V_1/i_1$$

Thus h_{11} may be determined from the ratio V_1/i_1. The value of i_1 can be obtained by applying a voltage at the input and then measuring the value of input current (i_1). Since h_{11} is the ratio of voltage to current, therefore it has the units of ohms i.e. the same unit as that of a resistance.

Because of this fact, h_{11} is called input resistance of the circuit with output short circuited. Similarlly , output current is given by the relation.

$$I_2 = h_{21}.i_1 + h_{22}.V_2$$

Again putting the value of V_2 the output current,

$$I_2 = h_{21}.i1 \text{ or } h_{21} = i_2/i_1$$

Thus h_{21} may be determined from the ratio i_2/i_1, the values of i_2 and i_1 may be obtained by applying a voltage at the input and then measuring the input current (i_1) and output current (i_2). Since h_{21} is the ratio of currents, therefore it has no units. The parameter h_{21} is called the forward current gain of the circuit with output short circuited.

Determination of h_{12} and h_{22}

These are determined by open circuiting the input terminals of the given circuit as shown in Figure (b). an open circuit at the input terminals, makes the current (i_1) equal to zero. We also know that the input voltage is given by the relation.

$$V_1 = h_{11}.i_1 + h_{12}.V_2$$

Putting the value of i_1 in this equation, the output voltage will be

$$V_1 = h_{12}.V_2 \text{ or } h_{12} = V_1/V_2$$

Thus h_{12} may be determined from the ratio V_1/V_2. The value of V_1 may be obtained by applying a voltage (V_2) and the measuring the input voltage (V_1). Since, h_{12} is a ratio of voltages, therefore it has no units. As h_{12} is the ratio of input voltage (V_1) to the output voltage (V_2), therefore, its value known as the reverse voltage gain.

Similarly, the output current is given by the relation.

$$I_2 = h_{21}.i_1 + h_{22}.V_2$$

Again putting the value of i_1 (equal to zero) in this equation. The output currents will be,

$$I_2 = h_{22}.V_2 \text{ or } h_{22} = i_2/V_2$$

$h_i = h_{11} =$ Input resistance with output shorted,
$h_r = h_{12} =$ Reverse voltage gain with input open,
$h_f = h_{21} =$ Forward current gain with output shorted,
$h_o = h_{22} =$ Output conductance with input open.

The h-parameters of a transistor depend upon the type of the configuration used i.e. common emitter (CE), common collector (CC) or common base (CB). Because of this, each of the four h-

parameters carries a second subscript letter e, b or c. the letter 'e' is used to represent common emitter; 'c' for common collector and 'b' for common base configuration.

| S.No	General parameter	Transistor configuration		
		Common emitter	Common base	Common collector
1	h_{11}	h_{ie}	h_{ib}	h_{ie}
2	h_{12}	h_{re}	h_{rb}	h_{re}
3	h_{21}	h_{ic}	h_{fb}	h_{fe}
4	h_{22}	h_{oe}	h_{ob}	h_{oe}

HYBRID EQUIVALENT FOR COMMON EMITTER TRANSISTOR

The figure shows the transistor connected in common emitter configuration and the figure also shows the hybrid equivalent circuit of such a transistor.

In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and emitter terminals. The input voltage (V_{be}) and the output current (i_c) are given by the following equations:

$$V_{be} = h_{ie}.i_b + h_{re}.V_c$$

$$i_e = h_{fe}.i_b + h_{oe}.V_c$$
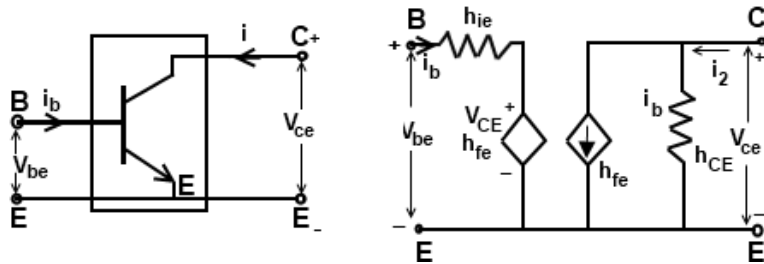
Current Gain

It is given by the relation,

$$A_i = -(h_{fe}/(1 + h_{oe}.r_L))$$

Where r_L is the A.C load resistance. Its value is equal to the parallel combination of resistance R_c and R_L. Since h_{fe} of a transistor is a positive number, therefore A_i of a common emitter amplifier is negative.

Input Resistance

The resistance looking into the amplifier input terminals (i.e. base of a transistor) is given by the relation,

$$R_i = h_{ie} + h_{re}.A_i.r_L = h_{ie} - ((h_{re}.h_{fe})/(h_{oe} + (1/r_L)))$$

The input resistance of the amplifier stage (called stage input resistance R_{is}) depends upon the biasing arrangement. For a fixed bias circuit, the stage input resistance is,

$$R_{is} = R_i // R_B$$

If the circuit has no biasing resistances, then $R_{is} = R_i$.

Voltage Gain

It is given by the relation,

$$A_v = A_i.r_1/R_i$$

Since the current gain (A_i) of a common emitter amplifier is negative, therefore the voltage gain (A_v) is also negative. It means that there is a phase difference of 180° between the input and output. In other words, the input signal is inverted at the output of a common emitter amplifier. The voltage gain, in terms of h-parameters, is given by the relation.

$$A_v = h_{fe}.r_1/(h_{ie} + \Delta h.r_L)$$

Where

$\Delta h = h_{ie}.h_{oe} - h_{re}.h_{fe}$

Output Resistance

The resistance looking into the amplifier output terminals is given by the relation,

$$R_o = (R_s + h_{ie})/(R_s.h_{oe} + \Delta h)$$

Where

R_s = Resistance of the source, and

$\Delta h = h_{ie}.h_{oe} - h_{re}.h_{fe}$

The output resistance of the stage,

$$R_{oe} = R_o // r_L$$

Overall Voltage Gain

It is given by the relation,

$$A_v = (A_v . R_{is})/(R_s + R_{is})$$

Overall Current Gain

It is given by relation,

$$A_{ie} = A_i . R_s/(R_s + R_{is})$$

Example

The h-parameters of a transistor used in a common emitter circuit are $h_{ie} = 1.0$ KΩ, $h_{fe} = 50$, $h_{re} = 1.0 \times 10^{-4}$, and $h_{oe} = 100$ μmhos. The load resistor for the transistor is 1KΩ in the collector circuit. The transistor is supplied from a signal source of resistance 1000Ω. Determine the value of input and output impedance, voltage and current gains in the amplifier stage.

Solution

Given Data:

$h_{ie} = 1$KΩ $= 1000$Ω
$h_{re} = 1.0 \times 10^{-4}$
$h_{oe} = 100$ μmhos $= 100 \times 10^{-6}$ mhos
$R_c = 1$KΩ $= 1000$Ω
$R_s = 1000$Ω

Input resistance of the amplifier stage

We know that thereis no load connected at the output of the amplifier (i.e. $R_L = 0$), therefore the value of A.C load resistance,

$r_L = Rc = 1000$Ω

we also know that current gain of a transistor,

$A_i = - (h_{fe}/(1 + h_{oe} . r_L) = -(50 / (1 + (100 \times 10^{-6}) \times 1000) = -45.5$

And the input resistance of a transistor,

$R_i = h_{ie} + h_{re} . A_i . r_L = 1000 + [(1.0 \times 10^{-4}) \times (-45.5) \times 1000] = 995$ Ω

Input resistance of the amplifier stage is,

$R_{is} = R_i = 995 \ \Omega$ **Ans.**

Output Resistance of Amplifier Stage

We know that:

$\Delta h = h_{ie}.h_{oe} - h_{re}.h_{fe}$

$= [1000 \ x \ (\ 100 \ x \ 10^{-5})] - (1.0 \ x \ 10^{-4}) \ x \ 50 = 95 \ x \ 10^{-3} = 0.095$

Output resistance of the transistor looking directly into collector.

$R_e = (R_s + h_{ie})/(R_s.h_{oe} + \Delta h)$

$= (1000 + 1000)/[1000 \ x \ (100 \ x \ 10^{-6})] + 0.95 = 2000/(0.1 + 0.95)$

$= 10300 \ \Omega$

And output resistance of the amplifier stage,

$R_{oe} = R_o \ // \ r_L = 10300 \ // \ 1000 = 910 \ \Omega$ Ans.

Current Gain of Amplifier Stage

We know that the current gain of amplifier stage,

$A_{is} = A_i.R_s/(R_s + R_{ie}) = (-45.5) \ x \ (\ 1000)/(1000 + 995) = -22.8$ **Ans.**

Voltage Gain Amplifier Stage

We know that voltage gain of a transistor,

$A_v = A_i.r_L/R_i = (-45.5) \ x \ (1000)/995 = -45.7$

Voltage gain of amplifier stage,

$A_{vs} = A_v.R_{ie}/(R_s + R_{ie}) = (-45.7) \ x \ 995/ (1000 + 995) = -22.8$ **Ans**

HYBRID EQUIVALENT FOR COMMON BASE CONFIGURATION

The figure shows the transistor connected in common emitter configuration and the figure also shows the hybrid equivalent circuit of such a transistor.

In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and base terminals. The input voltage (V_{be}) and the output current (i_c) are given by the following equations:

$$V_{be} = h_{ib}.i_b + h_{rb}.V_c$$

$$i_e = h_{fb}.i_b + h_{ob}.V_c$$

Common base transistor   Hybrid equivalent ckt for CB
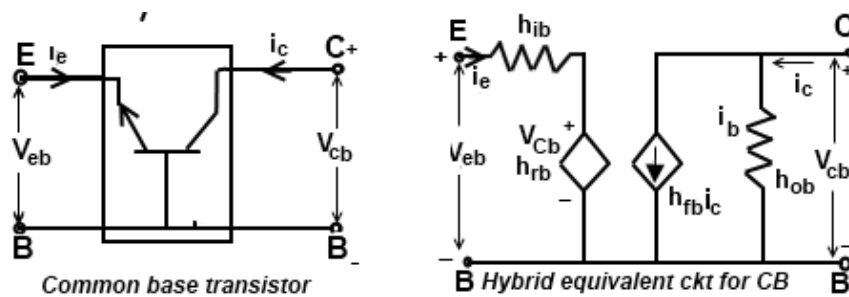
Current Gain

It is given by the relation,

$$A_i = -(h_{fb}/(1 + h_{ob}.r_L))$$

Where r_L is the A.C load resistance. Its value is equal to the parallel combination of resistance R_c and R_L. Since h_{fb} of a transistor is a positive number, therefore A_i of a common emitter amplifier is negative.

Input Resistance

The resistance looking into the amplifier input terminals (i.e. base of a transistor) is given by the relation, $$R_i = h_{ib} + h_{rb}.A_i.r_L = h_{ib} - ((h_{rb}.h_{fb})/(h_{ob} + (1/r_L)))$$

The input resistance of the amplifier stage (called stage input resistance R_{is}) depends upon the biasing arrangement. For a fixed bias circuit, the stage input resistance is, $R_{is} = R_i$

Voltage Gain

It is given by the relation,

$$A_v = A_i.r_l/R_i$$

Since the current gain (A_i) of a common base amplifier is positive, therefore the voltage gain (A_v) is also positive. It means that there is no phase difference between the input and output signals of the common base amplifier. The voltage gain, in terms of h-parameters, is given by the relation.

$A_v = h_{fb}.r_L/(h_{ib} + \Delta h.r_L)$

Where

$\Delta h = h_{ib}.h_{ob} - h_{rb}.h_{fb}$

Output Resistance

The resistance looking into the amplifier output terminals is given by the relation,

$$R_o = (R_s + h_{ib})/(R_s.h_{ob} + \Delta h)$$

Where

R_s = Resistance of the source, and

$\Delta h = h_{ib}.h_{ob} - h_{rb}.h_{fb}$

The output resistance of the stage,

$R_{os} = R_o \; // \; r_L$

Overall Voltage Gain

It is given by the relation,

$$A_{vs} = (A_v.R_{is})/(R_s + R_{is})$$

Overall Current Gain

It is given by relation,

$$A_{is} = A_i.R_s/(R_s + R_{is})$$

Example

A transistor used in a common base amplifier has the following vaules of h-parameters:

$h_{ib} = 28 \; \Omega$, $h_{fb} = -0.98$, $h_{rb} = 5 \times 10^{-4}$ and $h_{ob} = 0.34 \times 10^{-6}$ S

Calculate the values of input resistance, output resistance, current gain and voltage gain, if the load resistance is 1.2 KΩ. Assume source resistance as zero.

Solution

Given Data:

$h_{ib} = 28\ \Omega$
$h_{rb} = 5 \times 10^{-4}$
$h_{ob} = 0.34 \times 10^{-6}$ S
$r_L = 1.2$ KΩ
$R_s = 0$

Input resistance of the amplifier stage

We know that the input resistance,

Ri = hib + hrb.Ai.rL
$= 28 + [(5 \times 10^{-4}) \times 0.98 \times 1200] = 28 + 0.5 = 28\ \Omega$ Ans

Output Resistance of Amplifier Stage

We know that:

$\Delta h = h_{ib}.h_{ob} - h_{rb}.h_{fb}$

$= [23 \times (0.34 \times 10^{-6})] - [5 \times 10^{-4}) \times (-0.98)]$

Output resistance

Ro = (Rs + hib) / (Rs.hib + Δh) = hib/Δh   (as Rs = 0)

$= 28/5 \times 10^{-4} = 5.5 \times 10^{-4}\Omega = 56$ KΩ Ans.

Current Gain of Amplifier Stage

We know that the current gain of amplifier stage,

$A_i = -(h_{fb}/(1 + h_{ob}.r_L) = -(-0.98)/(1 + [(0.34 \times 10^{-6}) \times 1200] = 0.98$ *Ans.*

Voltage Gain Amplifier Stage

We know that voltage gain of a transistor,

$A_v = A_i.r_L/R_i = (0.98 \times 1200) / 28.6 = 41$ Ans.

HYBRID EQUIVALENT FOR COMMON COLLECTOR TRANSISTOR

The figure shows the transistor connected in common emitter configuration and the figure also shows the hybrid equivalent circuit of such a transistor.

In common emitter transistor configuration, the input signal is applied between the base and emitter terminals of the transistor and output appears between the collector and base terminals. The input voltage (V_{bc}) and the output current (i_c) are given by the following equations:

$$V_{bc} = h_{ic}.i_b + h_{re}.V_{ec}$$

$$i_e = h_{fe}.i_b + h_{oe}.V_{ec}$$

Common Collector Transistor   Hybrid equivalent for CC transistor
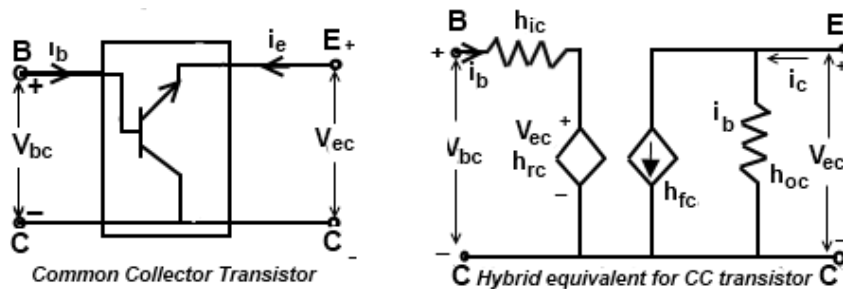
Current Gain

It is given by the relation,

$$A_i = -(h_{fc}/(1 + h_{oc}.r_L))$$

Where r_L is the A.C load resistance. Its value is equal to the parallel combination of resistance R_E and R_C. Since h_{fe} of a transistor is a positive number, therefore A_i of a common emitter amplifier is negative.

Input Resistance

The resistance looking into the amplifier input terminals (i.e. base of a transistor) is given by the relation,

$$R_i = h_{ie} + h_{re}.A_i.r_L = h_{ie} - ((h_{rc}.h_{fc})/(h_{oc} + (1/r_L)))$$

The input resistance of the amplifier stage (called stage input resistance R_{is}) depends upon the biasing arrangement. For a fixed bias circuit, the stage input resistance is,

$R_{is} = R_s$

Voltage Gain

It is given by the relation,

$$A_v = A_i.r_l/R_i$$

Since the current gain (A_i) of a common base amplifier is positive, therefore the voltage gain

(A_v) is also positive. It means that there is no phase difference between the input and output signals of the common base amplifier. The voltage gain, in terms of h-parameters, is given by the relation.

$$A_v = h_{fc}.r_L/(h_{ic} + \Delta h.r_L)$$

Where

$\Delta h = h_{ic}.h_{oc} - h_{rc}.h_{fc}$

Output Resistance

The resistance looking into the amplifier output terminals is given by the relation,

$$R_o = (R_s + h_{ic})/(R_s.h_{oc} + \Delta h)$$

Where

R_s = Resistance of the source, and

$\Delta h = h_{ic}.h_{oc} - h_{rc}.h_{fc}$

Overall Voltage Gain

It is given by the relation,

$$A_{vc} = (A_v.R_{is})/(R_s + R_{is})$$

Overall Current Gain

It is given by relation,

$$A_{is} = (A_i + R_s)/(R_i + R_{is})$$

Example:

A transistor used in a common collector amplifier has the following vaules of h-parameters:

h_{ic} = 2 KΩ, h_{fc} = -.51, h_{rc} = 1 and h_{oc} = 25 X 10^{-6}mhos

Calculate the values of input resistance, output resistance, current gain and voltage gains of the amplifier stage.

Solution

Given Data:

h_{ic} = 2 KΩ = 2000 Ω
h_{fc} = -.51
h_{rc} = 1
h_{oc} = 25 X 10^{-5}mhos
r_L = R_E = 5 KΩ = 5 X 10^3 Ω
R_s = 1 KΩ = 1000 Ω
R_1= R_2 = 10 KΩ

Input resistance of the amplifier stage

We know that the input resistance,

A_i = -(h_{fc}/(1 + h_{oc}.r_L))

= -51/[1 + {(25 x 10^{-6}) x (5 x 10^3)}]
= 45.3

and input resistance

R_i = h_{ie} + h_{re}.A_i.r_L
= 2000 + (1 x 45.3 x 5 x 10^3 Ω
= **228** x 10^3Ω
= 228 k**Ω**

As input resistace of the amplifier

R_{is} = R_1 // (R_1 // R_2)

= 228 // (10 // 10) = 4.9 k**Ω**

= 4900 Ω Ans

Output Resistance of Amplifier Stage

We know that:

$R_o = - (R_s + R_{ic})/h_{fc}$

$= - (1000 + 2000)/-51$

$= 59 \ \Omega$

and output resistance of the amplifier stage

$R_{os} = R_o \ // \ R_E$

$= 59 \ // \ (5 \ x \ 10^{-3})$

$= 58.3 \ Ans$

Current Gain

We know that the current gain of amplifier stage,

$A_{is} = -(A_i.R_s)/(R_s.R_{is}) = (45.3 \ x \ 1000)/(1000 + 4900) = 7.7 \ Ans.$

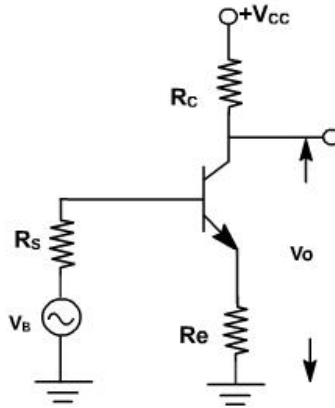**Voltage Gain Amplifier Stage**

We know that voltage gain is

$A_v = A_i.r_L/R_i = (45.3 \ X \ (5 \ x \ 10^3) \ / \ 228 \ x \ 10^3 = 1 \ Ans.$

and the voltage gain of the amplifier stage

$A_{vs} = A_v.A_{is}/(R_s + R_{is}) = (1 + 4900)/ (1000 + 4900) = 0.83 \ Ans$

ANALYSIS OF CE AMPLIFIER WITH AN EMITTER RESISTANCE

The voltage gain of a CE stage depends upon h_{fe}. This transistor parameter depends upon temperature, aging and the operating point. Moreover, h_{fe} may vary widely from device to device, even for same type of transistor. To stabilize voltage gain A_v of each stage, it should be independent of h_{fe}. A simple and effective way is to connect an emitter resistor R_e as shown in **figure below.** The resistor provides negative feedback and provides stabilization.

The Common-Emitter Amplifier is used to achieve high voltage gain and employs a bi-junction transistor (BJT). A diagram of the common-emitter amplifier is shown in figure 1.
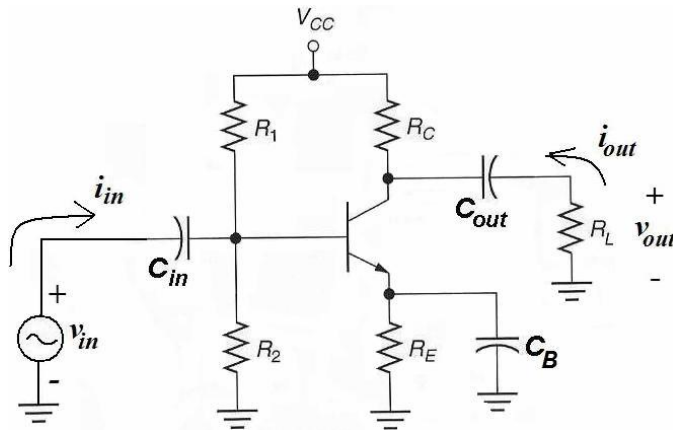
Common emitter (CE) amplifier circuit

Parameter definitions:

R_1, R_2 = Voltage Divider Resistors

R_C = Collector Resistor

R_E = Emitter Resistor

I_B = DC Base Current

I_C = DC Collector Current

I_E = DC Emitter Current

v_{in} = AC input voltage

i_{in} = AC input current

v_{out} = AC output voltage

i_{out} = AC output current

V_B = DC Base Voltage
V_C = DC Collector Voltage
V_E = DC Emitter Voltage
V_{BE} = DC Base-Emitter Voltage
V_{CC} = DC Supply Voltage
h_{FE} = DC Current Gain = $\dfrac{I_C}{I_B}$

The AC analysis of the common emitter amplifier involves replacing the transistor with its AC equivalent circuit, shown in figure..
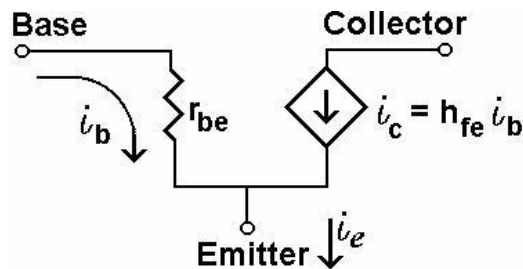
AC equivalent circuit of a bi-junction transistor

The parameters of this equivalent circuit are:

i_b = AC base current

i_c = AC collector current h_{fe} = AC Current Gain = $\dfrac{i_c}{i_b}$

i_e = AC emitter current r_{be} = Internal AC resistance of the base-emitter junction

The value of the AC current gain (h_{fe}) is typically fairly close to the DC current gain (h_{FE}). The AC resistance of the base-emitter junction (r_{be}) is calculated from:

$$r_{be} = \frac{0.025}{I_E} \quad \text{where } I_E = \text{DC Emitter Current}$$

Since this is a superposition problem, we short out the DC power supply VCC in Figure 1, and connect the AC equivalent circuit in Figure 2. We also short out all capacitors, because they will be selected to assure AC shorts over the frequency range of the input voltage, v_{in}. The result is the AC equivalent circuit of the entire amplifier shown in figure below.
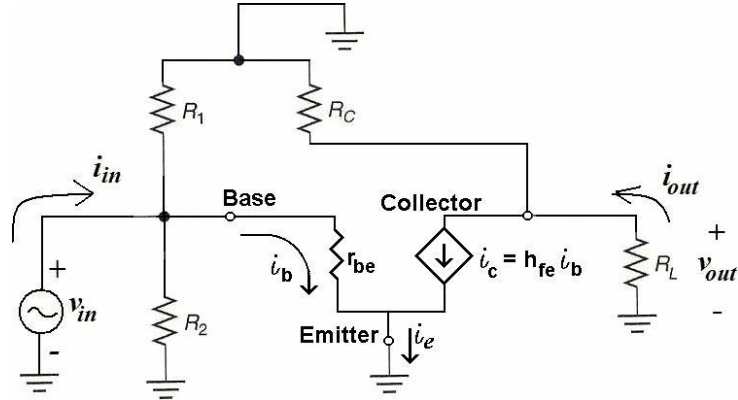
AC equivalent circuit of the common emitter (CE) amplifier

The circuit in Figure 3 can be simplified to that shown in figure below:
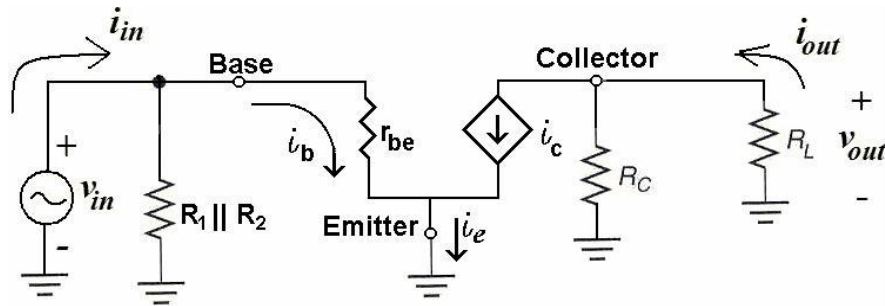
AC equivalent circuit of the common emitter (CE) amplifier

The AC resistance of the base-emitter junction (r_{be}) is calculated from:

$$r_{be} = (h_{fe} + 1) \frac{0.025}{I_E}$$

By Ohm's law, the AC base current is
$$i_b = \frac{v_{in}}{r_{be}}$$

The AC collector current is
$$i_c = h_{fe} i_b$$

The AC collector current is pulled through the parallel combination of R_C and R_L. So by Ohm's Law, the output voltage is:

$$v_{out} = i_c (R_c \| R_L)$$

LOW FREQUENCY ANALYSIS OF FET:

COMMON DRAIN CONFIGURATION:

The JFET equivalent of the BJT emitter-follower configuration is the source-follower configuration of figure shown below: Note that the output is taken off the source terminal and when the dc supply is replaced by its short-circuit equivalent, the drain is grounded.
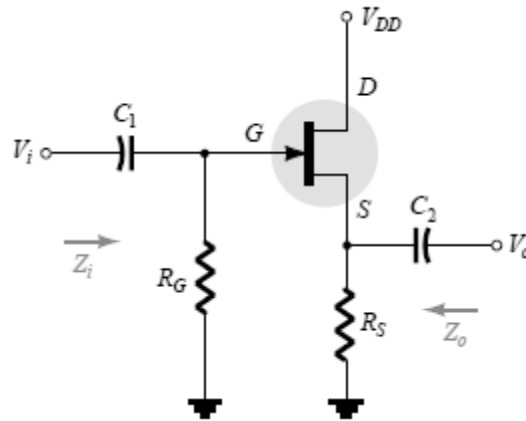
Substituting the JFET equivalent circuit will result in the configuration of figure below. The controlled source and internal output impedance of the JFET and tied to ground at one end and Rs on the other, with Vo across Rs. Since gmVgs,rd and Rs are connected to the same terminal and ground, they can all be placed in parallel as shown in figure. The current source reversed direction but Vgs is still defined between the gate and source terminals.
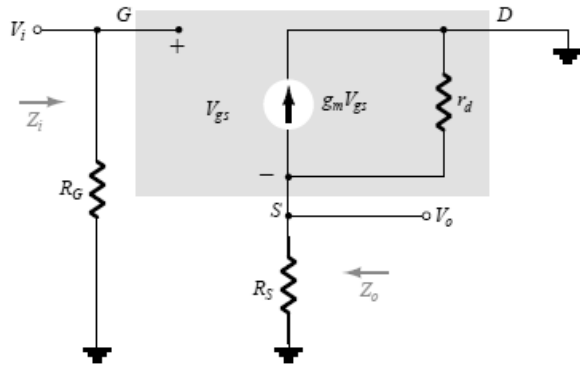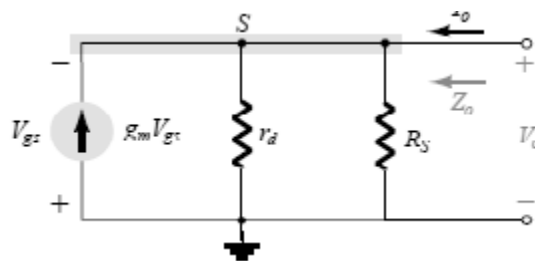
Network of Fig. 9.24 following the substitution of the JFET ac equivalent model.
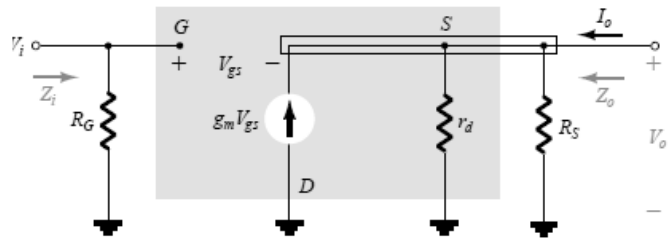
Network of Fig. 9.25 redrawn.

Zi is defined by, $Z_i = R_G$

Zo: setting Vi→0V will result in the gate terminal being connected directly to round as shown in figure below. The fact that Vgs and Vo are across the same parallel network results in Vo = -Vs.

Applying Kirchoffs's current law at node s,

$$I_0 + g_m V_{gs} = I_{rd} + I_{RS}$$

$$\frac{Vo}{rd} + \frac{Vo}{Rs}$$

$$I_o = V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m V_{gs}$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S}\right] - g_m[-V_o]$$

$$= V_o\left[\frac{1}{r_d} + \frac{1}{R_S} + g_m\right]$$

and

$$Z_o = \frac{V_o}{I_o} = \frac{V_o}{V_o\left[\dfrac{1}{r_d} + \dfrac{1}{R_S} + g_m\right]} = \frac{1}{\dfrac{1}{r_d} + \dfrac{1}{R_S} + g_m} = \frac{1}{\dfrac{1}{r_d} + \dfrac{1}{R_S} + \dfrac{1}{1/g_m}}$$

Which has the same fromat as the total resistance of three parallel resistors. Therefore

$$Zo = rd\|Rs\left\|\frac{1}{gm}\right.$$

For rd≥10Rs,

$$Zo = Rs\left\|\frac{1}{gm}\right.$$

A_V: the output voltage Vo is determined by

$$Vo = g_m V_{gs}(rd\|Rs)$$

And applying Kirchoff's voltage law around the perimeter of the network of figure will result in

$$V_i = V_{gs} + V_o$$

$$V_{gs} = V_i - V_o$$

$$V_o = g_m(V_i - V_o)\,rd\|Rs)$$

$$V_o = g_m V_i\,rd\|Rs) - gm Vo\,rd\|Rs)$$

$$Vo[1 + g_m\,rd\|Rs)] = gm Vi rd\|Rs)$$

$$Av = \frac{Vo}{Vi} = \frac{gm\,rd\|Rs)}{1 + gm\,rd\|Rs)}$$

Since the bottom of equation is larger than the numerator by a factor of one, the gain can never be equal to or greter than one
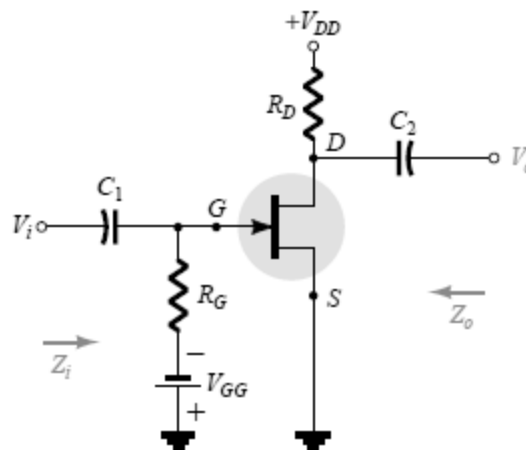
Phase relationship:

Since Av is a positive quantity, Vo & Vi are in phase for JFET source-follower configuration.

COMMON SOURCE CIRCUITS:

Fixed Bias:

The fixed-bias configuration includes the coupling capacitors C1 and C2 that isolate the dc biasing arrangement from the applied signal and load;they act as short-circuit equivalents for the ac analysis.

Once the level of gm and rd are determined from the dc biasing arrangement, specifications sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in figure. Both the capacitors have the short-circuit equivalent because the reactance $Xc - 1/2\pi fc$ is sufficiently small compared to other impedance levels of the network and the dc batteries V_{GG} and V_{DD} are set to zero volts by a short-circuit equivalent.
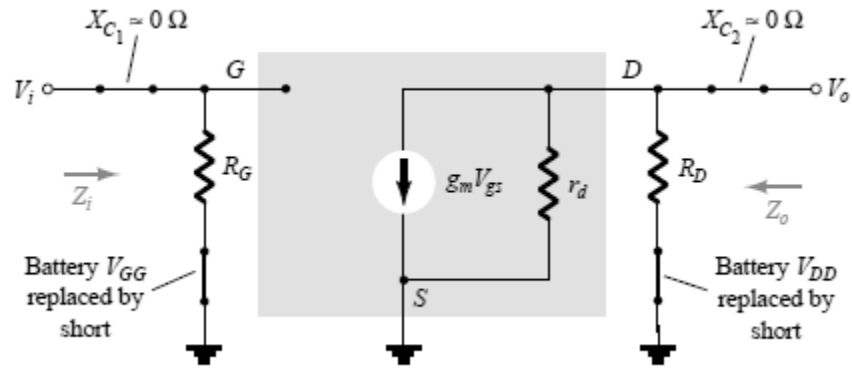
The network of figure is then carefully redrawn as shown in the above figure. The polarity of Vgs which defines the direction of gmVgs. If Vgs is negative the direction of the current source reverses. The applied signal is represented by Vi and the output signal across RD by Vo.

$$Zi=R_G$$

Because of the open circuit equivalence at the input terminals of the JFET.
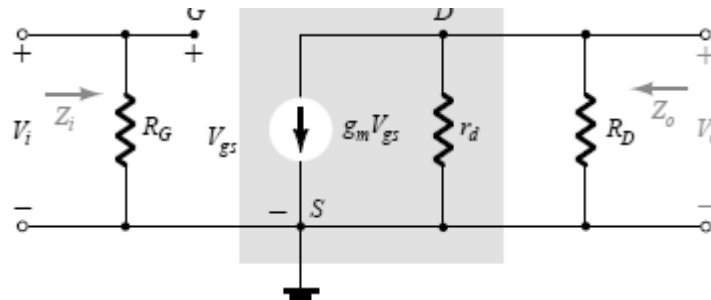
Zo: Setting Vi = oV as required by the definition of Zo will establish Vgs as 0V also. The result is gmVgs = 0mA and the current source can be replaced by an open-circuit equivalent as shown in figure above. The output impedance is

$$Zo = R_D \parallel r_d$$

If the resistance rd is sufficiently large compared to R_D, the approxiamation $R_D \parallel r_d = R_D$ can often be applied and

$$Zo \approx R_D$$
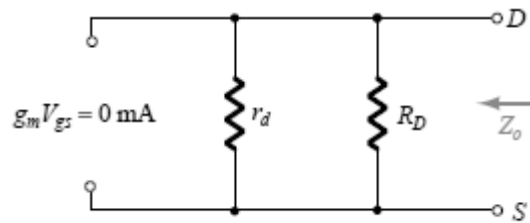
Av: Solving for Vo in the above figure, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$
$$V_{gs} = V_i$$
$$V_o = -g_m V_i(r_d \| R_D)$$

$$Av = \frac{Vo}{Vi} = -gm(R_D \| r_d)$$

If rd≥10R_D;

$$Av = \frac{Vo}{Vi} = -gmR_D$$

SELF BIAS CONFIGURATION

Bypassed Rs:

- The fixed bias configuration has the distinct disadvantage of requiring two dc voltage source.
- The self- bias configuration of fir requires only one dc supply to establish the desired operating point.
- The capacitor Cs acress the source resistance assumes its short circuit equivalence for dc, allowing Rs to define the operating point.
- Under ac conditions, the capacitor assumes the short – circuit state and " short circuits" the effect of Rs.
- If left in the ac, gain will be reduced .
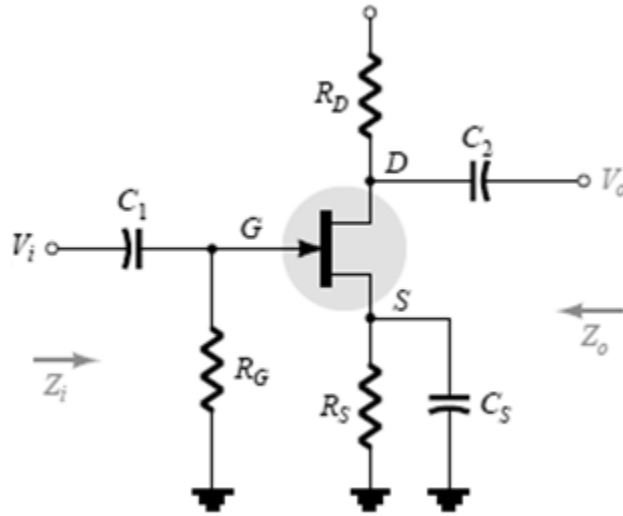
Fig : basic self bias of FET
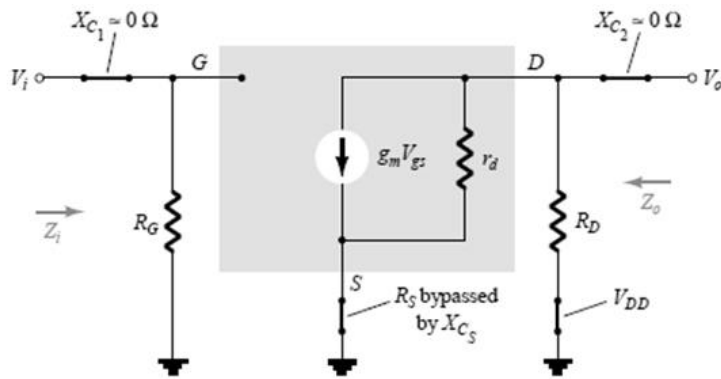
Fig: ac equivalent circuit of FET
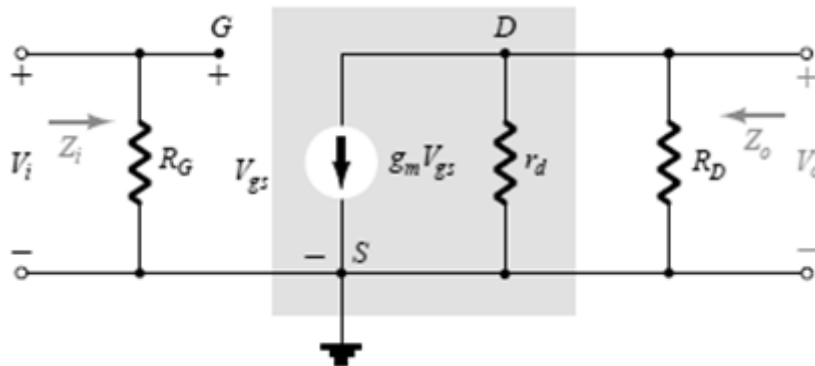
Fig: redrawn above network

Now $Z_i = R_G$

$$Zo = r_d \| R_d$$

if $r_d > 10\ R_d$ → $Zo \sim R_d$

Av:

$A_v = -g_m(r_d \| R_d)$

if $r_d > 10\ R_d$, $A_v = -g_mR_d)$

Phase relationship: The negative sign in the solution for A_v again indicates a phase shift of 180 degree between Vi and Vo

Un bypassed Rs
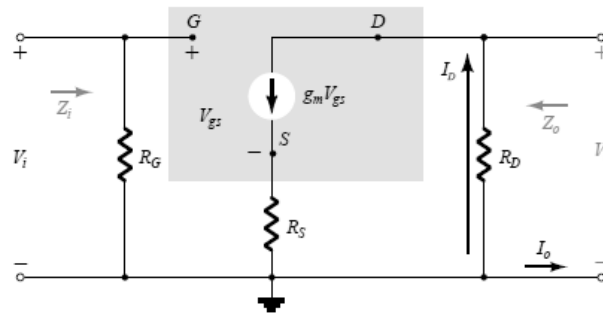
Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

- **Zi:** Due to the open circuit condition between gate and output network, the input remains the following

$$Z_i = R_G$$

- **Zo:** The output impedence is defined by

$$Zo = \frac{Vo}{Vi} \text{ at Vi =0}$$

- $setVi = 0V$, the voltage across Rg is then 0V, and Rg has been effectively shorted out.

And $Z_o = \frac{Vo}{Io} = \dfrac{-IdRs}{-Id\left(\dfrac{\left(1+gmRs+\frac{Rs}{rd}+\frac{Rd}{rd}\right)}{1+gmRs+\frac{Rs}{rd}}\right)}$

And finally,

$$Z_o = \dfrac{1 + gmRs + \dfrac{Rs}{rd} + \dfrac{Rd}{rd}}{\dfrac{Vo}{Io}} = \dfrac{1+gmRs+\frac{Rs}{rd}}{}Rd$$

For $r_d \geq 10R_D$,

$$1 + gmRs + \frac{Rs}{rd} \gg \frac{Rs}{rd} \wedge 1 + gmRs + \frac{Rs}{rd} + \frac{Rd}{rd} \quad 1 + gmRs + \frac{Rs}{rd}$$

$$Z_o = Rd$$

- **To find Av**: apply KVL to the input circuit, we get
$$V_i - V_{gs} - V_{Rs} = 0$$
$$V_{gs} = V_i - I_d R_s$$

- The voltage across rd using KVL is

$V_o - V_{Rs}$

And I' $= \frac{Vo - VRs}{rd}$

So that an application of KCL will result in

$$Id = gmVgs + \frac{Vo - VRs}{rd}$$

Substituting for Vgs for above and Substituting for Vo and Vrs we have

$$Id = gm[Vi - IdRs] + \frac{(-IdRd) - (IdRs)}{rd}$$

$$Id\left[1 + gmRs + \frac{Rd + Rs}{rd}\right] = gmVi$$

$$Id = gmVi / \left[1 + gmRs + \frac{Rd + Rs}{rd}\right]$$

The output voltage is then

$$Vo = -IdRd = gmRd\,Vi / \left[1 + gmRs + \frac{Rd + Rs}{rd}\right]$$

And $A_v = \frac{Vo}{Vi} = -\left\{\frac{gmVi}{\left[1 + gmRs + \frac{Rd + Rs}{rd}\right]}\right\}$

Again , if rd $\geq 10(R_D + R_S)$

$A_v = \frac{Vo}{Vi} = -\left\{\frac{gmRd}{[1 + gmRs]}\right\}$

Phase relationship: The negative sign indicated the a 180 degree phase shift between Vi and Vo.

FET Voltage Divider Configuration

under ac conditions.   Redrawn network
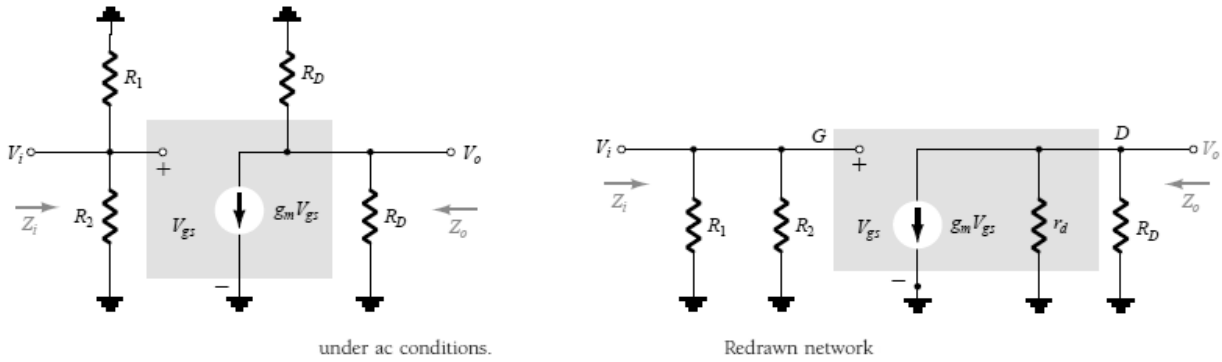
Input impedance:

Here R1 and R2 are in parallel so the equation becomes

$$Zi = R1 \| R2$$

Output impedance

Setting $Vi = 0$ will set Vgs and $V_{gs}g_m$ to zero and

$$Z0 = rd \| Rd$$

For $r_d \geq 10R_d$;

$$Z0 \sim rd$$

Av:

$V_{gs = } V_i$
and $Vo = -gmVgs(rd \vee Rd)$
so that ,

$$A_v = \frac{Vo}{Vi} = -gmVgs(rd \vee Rd)/Vgs$$

$$A_v = -gm(rd \vee Rd)$$

For $r_d \geq 10R_d$: $A_v = \frac{Vo}{Vi} - gm(rd)$

UNIT– II

Multistage Amplifiers: Need for cascading – Cascade amplifier – Cascode amplifier – Darlington Pair – Basic emitter coupled differential amplifier – Tuned amplifiers – single tuned –double tuned – stagger tuned amplifiers.

Feedback Amplifiers: Concept of feedback- topological classification-voltage series, voltage shunt, current series, current shunt - effect of feedback on gain, stability, distortion, band width, input and output impedances – practical feedback amplifier circuits and their analysis.

NEED FOR CASCADING

- To increases the voltage gain of the amplifier, multiple amplifier are connects in cascade.
- The output of one amplifier is the input to another stage. In this way the overall voltage gain can be increased, when number of amplifier stages are used in succession it is called a multistage amplifier or cascade amplifier.
- The load on the first amplifier is the input resistance of the second amplifier. The various stages need not have the same voltage and current gain.
- In practice, the earlier stages are often voltage amplifiers and the last one or two stages are current amplifiers. The voltage amplifier stages assure that the current stages have the proper input swing.
- The amount of gain in a stage is determined by the load on the amplifier stage, which is governed by the input resistance to the next stage.
- Therefore, in designing or analyzing multistage amplifier, we start at the output and proceed toward the input.

CASCADE AMPLIFIER

- An RC Coupled cascade amplifier built using BJT is shown in figure below: the need for cascading stages is the large overall voltage gain.
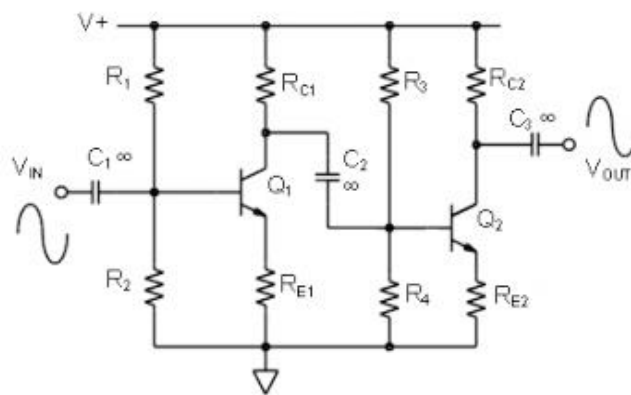
The voltage gain of each stage is

$$A_v = \frac{-R_C II R_L}{r_e}$$

The amplifier input impedance is that of stage 1,

$$Z_i = R1 II R2 II \beta re$$

And the output impedance of the amplifier is that of stage 2,

$$Z_i = RC II ro$$

CASCODE AMPLIFIER

- A Cascode connection has one transistor on top of another.
- Figure below shows a cascade configuration with a common emitter (CE) stage feeding a common-base (CB) stage.
- This arrangement is designed to provide high input impedance with a low voltage gain to ensure that the input Miller Capacitance is at a minimum with the CB stage providing good high-frequency operation.
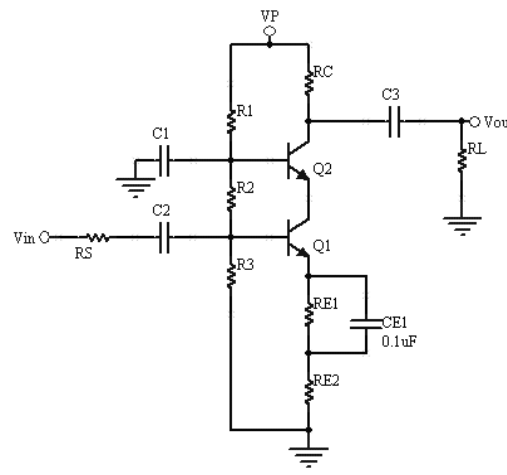
DARLINGTON AMPLIFIER

- The main feature of the Darlington connection is that the composite transistors acts as a single unit with a current gain that is the product of the current gain of the individual transistors.
- If the connection is made using two separate transistors having current gains β1β2, the Darlington connection provides a current gain of $\beta_D = \beta1\beta2$

If two transistors are matched so that β1 = β2= β. The Darlington connection provides a current gain of

$$\beta_D = \beta_D = \beta^2$$

A Darlington transistor connection provides a transistor having a very large current gain.
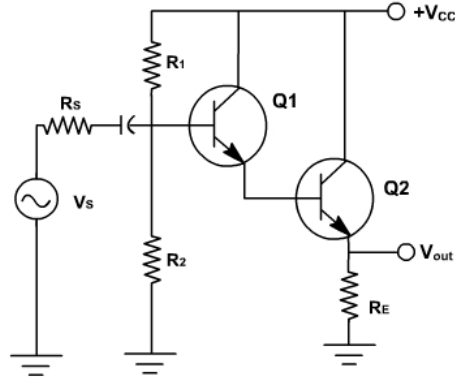
The base current may be calculated from

$$IB = \frac{VCC - VBE}{RB + \beta_D RE}$$

The emitter current is then,

$$IE = (\beta_D + 1)IB$$

Dc Voltages are

$$VE = I_E R_E$$

$$V_B = V_E + V_{BE}$$

The ac input signal is applied to the base of the Darlington transistor through capacitor C1, with the ac output, Vo, obtained from the emitter through capacitor C2. An ac equivalent circuit is shown below:

The Darlington transistor is replaced by an ac equivalent circuit comprised of an input resistance, ri and an output current source, $\beta_D = Ib$.

<u>INPUT IMPEDANCE</u>:

The ac base current through ri is

$$Ib = \frac{Vi - Vo}{Ri}$$

Since $\boldsymbol{Vo = (I_b + \beta_D I_b)R_E}$

Now,

$$\boldsymbol{I_b R_i = Vi - Vo = Vi - (I_b + \beta_D I_b)R_E}$$

The ac input impedance looking into transistor base is then,

$$\frac{Vi}{Ib} = ri + \beta_D R_E$$

And that looking into circuit is

$$Zi = R_B II(ri + \beta_D R_E)$$

CURRENT GAIN:

The ac output current through R_E is $\mathbf{Io = Ib} + \boldsymbol{\beta_D I_b} = (\boldsymbol{\beta_D} + \mathbf{1})\boldsymbol{I_b} = \boldsymbol{\beta_D I_b}$

The transistor current gain is then $\frac{Io}{Ib} = \boldsymbol{\beta D}$

The ac current gain of the circuit is, $\boldsymbol{Ai} = \dfrac{Io}{Ii} = \dfrac{\beta_D R_B}{R_B + \beta_D R_E}$

OUTPUT IMPEDANCE:

The ac output impedance can be determined for the ac circuit shown in figure. The output impedance seen by RL is determined by applying a voltage Vo and measuring the current Io. Solving for Io yields,

$$Io = \frac{Vo}{R_E} + \frac{Vo}{ri} - \beta_D I_b = \frac{Vo}{R_E} + \frac{Vo}{ri} - \beta_D \left(\frac{Vo}{ri}\right)$$

Solving for Zo gives, $\boldsymbol{Zo} = \dfrac{Vo}{Io} = \dfrac{1}{\left(^1/_{RE} + ^1/_{ri} + ^\beta/_{ri}\right)}$

VOLTAGE GAIN:

The ac voltage gain for the circuit can be determined using the ac equivalent circuit of figure. Since

$$\boldsymbol{Vo = (Ib + \beta_D I_b)R_E = Ib(R_E + \beta_D R_E)}$$

and $\boldsymbol{Vi = Ibri + (Ib + \beta_D I_b)R_E}$

Thus, $\boldsymbol{Vo} = \dfrac{Vi}{ri + R_E + \beta_D R_E}\left(R_E + \beta_D R_E\right)$

$$\boldsymbol{Av} = \frac{\boldsymbol{Vo}}{\boldsymbol{Vi}} = \frac{R_E + \beta_D R_E}{ri + R_E + \cdot \beta_D R_E} = \mathbf{1}$$

DIFFERENTIAL AMPLIFIER CIRCUIT

- The differential amplifier circuit can be described by considering the basic differential amplifier shown in figure. Notice that the circuit has two separate inputs, two separate

outputs, and that the emitters are connected together. While most differential amplifier circuits use two separate voltage supplies, the circuit can also operate using a single supply.

- A number of input signal combinations are possible.
- If an input signal is applied to either input, with the other input connected to ground, the operation is referred to as single-ended.
- If two opposite polarity input signals are applied, the operation is referred to as double-ended.
- If the same input is applied to both inputs, the operation is called common-mode.
- In single-ended operation a single input signal is applied. However, due to the common-emitter connection the input signal operates both transistors, resulting in output from both collectors.
- In double-ended operation two input signals are applied, the difference of the inputs resulting in outputs from both collectors due to the difference of the signals applied to both inputs.
- In common-mode operation the common input signal results in opposite signals a each collector, these signals cancelling so that the resulting output signal is zero. As a practical matter the opposite signals do not completely cancel and a small signal results.
- The main feature of the differential amplifier is the very large gains when opposite signals are applied to the inputs as compared to the very small gain resulting from common inputs. The ratio of this difference gain to the common gain is called common-mode rejection.

SINGLE TUNED AMPLIFIER

- A single tuned amplifier consists of a transistor amplifier containing a parallel tuned circuit as the collector load.
- The values of capacitance and inductance of the tuned circuit are so selected that its resonant frequency is equal to the frequency to be amplified.
- The output from a single tuned amplifier can be obtained either (a) by a coupling capacitor CC as shown in Fig. (i) or (b) by a secondary coil as shown in Fig. (ii).

OPERATION:

- The high frequency signal to be amplified is given to the input of the amplifier. The resonant frequency of parallel tuned circuit is made equal to the frequency of the signal by changing the value of C. Under such conditions, the tuned circuit will offer very high impedance to the signal frequency.

(i)   (ii)
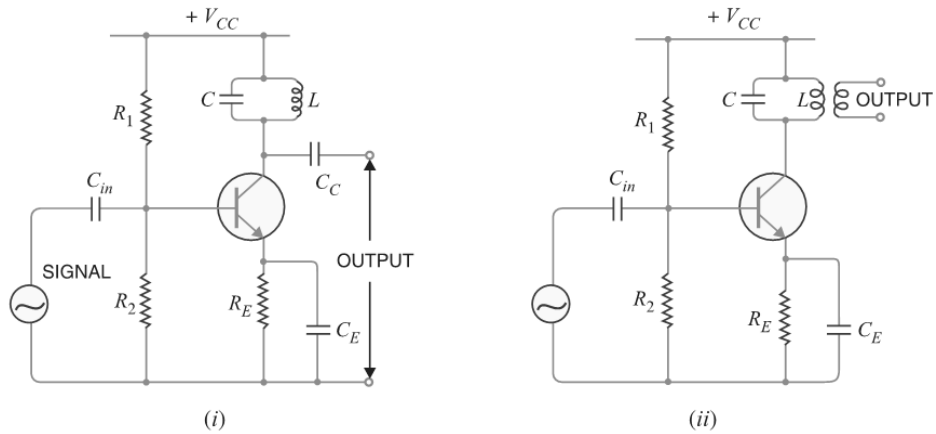
- Hence a large output appears across the tuned circuit. In case the input signal is complex containing many frequencies, only that frequency which corresponds to the resonant frequency of the tuned circuit will be amplified.
- All other frequencies will be rejected by the tuned circuit. In this way, a tuned amplifier selects and amplifies the desired frequency.

ANALYSIS OF TUNED AMPLIFIER

- Fig. below (i) shows a single tuned amplifier. Note the presence of the parallel LC circuit in the collector circuit of the transistor.
- When the circuit has a high Q, the parallel resonance occurs at a frequency fr given by:

(i)   (ii)
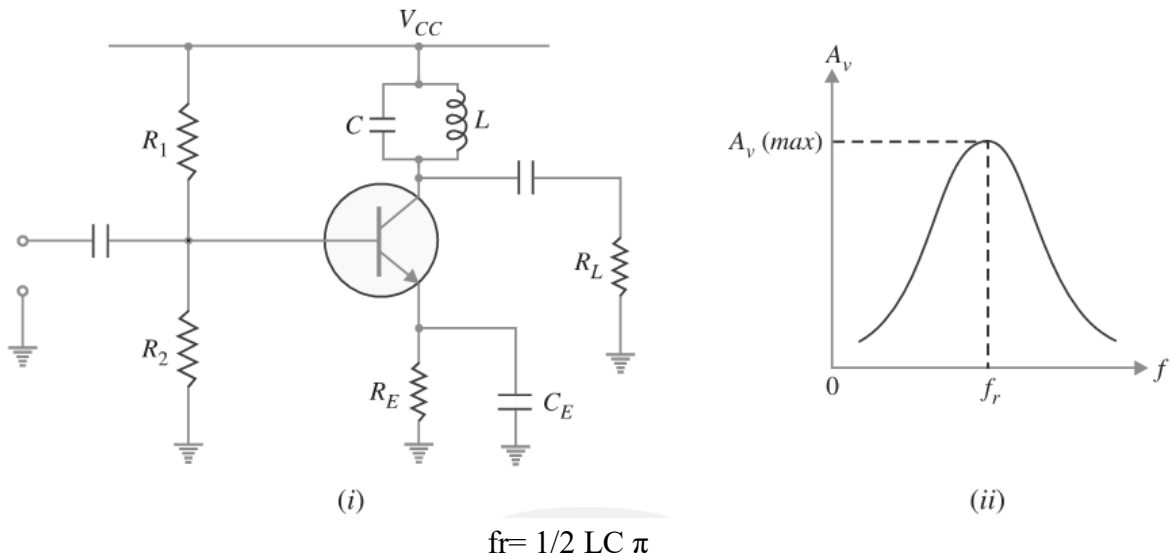
fr= 1/2 LC π

- At the resonant frequency, the impedance of the parallel resonant circuit is very high and is purely resistive. Therefore, when the circuit is tuned to resonant frequency, the voltage across RL is maximum.

- In other words, the voltage gain is maximum at fr . However, above and below the reso-nant frequency, the voltage gain decreases rapidly. The higher the Q of the circuit, the faster the gain drops off on either side of resonance [See Fig. (ii)].

A.C. EQUIVALENT CIRCUIT OF TUNED AMPLIFIER

- Fig. below (i) shows the ac equivalent circuit of the tuned amplifier. Note the tank circuit components are not shorted.
- In order to completely understand the operation of this circuit, we shall see its behaviour at three frequency conditions viz.,(i) fin = fr (ii) fin < fr (iii) fin > fr
- (i) When input frequency equals fr (i.e., fin = fr). When the frequency of the input signal is
- equal to fr, the parallel LC circuit offers a very high impedance i.e., it acts as an open. Since RL represents the only path to ground in the collector circuit, all the ac collector current flows through RL. Therefore, voltage across RL is maximum i.e., the voltage gain is maximum as shown in Fig. below (ii).
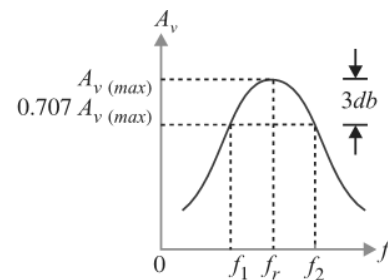
(i)   (ii)

DOUBLE TUNED AMPLIFIER

- Fig. below shows the circuit of a double tuned amplifier. It consists of a transistor amplifier containing two tuned circuits ; one (L1C1) in the collector and the other (L2C2) in the output as shown.

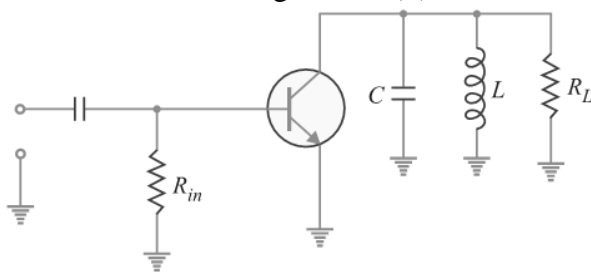(i)   (ii)

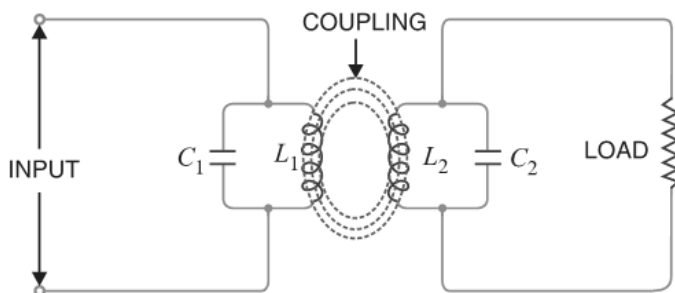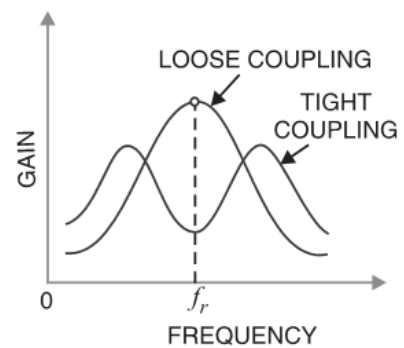- The high frequency signal to be amplified is applied to the input terminals of the amplifier. The resonant frequency of tuned circuit L1C1 is made equal to the signal frequency.
- Under such conditions, the * At frequencies below fr, XC > XL or IL > IC. Therefore, the circuit will be inductive.Transistor Tuned Amplifiers tuned circuit offers very high impedance to the signal frequency.
- Consequently, large output appears across the tuned circuit L1C1.The output from this tuned circuit is transferred to the second tuned circuit L2C2 through mutual induction.
- Double tuned circuits are extensively used for coupling the various circuits of radio and television receivers.
- The frequency response of a double tuned circuit depends upon the degree of coupling i.e. upon the amount of mutual inductance between the two tuned circuits.
- When coil L2 is coupled to coil L1 [See Fig. (i)], a portion of load resistance is coupled into the primary tank circuit L1C1 and affects the primary circuit in exactly
- the same manner as though a resistor had been added in series with the primary coil L1
- When the coils are spaced apart, all the primary coil L1 flux will not link the secondary coil L2. The coils are said to have loose coupling.
- Under such conditions, the resistance reflected from the load (i.e. secondary circuit) is small. The resonance curve will be sharp and the circuit Q is high as shown in Fig. (ii).
- When the primary and secondary coils are very close together, they are said to have tight coupling. Under such conditions, the reflected resistance will be large and the circuit Q is lower.
- Two positions of gain maxima, one above and the other below the resonant frequency, are obtained.

BANDWIDTH OF DOUBLE–TUNED CIRCUIT

- Bandwidth increases with the degree of coupling. Obviously, the determining factor in a double-tuned circuit is not Q but the coupling.
- For a given frequency, the tighter the coupling, the greater is the bandwidth. BWdt = k fr
- The subscript dt is used to indicate double-tuned circuit. Here k is coefficient of coupling.
- Practical application of Double Tuned Amplifier Double tuned amplifiers are used for amplifying radio-frequency (RF) signals.
- One such application is in the radio receiver as shown in Fig.. This is the IF stage using double tuned resonant circuits. Each resonant circuit is tuned to *455 kHz.
- The critical coupling occurs when the coefficient of coupling is cirtical=121QQ where Q1 = quality factor of primary resonant circuit (L1 C1)
- Q2 = quality factor of secondary resonant circuit (L2 C2)
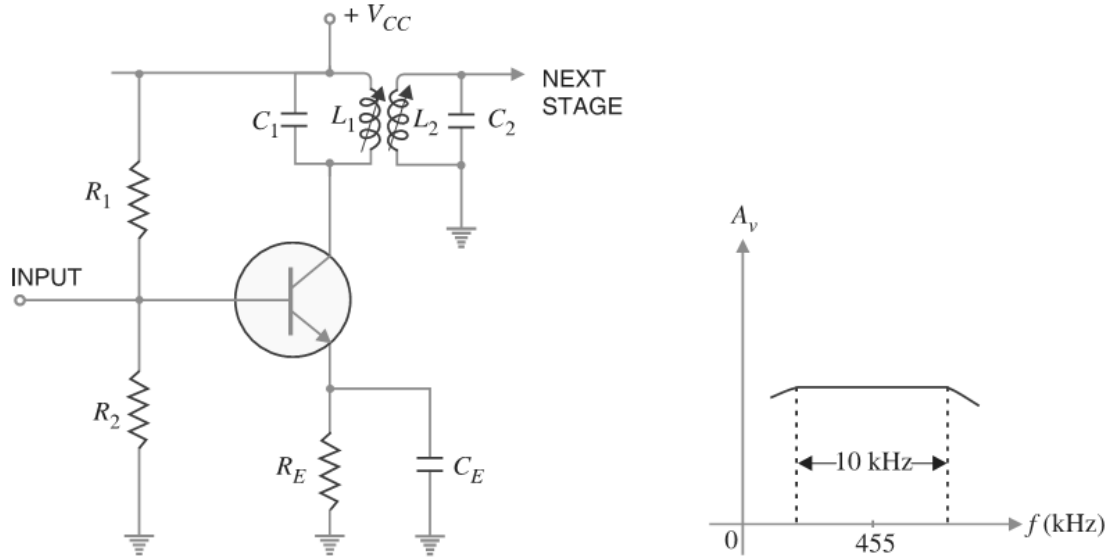
- When two resonant circuits are critically coupled, the frequency response becomes flat over a considerable range of frequencies as shown in Fig.
- In other words, the double tuned circuit has better frequency response as compared to that of a single tuned circuit.
- The use of double tuned circuit offers the following advantages :
  (i) Bandwidth is increased.
  (ii) Sensitivity (i.e. ability to receive weak signals) is increased.
  (iii) Selectivity (i.e. ability to discriminate against signals in adjacent bands) is increased.

FEEDBACK AMPLIFIERS

DEFINITION

- Feedback is defined as the process in which a part of output signal (voltage or current) is returned back to the input.
- The amplifier that operates on the principle of feedback is known as feedback amplifier.

FEEDBACK TYPES

i.   Positive Feedback (regenerative)-Eg. Oscillator-$A_f > A$

$$A_f = \frac{A}{1 - A\beta}$$

ii.   Negative Feedback (degenerative)-Eg.amplifier- $A_f < A$

$$Af = \frac{A}{1 + A\beta}$$

i) **POSITIVE FEEDBACK**:

If the original input signal and feedback signal are in phase.
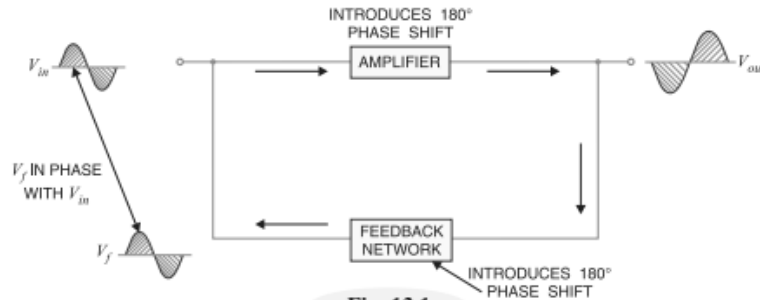
Advantages:

1. High gain

Disadvantages:

1. More distortion
2. Low band width
3. Poor gain stability compared to negative feedback amplifier

Applications

1. Used as a oscillator circuit

ii) **NEGATIVE FEEDBACK**:

If the original input signal and feedback signal are in out of phase
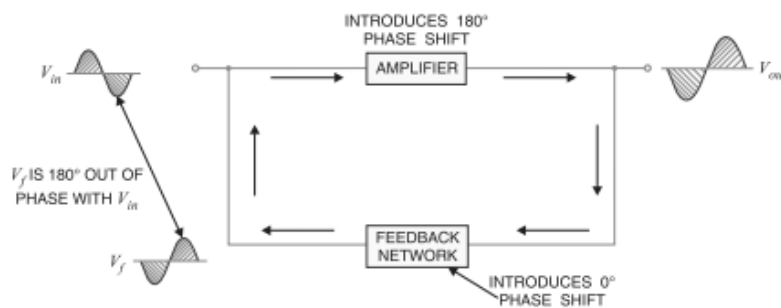
Advantages:

1. Bandwidth Extension – larger than that of basic amplified.
2. Reduction of Nonlinear Distortion

3. Control of Impedance Levels – input and output impedances can be increased or decreased.
4. Stabilizes gain

Disadvantages:

1. Reduced gain (improved by multistage amplifier were used).

Applications:

1. In almost all the electronics amplifier
2. In the regulated power supply
3. In wide band amplifier (amplifier having a large band width)

TYPES OF FEEDBACKS

There are 4 basic ways of connecting the feedback signal. Both voltage and current can be fed back to the input either in series or parallel. Specifically there can be,

1. Voltage-Series Feedback

2. Current- Series feedback

3. Current-Shunt feedback

4. Voltage-Shunt feedback

VOLTAGE SERIES FEEDBACK OR VOLTAGE AMPLIFIERS

- Voltage amplifiers are intended to amplify an input voltage signal and provide an output voltage signal.
- The voltage amplifier is essentially a voltage-controlled voltage source. A suitable feedback topology is the voltage-mixing (series connection at the input) and voltage sampling (parallel or shunt connection at the output) as shown in Fig
- Because of the Thevenin representation of the source, the feedback signal Vf should be a voltage that can be mixed with the source voltage in series.
- This topology not only stabilizes the voltage gain but also results in a higher input resistance (intuitively, a result of the series connection at the input) and a lower output resistance (intuitively, a result of the parallel connection at the output), which are desirable properties for a voltage amplifier.

$$A = \frac{V_e}{V_i}$$

$$\beta = \frac{V_f}{V_o}$$
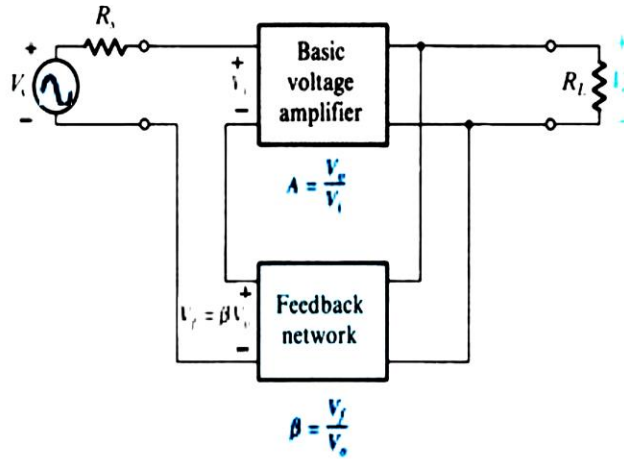
CURRENT SHUNT FEEDBACK OR CURRENT AMPLIFIERS

- The input signal in a current amplifier is essentially a current, and thus the signal source is most conveniently represented by its Norton equivalent.
- The output quantity of interest is current; hence the feedback network should sample the output current.
- The feedback signal should be in current form so that it may be mixed in shunt with the source current.
- Thus the feedback topology suitable for a current amplifier is the current mixing current-sampling topology
- Because of the parallel (or shunt) connection at the input, and the series connection at the output, this feedback topology is also known as shunt series feedback.
- This topology not only stabilizes the current gain but also results in a lower input resistance, and a higher output resistance, both desirable properties for a current amplifier.

$$A = \frac{I_o}{I_i}$$

$$\beta = \frac{I_f}{I_o}$$
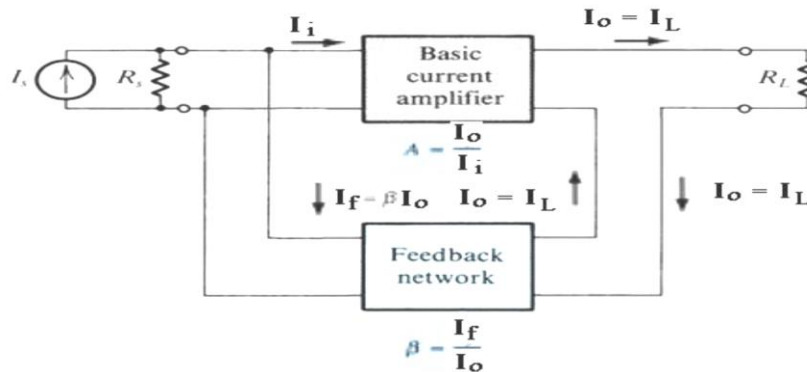
CURRENT SERIES FEEDBACK OR TRANSCONDUCTANCE AMPLIFIERS

• In transconductance amplifiers the input signal is a voltage and the output signal is a current.

• It follows that the appropriate feedback topology is the voltage-mixing current-sampling topology, illustrated in Fig
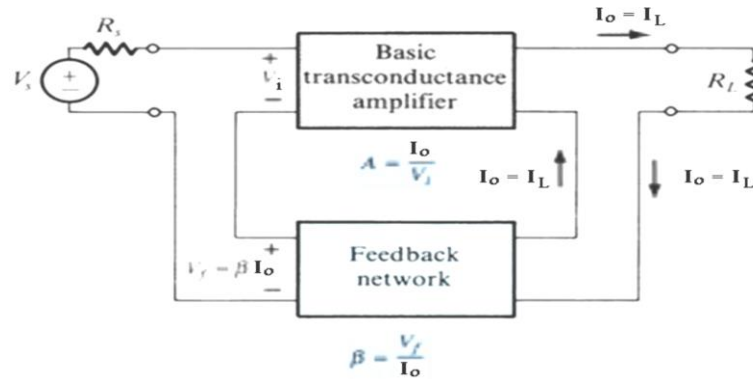
VOLTAGE SHUNT FEEDBACK OR TRANSRESISTANCE AMPLIFIERS

• In Trans resistance amplifiers the input signal is current and the output signal is voltage.

• It follows that the appropriate feedback topology is of the current – mixing voltage-sampling type, shown in Fig.

• The presence of the parallel (or shunt) connection at both the input and the output makes this feedback topology also Known as shunt - shunt feedback.
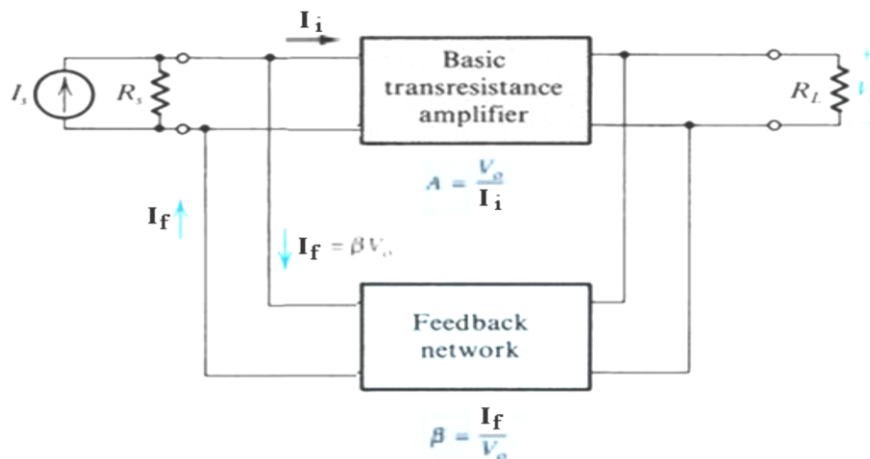
Here, the voltage refers to connecting the output voltage as input to the feedback network; Current refers to tapping off some output current through the feedback network; Series refers to connecting the feedback signal in series with the input signal voltage; Shunt refers to connecting the feedback tends to increase the output impedance.

GAIN WITH FEEDBACK:

VOLTAGE SERIES FEEDBACK:

- The voltage gain of any amplifier can be described by the formula:

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i}$$

The overall voltage gain with feedback is

$$V_{out} = A_o \qquad and \qquad V_{in} = 1 + A_o\beta$$

$$A = \frac{V_o}{V_s} = \frac{A}{1 + A\beta}$$

The above equation shows that the gain with feedback is the amplifier gain reduced by the factor $(1 + A_o\beta)$.

VOLTAGE SHUNT:

The gain with feedback for the network of figure below:

$$A = \frac{V_o}{I_s} = \frac{AIi}{Ii + I_f} = \frac{AIi}{Ii + \beta V_o} = \frac{AIi}{Ii + \beta AI_i} = \frac{A}{1 + A\beta}$$

INPUT IMPEDANCE WITH FEEDBACK:

VOLTAGE SERIES FEEDBACK:

The input impedance can be determined as follows:

$$Ii = \frac{V_i}{Z_i} = \frac{Vs - Vf}{Z_i} = \frac{Vs - \beta V_o}{Z_i} = \frac{Vs - \beta AV_i}{Z_i}$$

$$I_i Z_i = Vs - \beta AV_i$$

$$Vs = I_i Z_i = Vs - \beta AV_i = Vs - \beta AI_i Z_i$$

$$Z_{if} = \frac{Vs}{Ii} = Zi + \beta AI_i Z_i = Z_i(1 + \beta AI_i)$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1 + \beta A I_i)$ and applies to both voltage series and current series configuration.

VOLTAGE SHUNT FEEDBACK:

The input impedance can be determined to be

$$Z_{if} = \frac{Vs}{Ii} = \frac{Vi}{I_i + I_f} = \frac{Vi}{I_i + \beta V_o}$$

$$= \frac{Vi/Ii}{Ii/Ii + \beta Vo/Ii} = \frac{Zi}{1 + \beta A}$$

This reduced input impedance applies to the voltage-series connection and the voltage-shunt connection.

OUTPUT IMPEDANCE WITH FEEDBACK

The output impedance for the connections are dependent on whether voltage or current feedback is used. For voltage feedback the output impedance is decreased, while current feedback increases the output impedance.

VOLTAGE SERIES FEEDBACK:

The voltage series feedback circuit provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage, V resulting in a current I with Vs shorted out. (Vs=0).

The voltage V is then, $V = IZo + AVi$

For **Vs=0**, $Vi = -V_f$

So that $V = IZo - AV_f = IZo - A\beta V$

Rewriting the equation as $V + A\beta V = IZ_o$

Allows solving for the output resistance with feedback:

$$Z_{of} = \frac{V}{I} = \frac{Zo}{1 + A\beta}$$

The above equation shows that with voltage-series feedback the output impedance is reduced from that without feedback by the factor $(1 + A\beta)$.

CURRENT SERIES FEEDBACK:

- The output impedance with current-series feedback can be determined by applying a signal V to the output with Vs shorted out, resulting in a current I, the ratio of V to I being the output impedance.

- Figure below shows a more detailed connection with current series feedback. For the output part of a current series feedback connection shown in figure, the resulting output impedance is determined as follows, with Vs = 0, $V_i = V_f$

$$I = \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I$$

$$Z_o(1 + A\beta)I = V$$

$$Z_{of} = \frac{V}{I} = Z_o(1 + A\beta).$$

CHARACTERISTICS OF FEEDBACK AMPLIFIER:

- ### REDUCTION IN FREQUENCY DISTORTION

For a negative feedback amplifier having βA>>1, the gain with feedback is Af=1/β. It follows from this that if the feedback network is purely resistive, the gain with feedback is not dependent on frequency even though the basic amplifier gain is frequency dependent. Practically, the frequency distortion arising because of varying amplifier gain with frequency is considerably reduced in a negative feedback amplifier circuit.

- ### REDUCTION IN NOISE AND NONLINEAR DISTORTION

Signal feedback tends to hold down the amount of noise signal and nonlinear distortion. The factor $(1 + A\beta)$ reduces both input noise and resulting nonlinear distortion for considerable improvement. However, it should be noted that there is a reduction in overall gain. If additional stages are used to bring the overall gain up to the level without feedback, it should be noted that the extra stages might introduce as much noise back into the system as that reduced by the feedback amplifier. This problem can be somewhat alleviated by readjusting the gain of the feedback-amplifier circuit to obtain higher gain while also providing reduced noise signal

- ### EFFECT OF NEGATIVE FEEDBACK ON GAIN AND BANDWIDTH

The overall gain with negative feedback is shown to be

As long as βA>>1, the overall gain is approximately 1/β. For a practical amplifier the open loop gain drops off at high frequencies due to the active device and circuit capacitances. Gain mat also drop off at low frequencies for capacitively coupled amplifier stages. Once the open loop gain A drops low enough and the factor βA is no longer holds true.

Figure below shows that the amplifier with negative feedback has more bandwidth than the amplifier without feedback. The feedback amplifier has a higher upper 3-dB frequency and smaller lower 3-dB frequency.

The product of gain and frequency remains the same so that the gain bandwidth product of the basic amplifier is the same value for the feedback amplifier. However, since the feedback amplifier has lower gain, the net operation was to trade gain for bandwidth.

- ## GAIN STABILITY WITH FEEDBACK

In addition to the factor β setting precise gain value,

$$\left|\frac{dAf}{A_f}\right| = \frac{1}{|1 + A\beta|}\left|\frac{dA}{A}\right|$$

$$\left|\frac{dAf}{A_f}\right| \cong \left|\frac{1}{\beta A}\right|\left|\frac{dA}{A}\right| \ for \ \beta A \gg 1.$$

This shows that magnitude of the relative change in gain $\left|\frac{dAf}{Af}\right|$ is reduced by the factor $|\beta A|$ compared to that without feedback $\left(\left|\frac{dA}{A}\right|\right)$.

PRACTICAL FEEDBACK CIRCUITS

1. VOLTAGE SERIES FEEDBSCK

The emitter-follower circuit of figure provides voltage series feedback. The signal voltage, Vs, is the input voltage, Vi. The output voltage, Vo, is also the feedback voltage in series with the input voltage. The amplifier, as shown in figure provides the operation with feedback. The operation of the circuit without feedback provides, Vf=0. So that

$$A = \frac{V_o}{V_S} = \frac{h_{fe}I_b R_E}{V_S} = \frac{h_{fe}R_E\left(V_s/h_{fe}\right)}{V_S} = \frac{h_{fe}R_E}{h_{ie}}$$

And $\beta = \frac{Vf}{Vo} = 1$

The operation with feedback then provides that,

$$A = \frac{V_o}{V_S} = \frac{A}{1 + A\beta} = \frac{h_{fe}R_E}{h_{ie} + h_{fe}R_E}$$

For $h_{fe}R_E \gg h_{ie}$

$$A_f \cong 1.$$

2. CURRENT SERIES FEEDBACK

This is the feedback technique is to sample the output current (Io) and return a proportional voltage in series with the input. While stabilizing the amplifier gain, the current-series feedback connection increases input resistance.

Figure below shows a single transistor amplifier stage. Since the emitter of this stage has an unbypassed emitter, it effectively has current series feedback. The current through resistor R_E results in a feedback voltage that opposes the source signal applied so that output Vo is reduced. To remove the current series feedback the emitter resistor must be either removed or bypassed by a capacitor.

WITHOUT FEEDBACK

We have $A = \dfrac{I}{Vo} = \dfrac{-h_{fe}}{h_{ie}+R_E}$

$$\beta = \frac{V_f}{I_o} = \frac{-I_o R_E}{I_o} = -R_E$$

The input & output impedances are

$$`Z_i = R_B\|(h_{ie} + R_E) \cong (h_{ie} + R_E)$$

$$Zo = R_C$$

WITH FEEDBACK

$$A = \frac{Io}{Vo} = \frac{A}{1 + A\beta} = \frac{-h_{fe}}{h_{ie} + h_{fe}R_E}$$

The input and output impedance is calculated as

$$Z_{if} = Z_i(1 + A\beta) \cong h_{ie}\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right) = h_{ie} + h_{fe}R_E$$

$$Z_{of} = Zo(1 + A\beta) = R_C\left(1 + \frac{h_{fe}R_E}{h_{ie}}\right)$$

The voltage gain with feedback is,

$$A = \frac{Vo}{Vs} = \frac{IoR_C}{Vs} = \left(\frac{Io}{Vs}\right)R_C = A_f R_C \cong \frac{h_{fe}R_C}{h_{ie} + h_{fe}R_E}$$

3. VOLTAGE SHUNT FEEDBACK

The constant gain of figure below provides voltage-shunt feedback.

We have, $A = \dfrac{Vo}{Ii} = infinity$

$$\beta = \frac{I_f}{Vo} = \frac{-1}{Ro}$$

The gain with feedback is then

$$A = \frac{Vo}{Is} = \frac{Vo}{Ii} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -Ro$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback

$$Avf = \frac{Vo}{Is}\frac{Is}{Vi} = (-Ro)\frac{1}{R1} = \frac{-Ro}{R1}$$

UNIT– III

Oscillators: Barkhausen criterion for sustained oscillations - RC oscillators – RC phase shift oscillator and Wien bridge oscillator- LC oscillators - Hartley and Colpitts oscillators – crystal oscillators and frequency stability.

Multivibrators: Astable, monostable and bistable multivibrators using transistors– Schmitt trigger circuit.

OSCILLATOR

An oscillator circuit then provides a varying output signal. If the output signal varies sinusoidally, the circuit is referred to as a sinusoidal oscillator. If the output voltage rises quickly to one voltage level and later drops quickly to another voltage level, the circuit is generally referred to as pulse or square-wave oscillator.

Barkhausen criterion for sustained oscillations

It states that if A is the gain of the amplifying element in the circuit and $\beta(j\omega)$ is the transfer function of the feedback path, so βA is the loop gain around the feedback loop of the circuit, the circuit will sustain steady-state oscillations only at frequencies for which:

1. The loop gain is equal to unity in absolute magnitude, that is, $|\boldsymbol{\beta A}| = \mathbf{1}$ and
2. The phase shift around the loop is zero or an integer multiple of 2π(i.e.360^0)

Barkhausen's criterion is a *necessary* condition for oscillation but not a *sufficient* condition: some circuits satisfy the criterion but do not oscillate.

Proof: With feedback, $A_f = \dfrac{V_0}{V_s}$

$$V_i = V_s + V_f$$

$$V_f = \beta V_0 \; ; \quad V_s = V_i - V_f; \quad V_s = V_i - \beta V_0$$

$$A_f = \dfrac{V_0}{Vi - \beta V_0}$$

Dividing numerator & denominator by V_i

$$A_f = \dfrac{V_0/Vi}{Vi/vi - \beta V_0/Vi}$$

$$\boxed{A_f = \dfrac{A}{1 - A\beta}}$$

Proof: $|\beta A| = 1$

$$V_0 = A \, V_i$$

$$V_f = -\beta V_0$$

$$V_f = -\beta A \, V_i$$

$$\text{If, } V_f = V_i$$

$$V_i = -\beta A \, V_i$$

$$-\beta A = 1$$

$$\boxed{|\beta A| = 1}$$

TYPES OF OSCILLATOR

1. **RC oscillators**: They use a resistance-Capacitance network to determine the oscillator frequency. They are suitable for low (audio range) and moderate frequency applications (5Hz to 1MHz). They are further divided as,

- Phase shift oscillator
- Wien bridge oscillator and

2. **LC oscillators**: Here, inductors and capacitors are used either in series or parallel to determine the frequency. They are more suitable for radio frequency (1 to 500 MHz) and further classified as,

- Hartley
- Colpitts
- Clapp

3. **Crystal oscillator**: Like LC oscillators it is suitable for radio frequency applications. But it has very high degree of stability and accuracy as compared to other oscillators.

1. **RC oscillators**

- **PHASE SHIFT OSCILLATOR**

- A phase-shift oscillator is a linear electronic oscillator circuit that produces a sine wave output.
- It consists of an inverting amplifier element such as a transistor or op amp with its output fed back to its input through a phase-shift network consisting of resistors and capacitors.
- The feedback network 'shifts' the phase of the amplifier output by 180 degrees at the oscillation frequency to give positive feedback. Phase-shift oscillators are often used at audio frequency as audio oscillators.
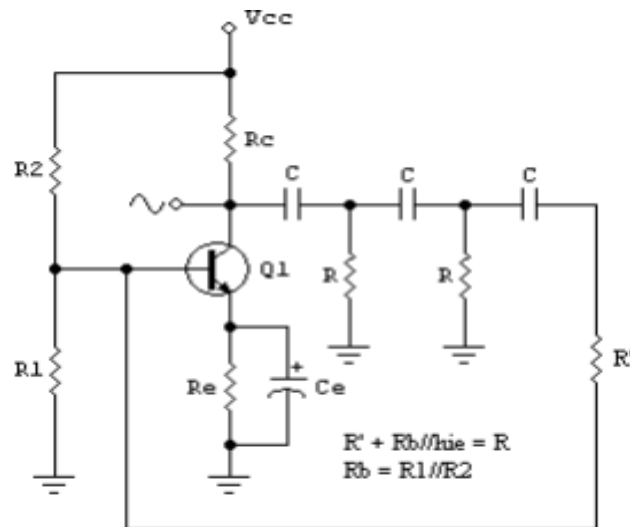
- Transistor stage (common emitter) has to produce 180° phase shift.
- 3 stage of RC combination produce remaining 180° phase shift.
- Total shift is $180^\circ + 180^\circ = 360^\circ$. This is the required condition for oscillator.

Analysis of the ac circuit provides the following equation for resulting oscillator frequency

$$f = \frac{1}{2\pi RC} \frac{1}{\sqrt{6 + 4\left(\frac{R_C}{R}\right)}}$$

For the loop gain to be greater than unity, the requirement on the current gain of the transistor is found to be

$$h_{fe} = 23 + 29\frac{R}{R_C} + 4\frac{R_C}{R}$$

Advantages

1. The circuit simple to design
2. Can produce output over AF range.
3. Produces sinusoidal output waveform
4. It is a fixed frequency oscillator.

Disadvantages

Frequency stability is poor.

WIEN BRIDGE OSCILLATOR

- A practical oscillator circuit uses RC bridge circuit, with the oscillator frequency set by the R and C components. Figure below shows the bridge connection.
- Resistors R1, R2 and capacitors C1, C2 form the frequency-adjustment element, while resistors R3 and R4 form part of the feedback path. The bridge circuit output at point b and d is the input to the transistor.
  Circuit
- Neglecting loading effects of input and output impedances, the analysis of the bridge circuit results in

$$\frac{R3}{R4} = \frac{R1}{R2} + \frac{C2}{C1}$$

And $$f_o = \frac{1}{2\pi\sqrt{R1C1R2C2}}$$

If, in particular, the values are R1=R2=R and C1=C2=C, the resulting oscillator frequency is,

$$f_o = \frac{1}{2\pi RC}$$

And $\frac{R3}{R4} = 2$.

Thus a ratio R3 to R4 greater than 2 will provide sufficient loop gain for the circuit to oscillate at the frequency calculated.

COMPARISONS OF RC & WIEN BRIDGE OSCILLATOR

| SI:NO	RC PHASE SHIFT OSCILLATOR	WIEN BRIDGE OSCILLATOR
1	It is a phase shift oscillator used for low frequency Range	It is a phase shift oscillator used for low frequency Range
2	The feedback network is the RC network with three RC Sections	The feedback is the lead-lag network which is called wein bridge circuit.
3	The feedback introduces 180° phase shift	The feedback network does not introduces phase shift
4	The frequency of oscillations, $f = \frac{1}{2\pi RC\sqrt{6}}$	The frequency of oscillations, $f = \frac{1}{2\pi RC}$
5	Amplifier gain is greater than $|A| \geq 29$	Amplifier gain is greater than $|A| \geq 3$
6	Frequency variation is difficult	Mounting the two capacitors on common shaft and varying their values, frequency can be varied.

LC OSCILLATORS:

- The oscillators which use the elements L and C to produce the oscillations are called LC oscillators.
- The circuit using elements L and C is called tank circuit or oscillatory circuit, which is an important part of LC oscillators.

- This circuit is also referred as resonating circuit, or tuned circuit.
- These oscillators are used for high frequency range from 200 KHz up to few GHz. Due to high frequency range, these oscillators are often used radio frequency.

HARTLEY OSCILLATOR

- The resistances R1 and R2are the biasing resistances.
- The RFC is the ratio frequency choke. Its reactance value is very high for high frequencies, hence it can be treated as open circuit. While for dc conditions, the reactance is zero hence causes no problem for dc capacitors.
- Hence due to RFC, the isolation between ac and dc operation is achieved. R_E is also a biasing circuit resistance and C_E is the emitter by pass capacitor. C_{C1} and C_{C2} are the coupling capacitor.
- The common emitter amplifier provides a phase shift of 180°. As emitter is grounded, the base and collector voltages are out of phase by 180°.

Oscillator Type	Reactance Elements in the tank circuit		
	X1	X2	X3
Hartley Oscillator	L	L	C
Colpitts Oscillator	C	C	L
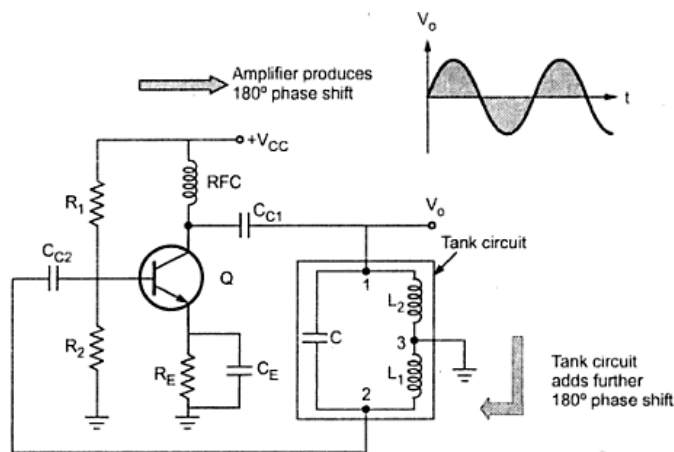
- As the centre of L1 and L2 is grounded, when upper end becomes positive, the lower becomes negative and vice versa. So the LC feedback network gives an additional phase shift of 180°, necessary to satisfy oscillation conditions. However L1 andL2 have mutual coupling.
- M which must be taken into account in determining the equivalent inductance for the resonant tank circuit.

- The circuit frequency of oscillation is then given approximately by, $fo = \dfrac{1}{2\pi\sqrt{L_{equ}C}}$

Where, **Leq= L1+L2+2M.**

- The frequency may be adjusted using a single variable capacitor, one side of which can be earthed
- The output amplitude remains constant over the frequency range
- Either a tapped coil or two fixed inductors are needed, and very few other components
- Easy to create an accurate fixed-frequency Crystal oscillator variation by replacing the capacitor with a (parallel-resonant) quartz crystal or replacing the top half of the tank circuit with a crystal and grid-leak resistor (as in the Tri-tet oscillator).

Disadvantages

- Harmonic-rich output if taken from the amplifier and not directly from the LC circuit (unless amplitude-stabilisation circuitry is employed).

COLPITTS OSCILLATOR

- The basic circuit is same as transistorized Hartley oscillator, except the tank circuit.
- The common emitter causes a phase shift of 180o, while the tank circuit adds further 180o phase shift, to satisfy the oscillating conditions.
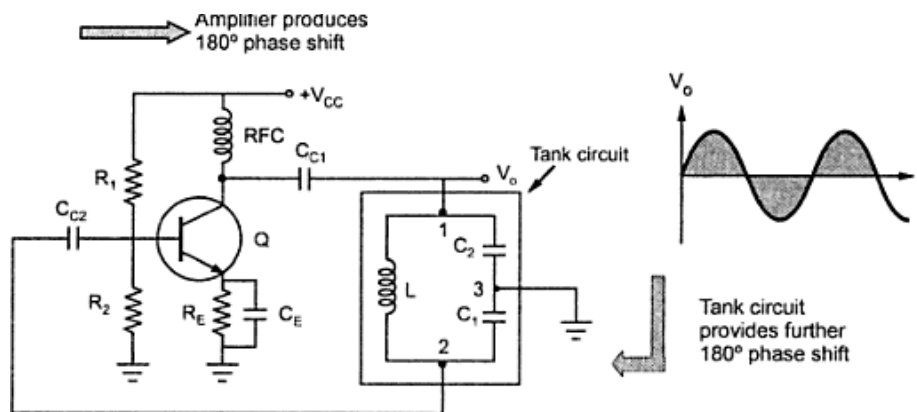
The oscillator frequency can be found be $f_o = \dfrac{1}{2\pi\sqrt{LC_{equ}}}$

Where, $C_{eq} = \dfrac{C1C2}{C1+C2}$

Advantages

- Good wave purity
- Fine performer at high frequency
- Good stability at high frequency
- Wide operation range 1 to 60 MHz

Disadvantages:

- Poor isolation (Load impedance v.s. frequency)
- Hard to design

CRYSTAL OSCILLATOR

- For an oscillator, the frequency of the oscillations must remain constant.
- The measure of ability of an oscillator to maintain the desired frequency as precisely as possible for as long a time as possible is called frequency stability of an oscillator.
- In a transistorized colpitts oscillator or Hartley oscillator, the base-collector junction is reverse biased and there exists an internal capacitance which is dominant at high frequencies. This capacitance affects the value of capacitance in the tank circuit and hence the oscillating frequency.
- Similarly the transistor parameters are temperature sensitive. Hence as temperature changes, the oscillating frequency also changes and no longer remains stable. Hence practically the circuits cannot provide stable frequency.

FACTORS AFFECTING THE FREQUENCY STABILITY:

In general following are the factors which affect the frequency stability of an oscillator:

1. Due to the changes in temperature, the values of the components of tank circuit get affected. So changes in the values of inductors and capacitors due to the changes in the temperature are the main cause due to which frequency does not remain stable.
2. Due to the changes in temperature, the parameters of the active device used like BJT, FET get affected which in turn affect the frequency.
3. The variation in the power supply is another factor affecting the frequency.
4. The changes in the atmospheric conditions, aging and unstable transistor parameters affect the frequency.
5. The changes in the load connected, affect the effective resistance of the tank circuit.
6. The capacitive effect in transistor and stray capacitances, affect the capacitance of the tank circuit and hence the frequency.

The frequency stability can be improved by the following modifications:

1. Enclosing the circuit in a constant temperature chamber.
2. Maintaining constant voltage by using the zener diodes.
3. The load effect is reduced by coupling the oscillator to the load loosely or with the help of a circuit having high input impedance and low output impedance.

CONSTRUCTION:

- A Crystal oscillator is basically a tuned circuit oscillator using piezoelectric crystal as a resonant tank circuit.

- The crystal has a greater stability in holding constant at whatever frequency the crystal is originally cut to operate.
- Crystal oscillators are used whenever great stability is required, for example, in communication transmitters and receivers.
- The natural shape of a quartz crystal is a hexagon prism. But for its practical use, it is cut to the rectangular slab. This slab is then mounted between the two metal plates.
- The symbolic representation of such a practical crystal is shown in figure below. The metal plates are called holding plates, as they hold the crystal slab in between them.
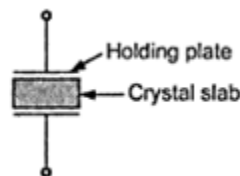
- When the crystal is not vibrating, it is equivalent to a capacitance due to the mechanical mounting of the crystal. Such a capacitance existing due to the two metal plates separated by a dielectric like crystal slab, is called mounting capacitance denoted as C_M.
- When it is vibrating, there are internal frictional losses which are denoted by a resistance r. while the mass of the crystal, which is indication of its inertia is represented by an inductance L.
- In vibrating condition, it is having some stiffness, which is represented by a capacitor C.
- The mounting capacitance is a shunt capacitance. And hence the overall equivalent circuit of a crystal can be shown as in figure:
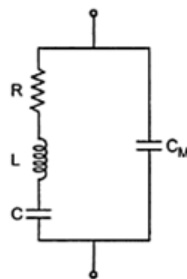
- RLC forms a resonant circuit. The expression of a resonant frequency fr is,

$$f_r = \frac{1}{2\pi\sqrt{LC}}\sqrt{\frac{Q^2}{1+Q^2}}$$

Where, Q- Quality of a quartz crystal , $Q = \frac{\omega L}{R}$

- The Q factor of the crystal is very high typically 20,000. Value of Q up to 10^6 also can be achieved. Hence the factor $\sqrt{\frac{Q^2}{1+Q^2}}$ approaches to unity and we get the resonating frequency as,
- $f_r = \frac{1}{2\pi\sqrt{LC}}$
- The crystal frequency is inversely proportional to thickness of the crystal,
- $f \propto \frac{1}{t}, where\ t\ is\ the\ thickness$
- So to have very high frequencies, thickness of the crystal should be very small. But it makes the crystal mechanically weak and hence it may get damaged, under the vibrations. Hence practically crystal oscillators are used up to 200 or 300 KHz on;y.
- The crystal has two resonating frequencies, series resonant frequency and parallel resonant frequency.

SERIES AND PARALLEL RESONANCE

- One resonant condition occurs when the reactance of series RLC leg are equal i.e. XL= XC. This is nothing but the series resonance.
- The impedance offered by this branch, under resonant condition is minimum, which is resistance R. the series resonance frequency is same as the resonating given by the equation,

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

- The other resonant condition occurs when the reactance of series resonant leg equals the reactance of the mounting capacitor CM. this is parallel resonance or anti resonance condition.
- Under this condition the impedance offered by the crystal to the external circuit s maximum.
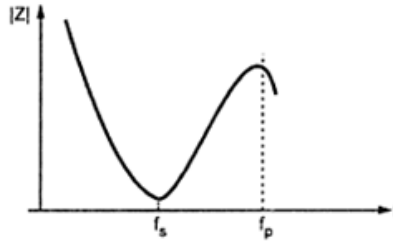- Under parallel resonance, the equivalent capacitance is,

$$C_{eq} = \frac{C_M C}{C_M + C}$$

Hence the parallel resonating frequency is given by,

$$fp = \frac{1}{2\pi\sqrt{L_{equ}C}}$$

- When the crystal capacitance C is much smaller than CM, then the figure below shows the behavior of crystal impedance versus frequency.

- Generally values of fs and fp are very close to each other and practically it can be said that there exists only one resonating frequency of a crystal.
- Higher the Q is the frequency of the crystal. Due to high frequency it gives higher stability.

MULTIVIBRATORS

- The electronic circuits which are used to generate non-sinusoidal waveforms are called multivibrators.
- The different types of sinusoidal as well as non-sinusoidal waveforms are used in variety of electronic applications.
- The sinusoidal waveforms include the waveforms such as square wave, rectangular wave, triangular wave, saw tooth wave, ramp, etc., there are certain electronic circuits which are in use to generate such non-sinusoidal waveforms.

TYPES OF MULTIVIBRATORS

**Ther are three types of mulitvibrator circuits in use, namely,**

1. Astable Multivibrator
2. Bistable Mutivibrator
3. Monostable Multivibrator

ASTABLE MULTIVIBRATOR

- The astable or free running multivibrator generates square wave without any external triggering pulse. It has no stable states, i.e. it has two quasi stable states.
- It switches back And forth from one state to the other, remaining in each state for a time depending upon the discharging of a capacitive circuit.
- Figure below shows a basic symmetrical transistor astable multivibrator in which components in one half of a cycle of the circuit are identical to their counterpart in the other half.
- The square wave output can be taken from collector point Q1 or Q2. The waveforms at base and collector of transistors Q1 and Q2 are shown.

- When the supply voltage +Vcc is applied, one transistor will conduct more than the other due to some circuit imbalance. Initially, let us assume that Q1 is conducting and Q2 is cut-off. Then VC1, the output of Q1 is equal to VCE(sat) i.e. approximately zero volt and VC2 = +Vcc. At this instant, C1 charges exponentially with a time constant R1C1 towards the supply voltage trough R1 and correspondingly, VB2 also increases exponentially towards Vcc.
- When B2 crosses the cut-in voltage, Q2 starts conducting and VC2 falls to VCE(Sat). Also, VB1 falls due to to capacitive coupling between collector of Q2 and base of Q1, thereby driving Q1, into OFF state. Now the rise in voltage Vc1 is coupled through C1 to the base of Q2, causing a small overshoot in voltage Vg2. Thus Q1 is OFF and Q2 is ON. At this instant, the voltage levels are:

  VB1 is negative. Vc1 = Vcc, VB2= VBE(Sat) and VC2 = VCE(Sat).
- It is clear that when Q2 is ON, the falling voltage VC2 permits the discharging of the capacitor C2 which drives Q1 into cut-of. The rising voltage of VC1 feeds back to the base of Q2 tending to turn it ON. This process is said to be regenerative.
- The ON time for Q1 is T1= R1C1 in 2=0.693 R1C1
- Similarly, the ON time for Q2 is T2 = R2C2in 2 = 0.693R2C2.
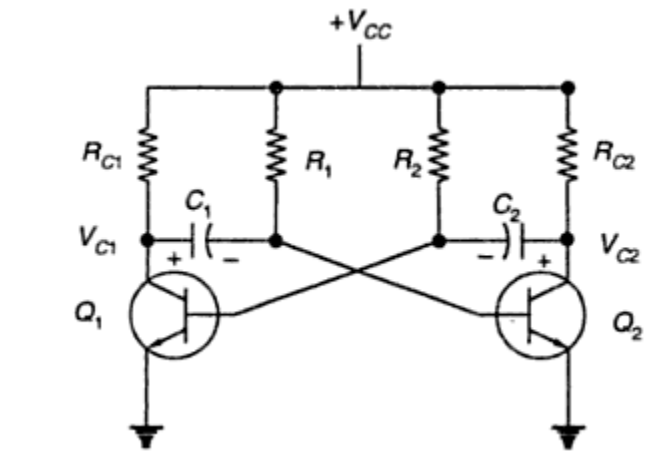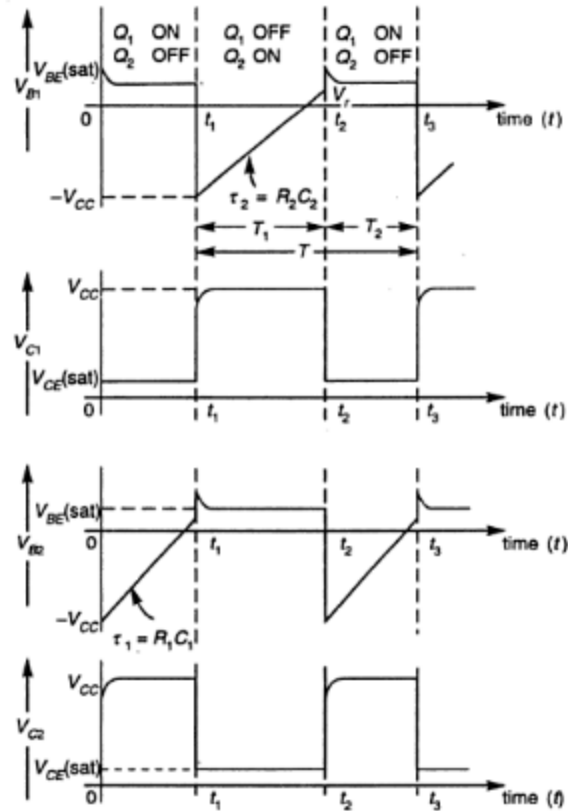
Applications

1. The various applications of astable multivibrator are:
2. Used as a square wave generator, voltage to frequency converter etc.,
3. Used as a clock for binary logic signals
4. Used in the digital voltmeter and switched mode power supplies.
5. As an oscillator to generate wide range of audio and radio frequencies.
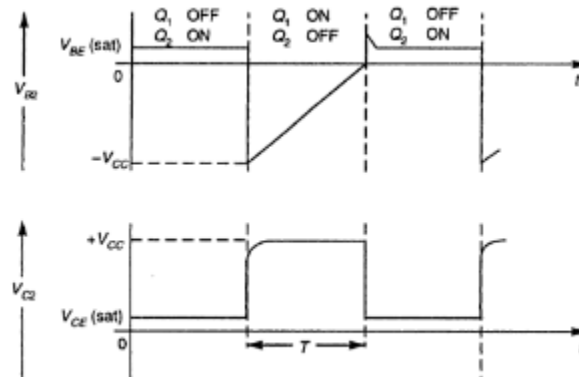
MONOSTABLE MULTIVIBRATOR

- Monostable Multivibrator has one stable state and one quasi-stable state. It is also known as one shot multivibrator or univibrator.
- T remains in its stable state until an input pulse triggers it into its quasi-stable state for a time duration determined by discharging an RC circuit and the Circuit returns to its original stable state automatically.
- It remains there until the next trigger pulse is applied. Thus a monostable multivibrator cannot generate square wave of its own like an astable multivibrator. Only external trigger pulses will cause it to generate the rectangular waves.
- Figure below shows the circuit of a transistor monostable multivibrator and the output waveforms are shown. It consists of two identical transistors Q1 and A2 with equal collector resistances of Rc1 andRc2. The output of Q2 is coupled to the input at the base of Q1

through a resistive attenuator in which C1 is a small speed up capacitor to speed up the transition. The values of R2 and –VBB are chosen so as to reverse bias Q1 and keep it in the ON state. Actually, this is the stable state for the circuit.

- When a positive trigger pulse of short duration and sufficient magnitude is applied to the base of Q1 through C2, transistor Q1 starts conducting and thereby decreasing the voltage at its collector Vc1 which is coupled to the base of Q2 through capacitor C. This decrease the forward bias on Q1 and its collector current decreases.
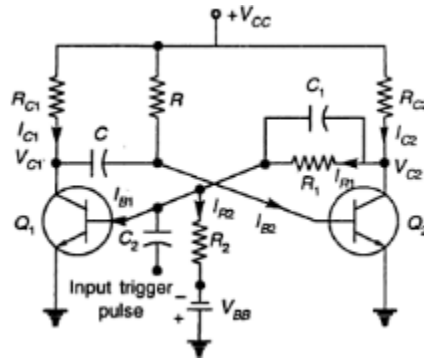
- The increasing positive potential on the collector of Q2 is applied to the base of Q1 through R1. This further increase the base potential of Q1 and Q2 is quickly driven to saturation and Q2 to Cut-off.
- The capacitor C is charged to approximately +Vcc through the path Vcc, R and Q1. As the capacitor C discharges, the base of Q2 is forward biased and collector current starts to flow into Q2. Thus Q2 is quickly driven to saturation and Q1 is cut-off. This is the stable state for the circuit and remains in this condition until another trigger pulse causes the circuit to switch over the states.
- The duration of the output pulse of the monostable multivibrator is given by Y=0.69 RC
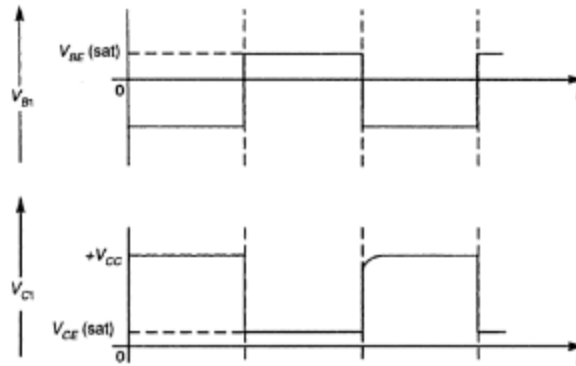
Applications:

1. The monostable multivibrator is used to function as an adjustable pulse width generator.
2. It is used to generate uniform width pulses from a variable width input pulse train.
3. It is used to generate clean and sharp pulses from the distorted pulses. It is used as a time delay unit since it provides a transition at a fixed time after the trigger signal.

BISTABLE MULIVIBRATOR:

- The bistable multivibrator is also referred to as flip-flop, it has two stable states.
- A trigger pulse applied to the circuit will cause it to switch from one state to the other. Another trigger pulse is then required to switch the circuit back to its original state.
- Figure below shows the circuit of a bistable multivibrator using two NPN transistors. In this circuit the output of a transitor of Q2 is coupled to the base of Q2 through resistor R2. Similarly the ouput of Q1 is coupled to the base of Q2 through a resistor R1.
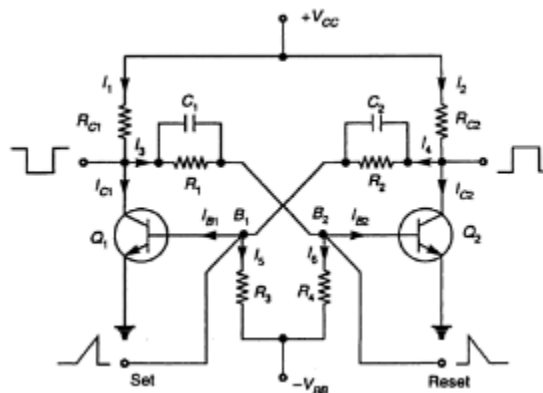
- The main purpose of capacitors C1and C2 is to improve the switching characteristics of the cirucit by passing the high frequency components of these square wave pulses. This allows fast rise and fall times, so that these square waves will not be distorted. C1 and C2 are thus called commutating capacitors.
- When the circuit is first switched on, one of the transistors will start conducting more than the other. This transistor is thus driven into saturation.

- Then, because of the regenerative feedback action, the other transistor is taken into cut-off state. Let us assume that transistor Q1 is ON and Q2 is OFF. It is a stable state of the circuit and will remain in this state till a trigger pulse is applied from outside.
- A positive triggering pulse applied to the reset input increases its forward bias, thereby turning transistor Q2 ON and an increase in collector current and a decrease in collector voltage.
- The fall in collector voltage is coupled to the base of Q1, where it reverse biases the base-emitter circuit and Q1 is positive trigger pulse is applied to set input.
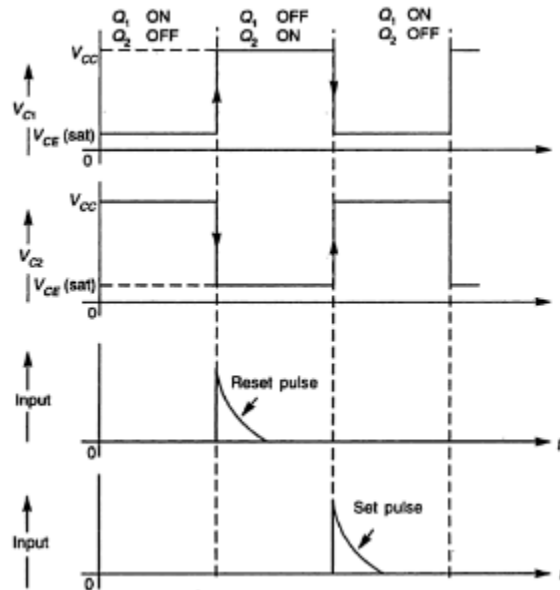

- A similar action can be achieved by applying a negative pulse at the set input for transition fro the first stable state to the second stable state and by applying a negative pulse at the reset input, reverse transition can be obtained.
- Figure above shows the waveforms at the collector of transistor Q1 and Q2 of the bistable multivibrator in response to the trigger pulses applied to the set and reset input. It is evident from these waveforms that the output waveforms are the complement of each other.
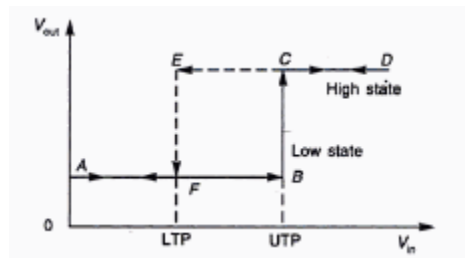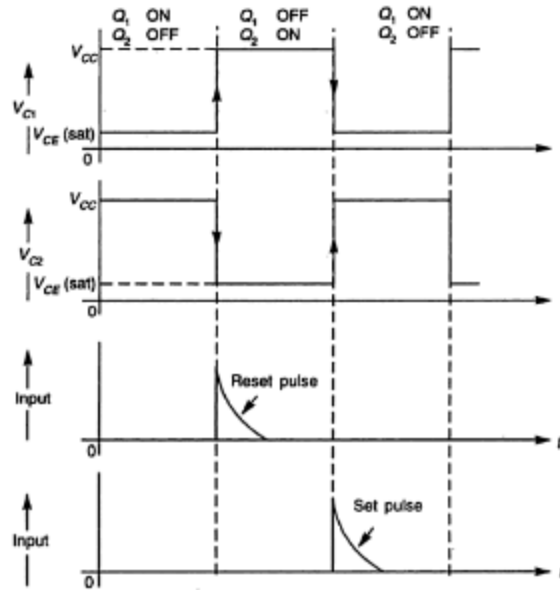
Applications:

1. The bistable multivibrator is used as memory element in shift registers, counters, and so on.
2. It is used to generate square waves of symmetrical shape by sending regular triggering pulse to the input. By adjusting the frequency of the input trigger pulse, the width of the square wave can be altered.
3. It can also be used as a frequency divider

SCHMITT TRIGGER

- Schmitt Trigger is a wave shaping circuit, used for generation of a square wav from a sine wave input. It is a bistable circuit in which two transistor switches are connected regeneratively.
- Consider an a.c. signal of sinusoidal or triangular variation applied to the base of Q1. When the voltage increases above zero, nothing will happen till it crosses the upper trigger level (UTL). As the input voltage increases above UTL, i.e. Vss> VRE + VBE, Q1conducts.
- The point at which Q1 starts conducting is known as Upper trigger point (UTP). As the transistor Q1 conducts, its collector voltage falls below Vcc. Since the collector of Q1 is coupled to base of Q2, the forward bias to Q2 is reduced. This in turn reduces the current of transistor Q1 and hence the voltage drop across RE. As a result, the reverse bias of transistor Q1 is reduced and a conducts more which drives Q2 to nearer to cut-off. At this instant, the collector voltage levels are $V_{C1} = V_{CE(Sat)}$ and $V_{C2} = Vcc$.
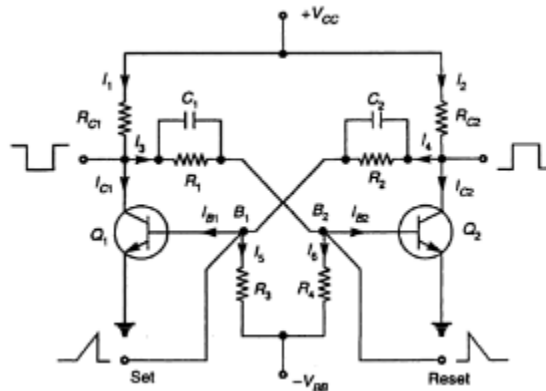
- Transistor Q1 will continue to conduct till the input voltage crosses the Lower trigger level (LTL). When the input voltage becomes equal to LTL, the emitter-vase junction of Q1 becomes reverse biased. i.e Vin < V_{BE} + V_{BE1}.Hence its collector voltage stars rising towards Vcc.
- This forward biases Q1 and it starts conducting. The point at which Q2 statrs conducting is called Lower trigger point (LTP). Then Q2 is very quickly driven into saturation and Q1 is cut-off. At this instant the collector voltage levels are V_{C1} = Vcc and V_{C2} = $V_{CE(Sat)}$. No change in state will occur during the negative half cycle of the input voltage.
- The difference between UTP and LTP is known as Hysteresis voltage (V_R) as shown in figure. V_{tt} is also known as Dead zone of the schmitt Trigger.
- The lagging of the lower threshold voltage from the upper threshold voltage is known as the Hysteresis

Applications

1. Schmitt trigger is used for wave shaping circuits
2. It can be used for generation of a rectangular waveforms with sharp edges from a sine wave orany other waveform
3. It can be used as a voltage comparator.
4. The hysteresis in schmitt trigger is variable when conditioning noisy signals for using digital circuits. The noise does not cause false triggering and so the output will be free from noise.

UNIT– IV

Wave Shaping Circuits: RC Integrator and Differentiator circuits – Storage, Delay and Calculation of Transistor Switching Times – Speed-up Capacitor- Clamper circuits – positive, negative and biased clampers -Voltage doubler, tripler and quadrupler circuits.

Time Base Generators: General features of time base signals – RC ramp generator – constant current ramp generator, UJT saw tooth generator – Bootstrap ramp generator – Miller integrator ramp generator – triangular waveform generator – pulse generator circuit – function generator – sine wave converter.

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WAVE SHAPING CIRCUITS

- A process by which non sinusoidal waveforms are altered in passing through the circuit elements (such as diodes, resistors, inductors & capacitors) is called wave shaping.
- Wave shaping performed following functions:
    1. To generate one wave from the other.
    2. To limit the voltage level of the waveform to some preset value and suppressing all other voltage levels in the excess of the preset level.
    3. To cut-off positive & negative portions of the input waveform.
   4. To hold the waveform to a particular d.c level.

TYPES

- L**inear wave shaping circuits -** the circuits, which make use of only linear circuit elements such as L, C and R. Such circuits are performed differentiation and integration.

- **Non linear wave shaping circuits -** the circuits, which (in addition to linear circuit elements) make use of non linear circuit elements such as diodes and transistors. Such circuits are performed amplitude limiting, clipping and clamping.

RC **integrator**
- An *RC* integrator is a circuit that approximates the mathematical process of integration. Integration is a summing process, and a basic integrator can produce an output that is a running sum of the input under certain conditions.
- A basic *RC* integrator circuit is simply a capacitor in series with a resistor and the source. The output is taken across the capacitor.
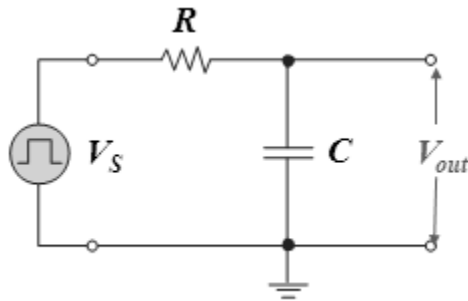
- When a pulse generator is connected to the input of an RC integrator, the capacitor will charge and discharge in response to the pulses.
- When the input pulse goes HIGH, the pulse generator acts like a battery in series with a switch and the capacitor charges.

The output is an exponentially rising curve.
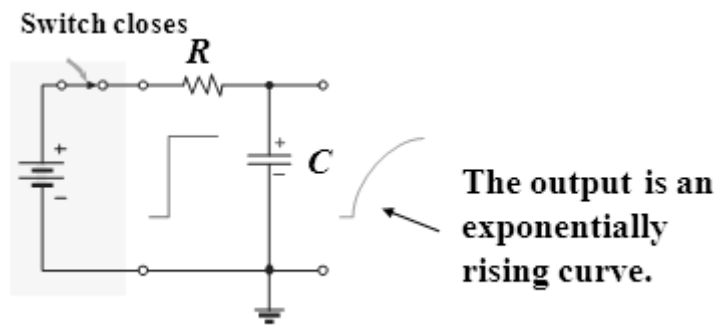
- When the pulse generator goes low, the small internal impedance of the generator makes it look like a closed switch has replaced the battery.
- The pulse generator now acts like a closed switch and the capacitor discharges


The output is an exponentially rising curve.
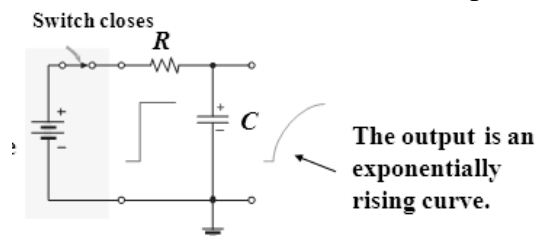
a) If t is increased, the waveforms approach the average dc level as in the last waveform. The output will appear triangular but with a smaller amplitude
b) Alternatively, the input frequency can be increased (T shorter). The waveforms will again approach the average dc level of the input.
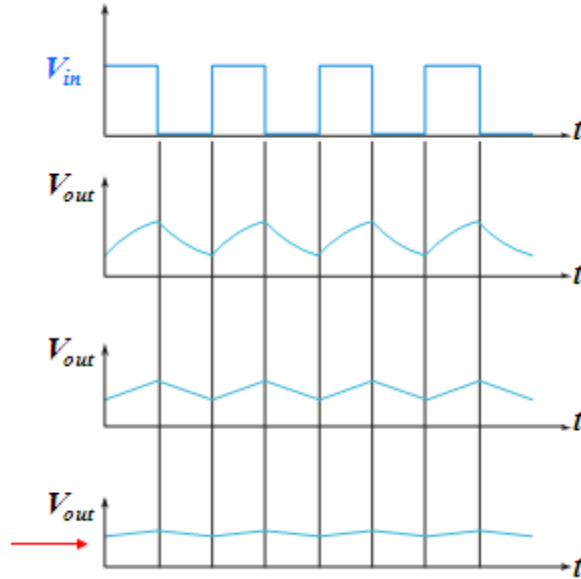
RC differentiator

- An *RC* differentiator is a circuit that approximates the mathematical process of differentiation. Differentiation is a process that finds the rate of change, and a basic differentiator can produce an output that is the rate of change of the input under certain conditions.
- A basic *RC* differentiator circuit is simply a resistor in series with a capacitor and the source. The output is taken across the resistor.
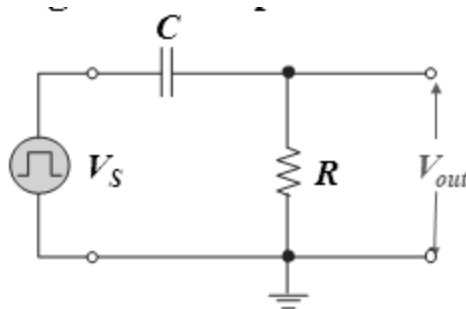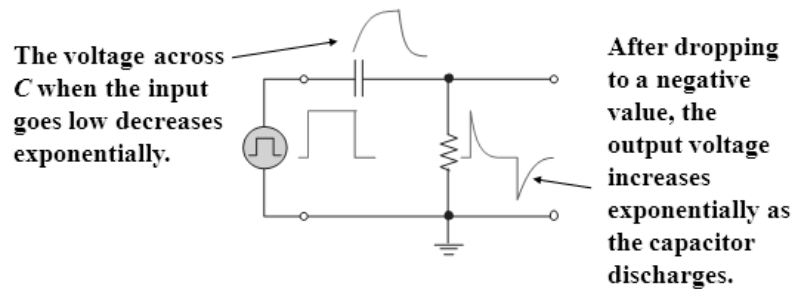

a) When a pulse generator is connected to the input of an *RC* differentiator, the capacitor appears as an instantaneous short to the rising edge and passes it to the resistor.

b) The capacitor looks like a short to the rising edge because voltage across *C* cannot change instantaneously

$V_C = 0$

During this first
instant, the
output follows
the input.
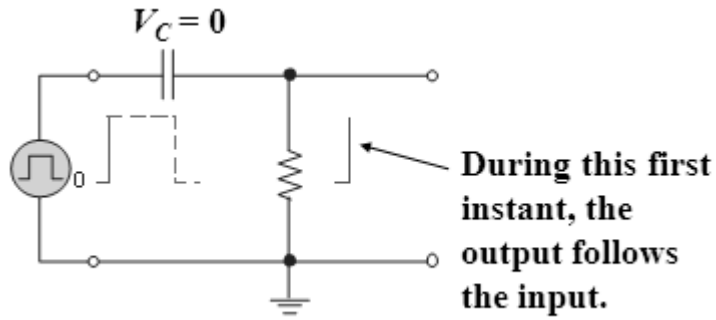
1. After the initial edge has passed, the capacitor charges and the output voltage decreases exponentially
2. The voltage across C is the traditional charging waveform.

The output
decreases as the
pulse levels off.
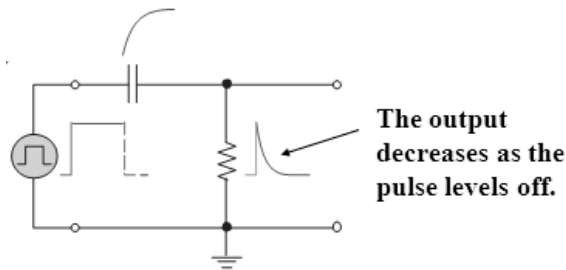
1. The falling edge is a rapid change, so it is passed to the output because the capacitor voltage cannot change instantaneously. The type of response shown happens when t is much less than the pulse width ($t << t_w$).

The voltage across
C when the input
goes low decreases
exponentially.

After dropping
to a negative
value, the
output voltage
increases
exponentially as
the capacitor
discharges.

2. The output shape is dependent on the ratio of t to t_w.
3. When $5t = t_w$, the pulse has just returned to the baseline when it repeats

V_{in} $\longleftarrow t_w \longrightarrow$

$5\tau = t_w$

$5\tau >> t_w$
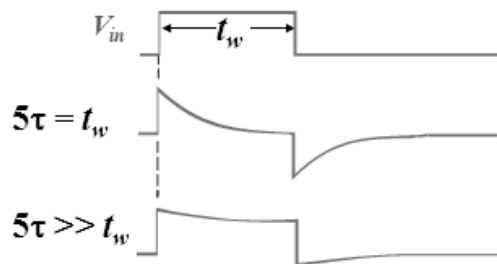
4. If t is long compared to the pulse width, the output does have time to return to the original baseline before the pulse ends. The resulting output looks like a pulse with "droop".

Clampers circuits

- The circuits which are used to add a d.c. level as per the requirements to the a.c output signalare called clamper circuits.
- The capacitor, diode and resistance are the three basic elements of a clamper crcuit. The clamper circuits are also called d.c restorer or d.c inserter circuits.
- Depending upon whether the positive d.c or negative d.c shift is introduced in the output waveform, the clampers are classified as,
c) Negative Clampers
d) Positive Clampers
e) Biased Clampers

The following assumptions are made while analysisng the clamper circuit;

3. The diode is ideal in behaviour.
4. The time constant RC is designed to be very large by selecting large values of R and C

Negative clamper:
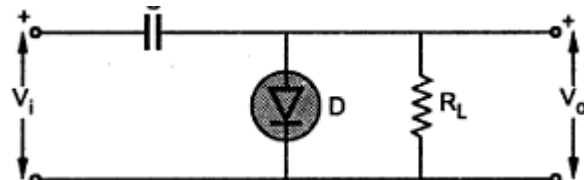
Operation:

- During the first quarter of positive cycle of the input voltage Vin the capacitor gets charged through forward biased diode D up to the maximum value Vm of the input signal Vi.
- The capacitor charging is almost instantaneous, which is possible by selecting proper values of C and RL in the circuit.
- The capacitor once charged to Vm, acts as a battery of voltage Vm as shown in the figure below:
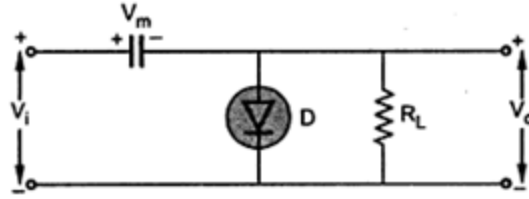
- Thus when D is ON, the output voltage Vo is zero. As input voltage decreases after attaining its maximum value Vm, the capacitor remains changed to Vm and the diode D becomes reverse biased.
- Due to large RC time constant the capacitor holds its entire charge and capacitor voltage remains as VC = Vm as shown in figure below.
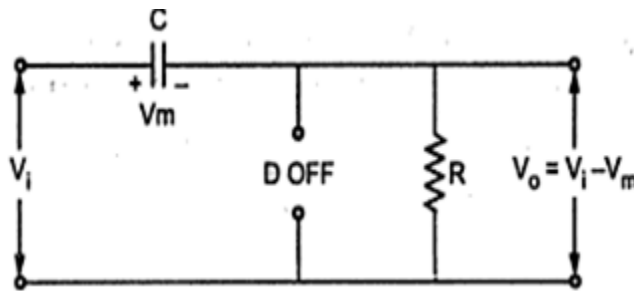
- And the output voltage Vo is given by, Vo = Vi-Vc= Vi-Vm
- In the negative half cycle of Vi, the diode will remains reverse biased. The capacitor starts discharging through the resistance Rl.
- As the time constant RC is vey large, it can be approximated that the capacitor holds all its charge and remains charges to Vm, during this period also. Hence we can write,

Vo = Vi – Vc= Vi-Vm

Vo = -Vm; for Vi = 0

Vo = 0; for Vi = Vm

Vo = -2Vm; for Vi = -Vm
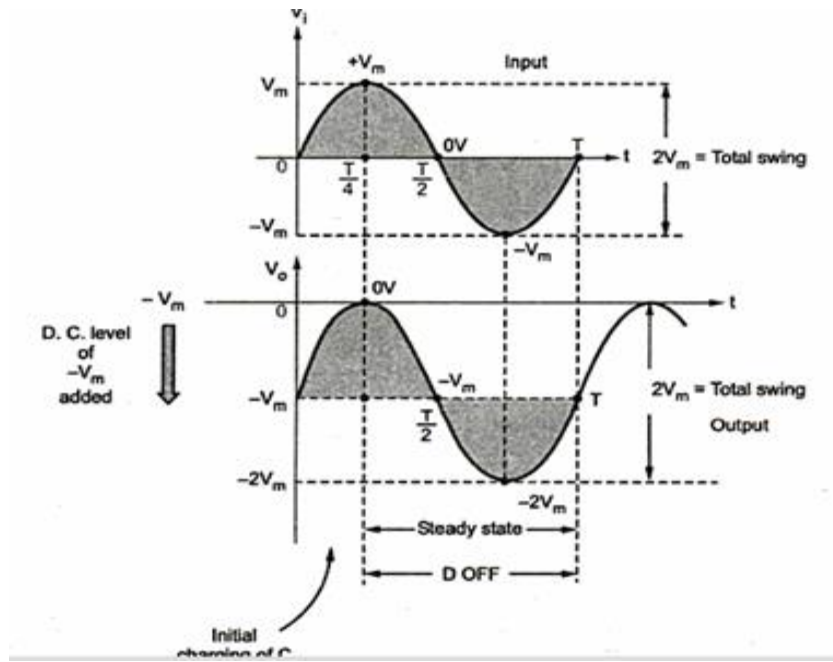
Positive Clamper

The circuit is shown below
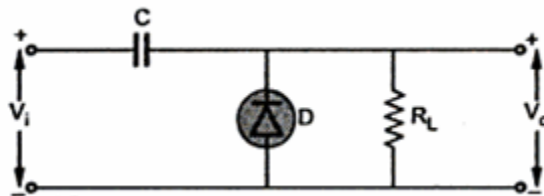
Operation

- During the first quarter of negative half cycle of the input voltage Vi, diode D gets forward biased and almost instantaneously capacitor gets charged equal to the maximum value Vm of the input signal Vi, with the polarities as shown in figure below
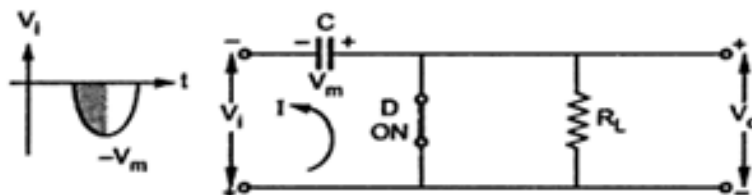
- The capacitor once charged to Vm, acts as a battery of voltage Vm with the polarities as shown in figure above. This is because RC time constant is very large hence capacitor holds its entire charge all the time.
- Thus when V=Vm, the output voltage Vo is 2Vm. Under steady conditions we can write, Vo = Vi + Vm
- In the positive half cycle, the diode D is reverse biased.
- The capacitor starts discharging through Rl. But due to large time constant, it hardly gets discharged during positive half cycle of Vi. This is shown in figure below:
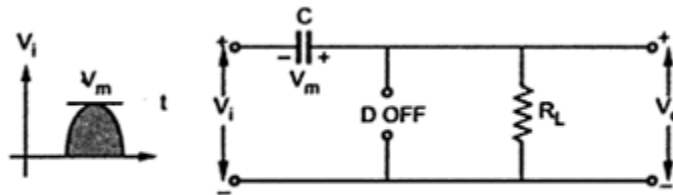
Hence **Vo = Vi + Vm**

Vo = Vm; for Vi = 0

Vo=2Vm; for Vi=Vm

Vo=0; for Vi=-Vm

<u>Biased clampers:</u>

(b)

INPUT WAVEFORM

OUTPUT WAVEFORM

(c)

INPUT WAVEFORM

OUTPUT WAVEFORM

(d)

INPUT WAVEFORM

OUTPUT WAVEFORM

(e)

INPUT WAVEFORM

OUTPUT WAVEFORM

(f)

INPUT WAVEFORM

OUTPUT WAVEFORM
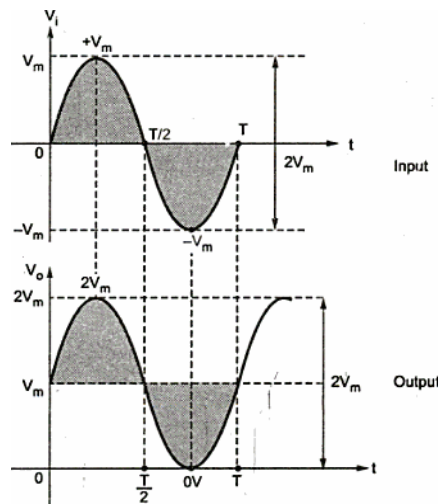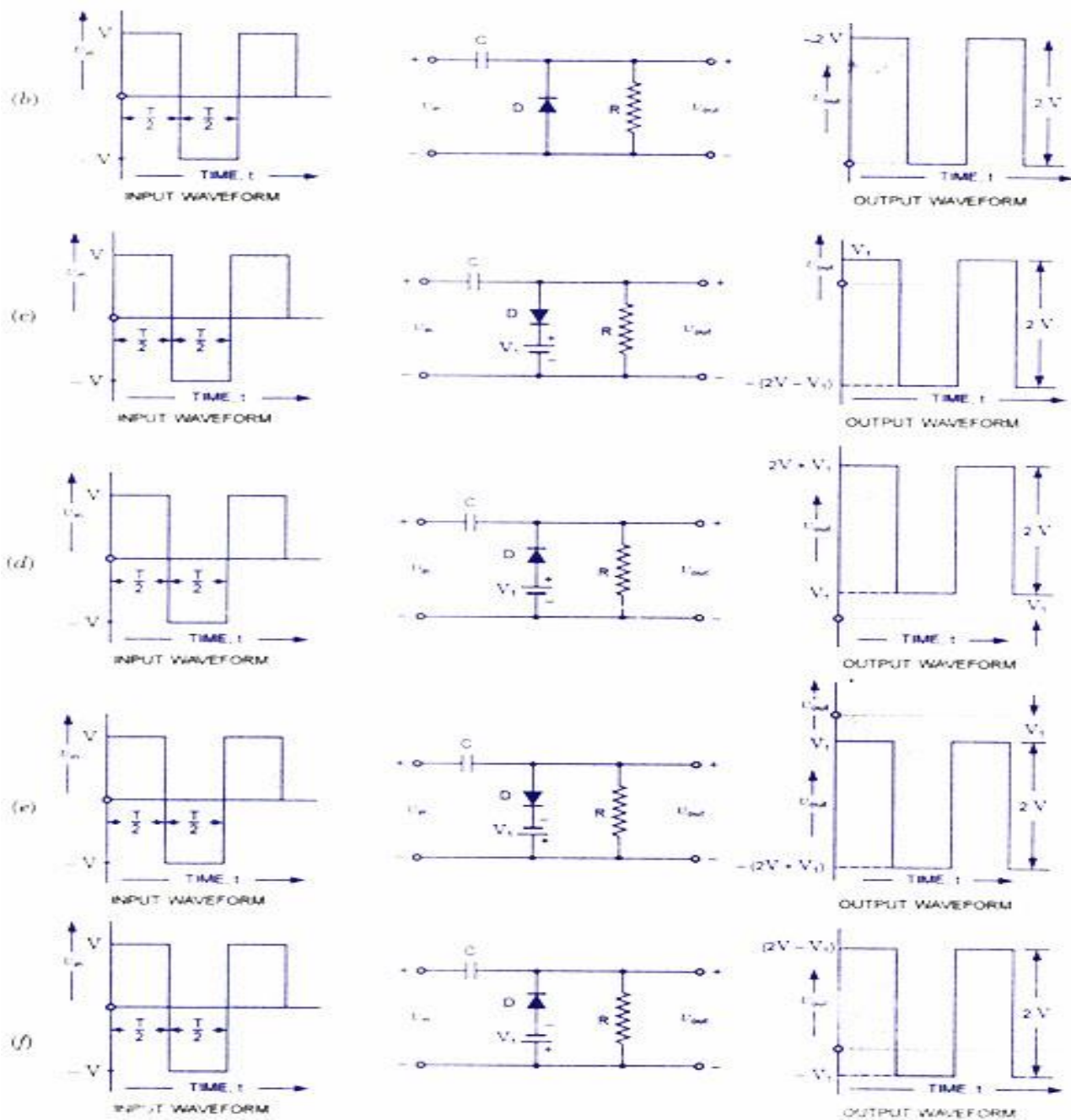
Clampers applications

As a "DC restorer" in "composite video" circuitry in both television transmitters and receivers.

- Clamping circuit are used to shift any part of the input signal waveform and can be maintained at a specified voltage level Such circuit are used in television receivers to restore the original d.c reference signal (corresponding to the brightness level of the picture) to the

video Signal The clamping of peak (i.e. 2Vm, 3Vm, 4Vm etc.,) Such to circuit are known as voltage multipliers These circuit are used to supply power to thigh voltage/low current devices like cathode ray tubes used in Television receivers, oscilloscopes and computer displays.

MULTIPLER

- In voltage multiplier circuit two or more peak rectifiers are cascaded to produce a d.c voltage equal to multiplier of the peak input voltages V_p i.e., $2V_p$, $3V_p$, $4V_p$.

HALF WAVE VOLTAGE DOUBLER

- A voltage multiplier, whose output d.c. voltage is double the peak a.c. input voltage, is called a voltage doubler below Figure shows the circuit, of a half-wave voltage doubler.

Full wave voltage doubler

- During the positive half-cycle of the input signal, the diode DI conducts and diode D_2 is cut off, charging the capacitor CI up to the peak rectified voltage i.e., V_m.
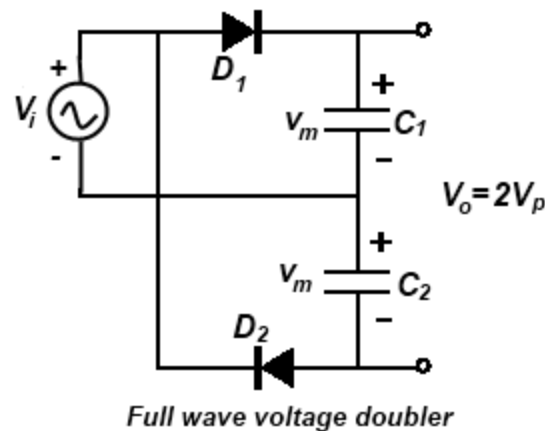- During the negative half-cycle, diode, D_1 is cut off and diode D_2 conducts charging capacitor C_2. It may be noted that during negative half cycle, the voltage across capacitor C_1 is in series with the input voltage.
- Therefore the total voltage presented to capacitor C_2 is equal to $2V_m$ during the negative half cycle.
- On the next positive half cycle, the diode D_2 is non-conducting and the capacitor will discharge through the load. If no load is connected across capacitor C_2, both capacitors stay charged at their full values (i.e., C_1 to V_m and C_2 to $2V_m$).

VOLTAGE TRIPLER

- During the first positive half cycle, the capacitor C_1 charges through diode D_1 to a peak voltage V_m. During negative half cycle, capacitor C_2 charges through diode D_2 to twice the

peak voltage $2V_m$ developed by the sum of the voltages across capacitor C_1 and the input signal.
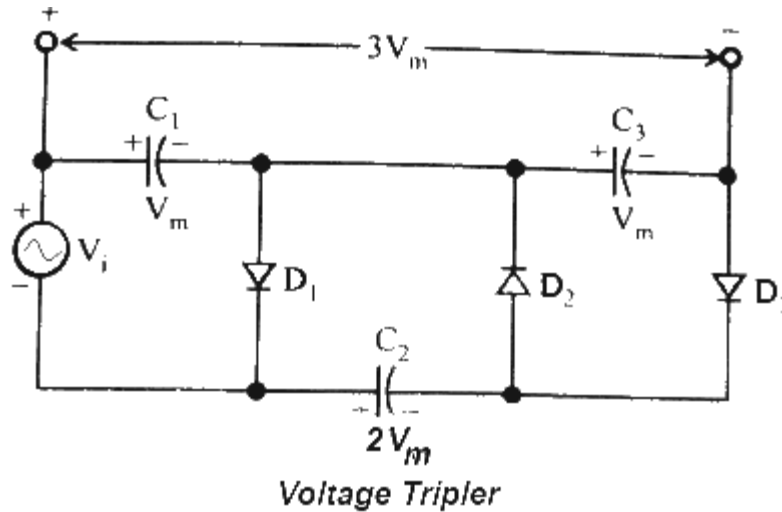
Voltage Tripler

- During the second positive half cycle, the diode D_2 conducts and the voltage across capacitor C_2 charges the capacitor C_3 to the same $2V_m$ peak voltage. The triple output taken across C_1 and C_3 connected in series, the output voltage is three times the input voltage.

VOLTAGE QUADRUPLER

- The addition of still another diode-capacitor section to the voltage Tripler produces an output four times the peak voltage. The circuit diagram is shown in below Figure.
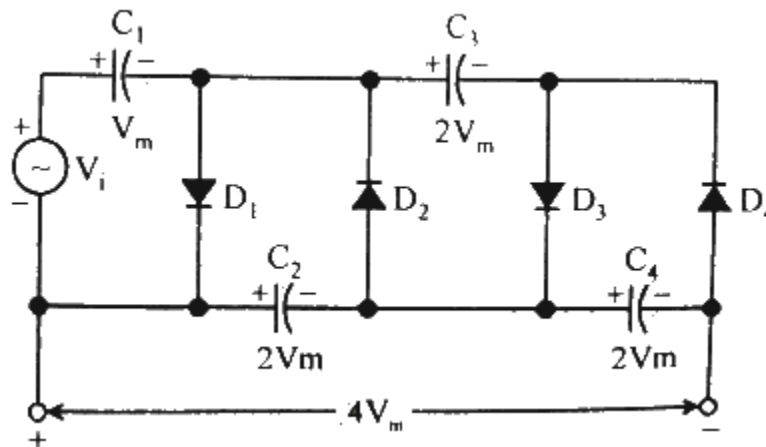
- In such type of circuit C_1 charges to V_m, through D_1, C_2 charges through D_2, C_3 and C_4 charges through D4, C_2, C_3 and C_4 charges to $2V_m$. The $4V_m$ output is taken across C_2 and C_4.

- The ripple frequency is twice the input frequency.

- Theoretically there is no upper limit to the amount of voltage multiplication that can be obtain. But practically there is a limit the reason is that total amount of capacitance becomes large to maintain the desired d.c. output except extremely light loads.

Application

- Voltage multipliers are used in high voltage, low current applications such as for accelerating purpose in a cathode ray tube. Generally these are used where both the supply voltage and load are maintained constant.

- **TIME BASE GENERATORS**
- A time-base generator is an electronic circuit which generates an output voltage or current waveform, a portion of which varies linearly with time. Ideally the output waveform should be a ramp.
- Time-base generators may be voltage time-base generators or current time-base generators. A voltage time-base generator is one that provides an output voltage waveform, a portion of which exhibits a linear variation with respect to time.
- A current time-base generators, such as in CRO, television and radar displays. To display the variation with respect to time of an arbitrary waveform on the screen of an oscilloscope it is required to apply to one set of deflecting plates a voltage which varies linearly with time.
- Since this waveform is used to sweep the electron beam horizontally across the screen it is called the sweep voltage and the time-base generators are called the sweep circuits.

GENERAL FEATURES OF A TIME-BASE SIGNAL

- Figure below shows the typical waveform of a time-base voltage. The time during which the output increases is called the sweep time and the time taken by the signal to return to its initial value is called restoration time, the return time or flyback time.

(a)   (b)
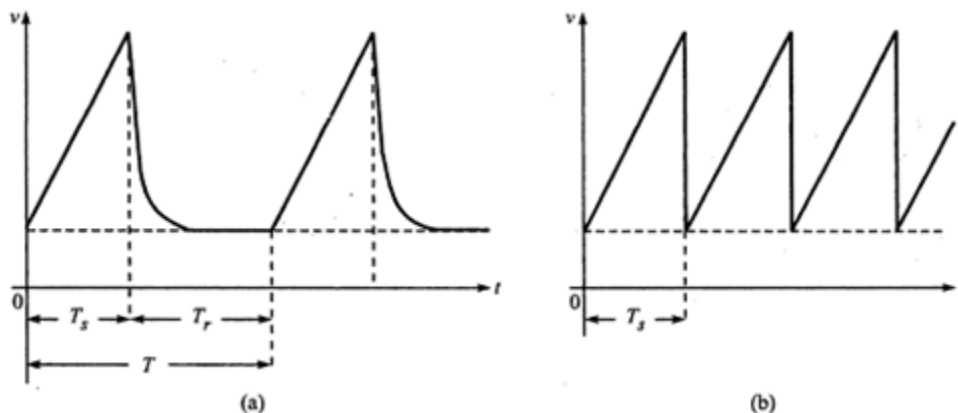
- The deviation from linearity is expressed in three most important ways:
  5. The slope or sweep spped error
  6. The displacement error,
  7. The transmission error

$$slope \lor sweep - speederror, es = \frac{difference \in slopeatbegiing \land endofsweep}{intialvalueofslope}$$

The transmission error, et

- When a ramp signal is transmitted through a high pass circuit, the output falls away from the input as shown in figure. This deviation is expressed as transmission error, et, defined as the difference between the input and the output divided by the input at the end of the sweep.

$$e_t = \frac{V_s{'} - V_s}{V_s{'}}$$

Where Vs' – input Vs- output
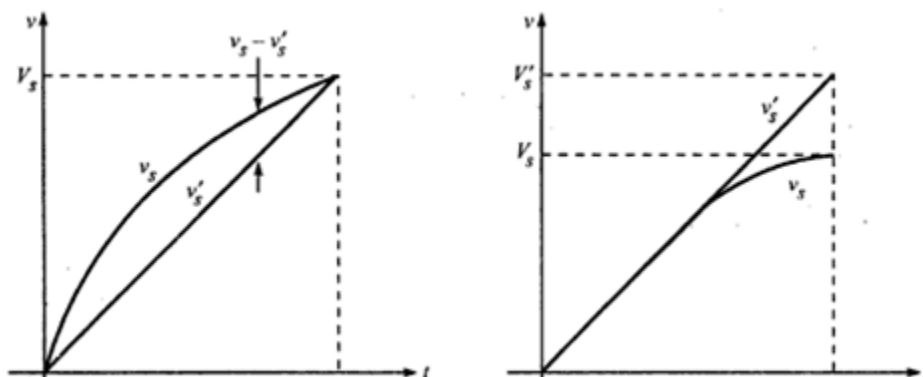
RAMP GENERATOR

- Voltage and current linear ramp generator find wide application in instrumentation and communication systems.
- Linear ramp generators are also known as sweep generators, from basic building blocks of cathode ray oscilloscope and analog to digital converters.
- Linear current ramp generators are extensively used in television deflection systems. This topic considers the circuits employed in the generation of voltage and current sweeps.

Ramp Generation Methods

Although there are a number of methods of ramp generation, yet the following are important from the topic point of view.

Exponential Charging

In this method a capacitor is charged through a resistor to a voltage which is small in comparison with the supply voltage.

Constant Current Charging

In this method a capacitor is charged linearly from a constraint current source.

Miller Integration

In this method a constant current is approximated by maintaining nearly constant voltage across a fixed resistor in series with a capacitor.

RC Ramp Generator

- Figure 1 shows the basic circuit of RC ramp generator. This circuit requires a gating waveform V_i as shown in Figure 1(b).
- It may be obtained from a Monostable multivibrator (i.e. one shot) or an Astable multivibrator.
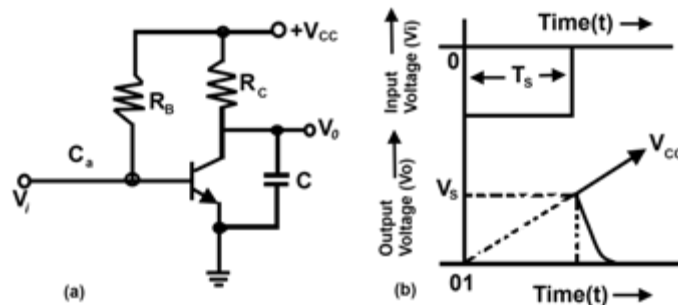
Figure 1: (a) RC Ramp Generator (b) Input and Output Waveforms

- Initially the transistor is biased ON and operates in the saturation region. Thus when there is no input (i.e. $V_i = 0$), the output voltage is zero. Actually its value is equal to V_{CE} (sat).
- When gating pulse i.e. a negative pulse is applied the transistor turns OFF. As a result of this, the capacitor voltage rises to a target value V_{CC} with a time constant $R_C C$. The charging curve ignoring V_{CE} (sat) is given by the relation.

$$V_o(t) = V_{CC}\left(1 - e^{\frac{-1}{RC}}\right)$$

- If $t / R_C C \ll 1$, then above relation may be expanded into a power series in $t / R_C C$. Then taking only the first term of the power series, the output voltage.

$$V_o(t) = V_{CC} \frac{1}{R_C C}$$

At t = T$_S$ the output voltage

$$V_o(t) = V_{CC} \frac{T_S}{R_C C} V_S$$

- It may be observed that the transistor switch is OFF only for the gating time (T$_S$). At the end of time T$_S$, the capacitor discharges and the voltage is again zero.

Constant Current Ramp Generator
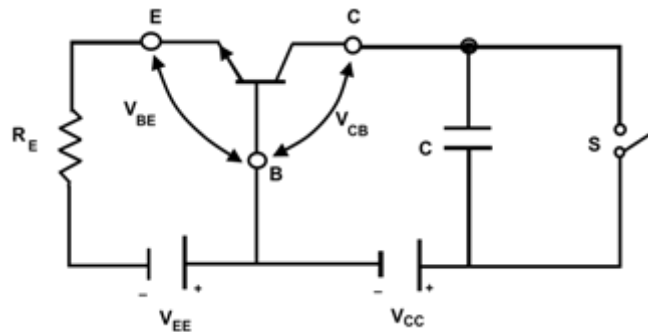
Figure 2: Constant Current Ramp Generator

- Figure 2 shows a circuit to generate a ramp using constant current from a common base transistor. We know that except for very small value of collector to base voltage, the collector current of a transistor in the common base configuration is very nearly constant, when the emitter current is held fixed.
- This characteristic may be used to generate a quite linear ramp by causing a constant current to flow into a capacitor. The value of emitter current is given by the relation.

$$I_E = (V_{EE} - V_{EB}) / R_E$$

- If the emitter to base voltage V$_{EB}$ remains constant with time after the switch S is opened, then the collector current will be a constant whose normal value,

- $I_C = h_{fb}. I_B = \alpha I_E$

- The drawback of constant current ramp circuit is that it makes the sweep rate as a function of temperature. Since the emitter base junction voltage V$_{BE}$ for fixed current decreases by about 2 mv/c^o, therefore the ramp speed increases with the temperature.

UJT Relaxation Oscillator

- The UJT relaxation as a relaxation oscillator is shown in Figure 3 generates a voltage waveform V_{B1}(Figure 3), which can be applied as a triggering pulse to an SCR gate to turn on the SCR.

- When switch S is first closed, applying power to the circuit, capacitor C starts charging exponentially through R to the applied voltage V. The voltage across it's the voltage V_E applied to the emitter of UJT.

- When C has charged to the peak point voltage V_P of the UJT, the UJT is turned on, decreasing greatly the effective resistance R_{B1} between the emitter and base1. A sharp pulse of current I_E (limited only be R_1) flows from base 1 into the emitter, discharging C.

- When the voltage across C has dropped to approximately 2V, the UJT turns off and the cycle is repeated.
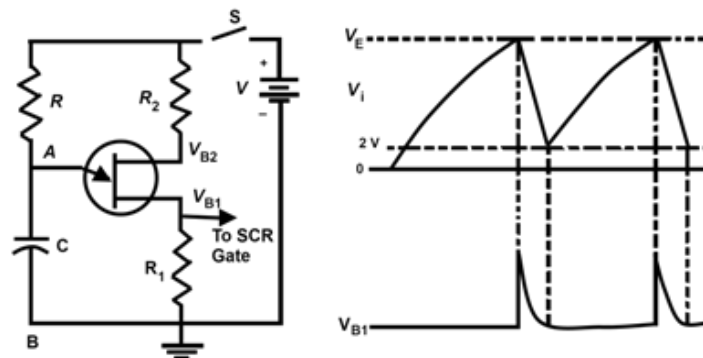
Figure 3: UJT Relaxation Oscillator

- The waveforms in figure 3 shows the saw-tooth voltage V_E, generated by the charging of C and the output pulse V_{B1} developed across R_1, V_{B1} is the pulse which will be applied to the gate of an SCR to trigger the SCR.

- The frequency f of the relaxation oscillator depends on the time constant RC and the characteristics of the UJT. For values of $R_1 < 100K\Omega$, the period of oscillation T is given approximately by the equation.

  - $T = 1 / f = R_T C_T 1\eta \ (1 / 1 - \eta)$

- The value of R is limited to the range 3000Ω to $3M\Omega$. The supply voltage V normally used lies in the range of 10 to 35 V and etc η is called intrinsic standoff ratio of injunction transistor (i.e. ratio of R_{B1} and R_{BB}).

Bootstrap Ramp Generator
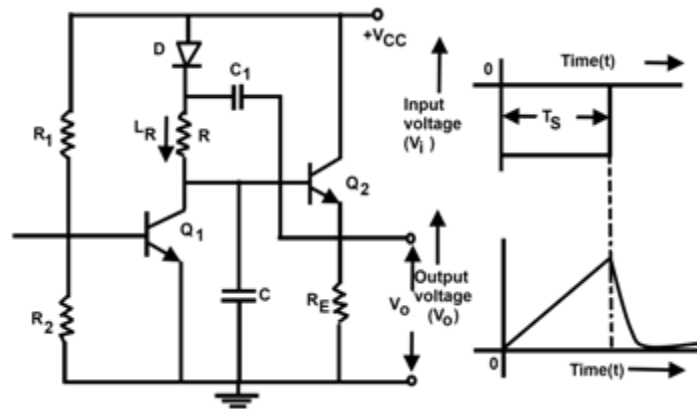
Figure 4: Bootstrap Ramp Generator

- Figure 4 shows the bootstrap ramp generator. In such case the transistor Q_1 acts as a switch and Q_2 as an emitter follower i.e. a unity gain amplifier.

- Suppose the transistor Q_1 is ON and Q_2 is OFF. Therefore the capacitor C_1 is charged to V_{CC} through the diode forward resistance R_E. At this instant, the output voltage V_o is zero.

- When negative pulse as shown in Figure 4 is applied to the base of transistor Q_2 it turns OFF. Since transistor Q_2 is an emitter follower, therefore the output voltage (V_o) is the same as the base voltage of transistor Q_2.

- Thus as the transistor Q_1 turns OFF, the capacitor C_1 starts charging this capacitor C through resistor R. As a result of this, both the base voltage of Q_2 and the output voltage begin to increase from zero.

- As the output voltage increases, the diode D becomes reverses biased. It is because of the fact that the output voltage is coupled through the capacitor C_1 to the diode. Since the value of capacitor C_1 is much larger than that of capacitor C, therefore the voltage across capacitor C_1 practically remains constant.

- Thus the voltage drop across the resistor R also remains constant because of this; the current i_R through the resistor also remains constant. This causes the voltage across the capacitor C (and hence the output voltage) to increase linearly with time.

Miller Integrator Ramp Generator
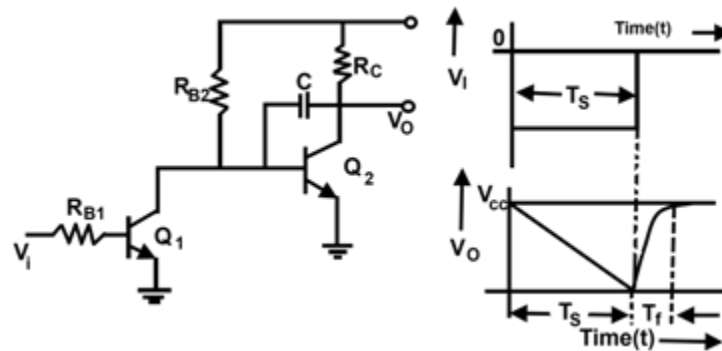
Figure 5: Miller Integrator Ramp Generator

- Figure 5 shows the miller integration ramp generator. It is also called Miller integrator. In such a case transistor Q_1 acts as a switch and transistor Q_2 is a common emitter amplifier i.e. a high gain amplifier.

- Suppose that initially, the transistor Q_1 is ON and Q_2 is OFF. At this instant, the voltage across the capacitor and the output voltage are equal to V_{CC}.

- Let us suppose that a pulse of negative polarity as shown in Figure 5(b) is applied at the base of the transistor Q_1. As a result of this, the emitter-base junction of the transistor Q_1 is reverse biased and it turns OFF. This causes the transistor Q_2 to turn ON.

- As the transistor Q_2 conducts, the output voltage begins to decrease towards zero. Since the capacitor C is coupled to the base of transistor Q_2 therefore the rate of decrease of the output voltage is controlled by the rate of discharge of capacitor C.

- The time constant of the discharge is R_BC.

- As the value of time constant is very large, therefore the discharge current remains constant. Hence a result of this, the rundown of the collector voltage is linear.

- When the input pulse is removed the transistor Q1 turns ON and Q_2 turns OFF. It will be interesting to know that as the transistor Q_1 turns OFF, the capacitor C charges quickly through resistor R_C to V_{CC} with the time constant equal to R_CC.

- The waveform of the generated ramp or the output voltage is shown in Figure 5(b). The Miller integrators provide excellent ramp linearity as compared to the other ramp circuits.

Triangular Wave Generator

- Triangular wave is a periodic, non-sinusoidal waveform with a triangular shape. People often get confused between triangle and sawtooth waves.
- The most important feature of a triangular wave is that it has equal rise and fall times while a sawtooth wave has un-equal rise and fall times. The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc.
- There are many methods for generating triangular waves but here we focus on method using opamps. This circuit is based on the fact that a square wave on integration gives a triangular wave.
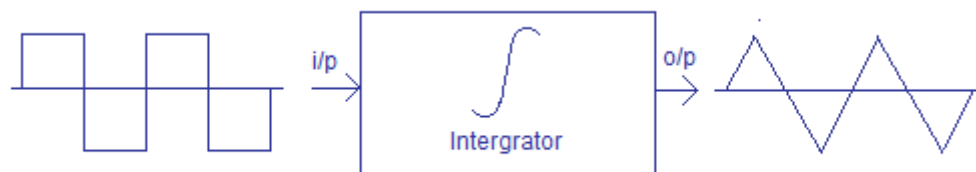
Generating triangular wave from a square wave

- The circuit uses an opamp based square wave generator for producing the square wave and an opamp based integrator for integrating the square wave.
- The circuit diagram is shown in the figure below.
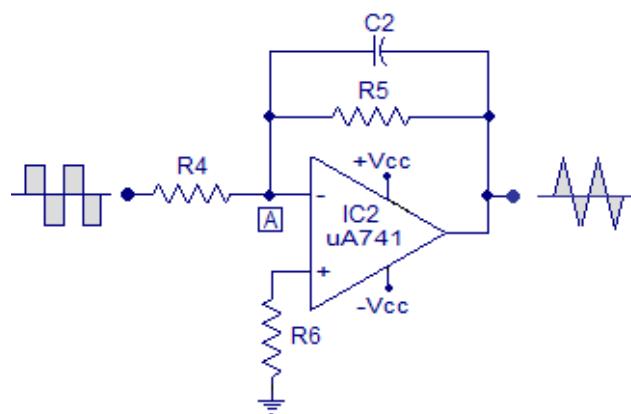
- Let's assume the positive side of the square wave is first applied to the integrator. By virtue capacitor C2 offers very low resistance to this sudden shoot in the input and C2 behaves something like a short circuit.
- The feedback resistor R5 connected in parallel to C2 can be put aside because R5 has almost zero resistance at the moment. A serious amount of current flows through the input resistor R4 and the capacitor C2 bypasses all these current. As a result the inverting input terminal

(tagged A) of the op-amp behaves like a virtual ground because all the current flowing into it is drained by the capacitor C2.

- The gain of the entire circuit (Xc2/R4) will be very low and the entire voltage gain of the circuit will be close the zero.
- After this initial "kick" the capacitor starts charging and it creates an opposition to the input current flowing through the input resistor R4.
- The negative feedback compels the op-amp to produce a voltage at its out so that it maintains the virtual ground at the inverting input. Since the capacitor is charging its impedance Xc keeps increasing and the gain Xc2/R4 also keeps increasing.
- This results in a ramp at the output of the op-amp that increases in a rate proportional to the RC time constant (T=R4C2) and this ramp increases in amplitude until the capacitor is fully charged.
- When the input to the integrator (square wave) falls to the negative peak the capacitor quickly discharges through the input resistor R4 and starts charging in the opposite polarity.
- Now the conditions are reversed and the output of the op-amp will be a ramp that is going to the negative side at a rate proportional to the R4R2 time constant.
- This cycle is repeated and the result will be a triangular waveform at the output of the op-amp integrator.

Pulse Generator

- A device that produces an electrical discharge at regular intervals, which can be modified as needed, as in an electronic pacemaker.
- A pulse differs from a square wave in that it needs neither base line, nor left-right symmetry. Pulse generator consists of three parts called square wave generator (i.e. stable multivibrator). Monostable Multivibrator (i.e. one shot) and a attenuator.

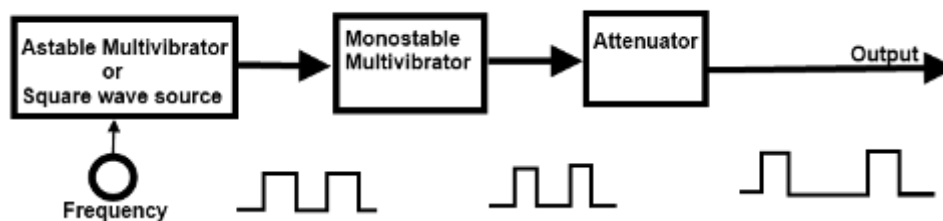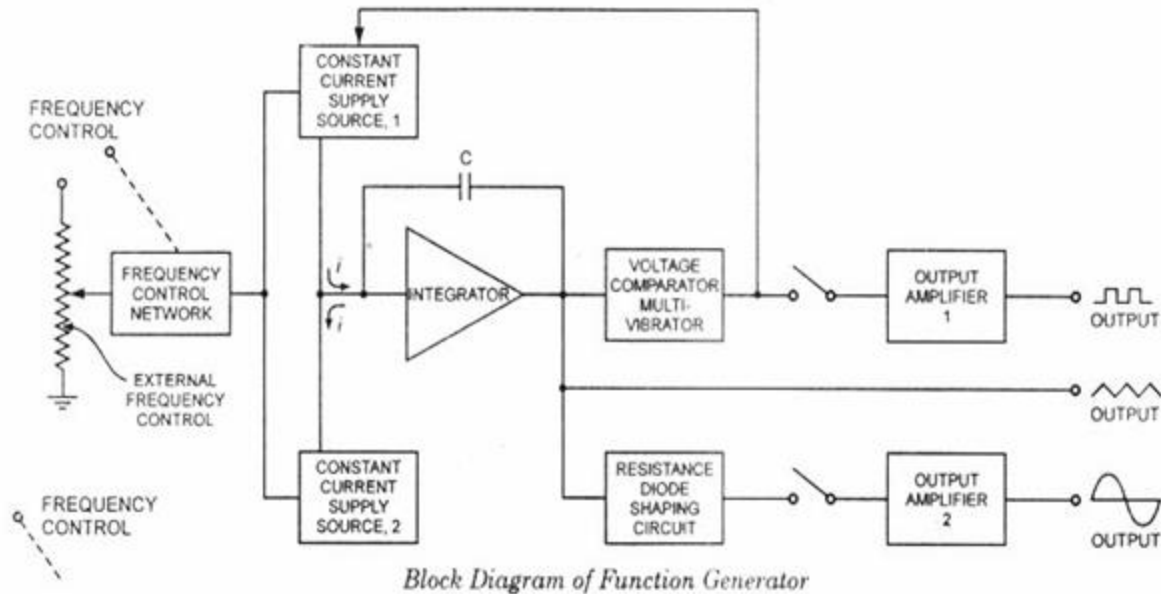
Figure 1: Pulse Generator Block Diagram

- Figure 1 shows the block diagram to contract a pulse generator.
- A Monostable multivibrator i.e. one shot follows a square wave oscillator. The pulse repetition rate is set by the square wave frequency.

- The one shot triggers on the leading edge of the square wave and produced me output pulse for each input cycle.
- The duration of each output pulse is set by the one time of the one shot, and may be either very short or may approach the period of the square wave.

Function Generators
- A function generator is a signal source that has the capability of producing different types of waveforms as its output signal.
- The most common output waveforms are sine-waves, triangular waves, square waves, and saw tooth waves. The frequencies of such waveforms may be adjusted from a fraction of a hertz to several hundred kHz.
- Actually the function generators are very versatile instruments as they are capable of producing a wide variety of waveforms and frequencies.
- The triangular-wave and saw tooth wave outputs of function generators are commonly used for those applications which need a signal that increases (or reduces) at a specific linear rate. They are also used in driving sweep oscillators in oscilloscopes and the X-axis of X-Y recorders.
- Many function generators are also capable of generating two different waveforms simultaneously (from different output terminals, of course). This can be a useful feature when two generated signals are required for particular application. For instance, by providing a square wave for linearity measurements in an audio-system, a simultaneous sawtooth output may be used to drive the horizontal deflection amplifier of an oscilloscope, providing a visual display of the measurement result.
- For another example, a triangular-wave and a sine-wave of equal frequencies can be produced simultaneously. If the zero crossings of both the waves are made to occur at the same time, a linearly varying waveform is available which can be started at the point of zero phase of a sine-wave.
- Another important feature of some function generators is their capability of phase-locking to an external signal source. One function generator may be used to phase lock a second function generator and the two output signals can be displaced in phase by an adjustable amount. In addition, one function generator may be phase locked to a harmonic of the sine-wave of another function generator.
- By adjustment of the phase and the amplitude of the harmonics, almost any waveform may be produced by the summation of the fundamental frequency generated by one function generator and the harmonic generated by the other function generator.
-
- The function generator can also be phase locked to an accurate frequency standard, and all its output waveforms will have the same frequency, stability, and accuracy as the standard.

Block Diagram of Function Generator

- The block diagram of a function generator is given in figure. In this instrument the frequency is controlled by varying the magnitude of current that drives the integrator. This instrument provides different types of waveforms (such as sinusoidal, triangular and square waves) as its output signal with a frequency range of 0.01 Hz to 100 kHz.
- The frequency controlled voltage regulates two current supply sources. Current supply source 1 supplies constant current to the integrator whose output voltage rises linearly with time. An increase or decrease in the current increases or reduces the slope of the output voltage and thus controls the frequency.
- The voltage comparator multivibrator changes state at a predetermined maximum level, of the integrator output voltage. This change cuts-off the current supply from supply source 1 and switches to the supply source 2.
- The current supply source 2 supplies a reverse current to the integrator so that its output drops linearly with time. When the output attains a predetermined level, the voltage comparator again changes state and switches on to the current supply source.
- The output of the integrator is a triangular wave whose frequency depends on the current supplied by the constant current supply sources.
- The comparator output provides a square wave of the same frequency as output. The resistance diode network changes the slope of the triangular wave as its amplitude changes and produces a sinusoidal wave with less than 1% distortion.

# UNIT– V

Large Signal Amplifiers: Classification of power amplifiers - Class A power amplifier-direct and transformer coupled amplifiers; - Class B - Push-pull arrangements and complementary symmetry amplifiers; conversion efficiency calculations, cross over distortion – class AB amplifier - amplifier distortion – power transistor heat sinking – Class C and D amplifiers.

CONCEPT

Generally, amplifiers can be sub-divided into two distinct types depending upon their power or voltage gain. One type is called the Small Signal Amplifier which include pre-amplifiers, instrumentation amplifiers etc. Small signal amplifies are designed to amplify very small signal voltage levels of only a few micro-volts (µV) from sensors or audio signals.

The other types are called Large Signal Amplifiers such as audio power amplifiers or power switching amplifiers. Large signal amplifiers are designed to amplify large input voltage signals or switch heavy load currents as you would find driving loudspeakers.
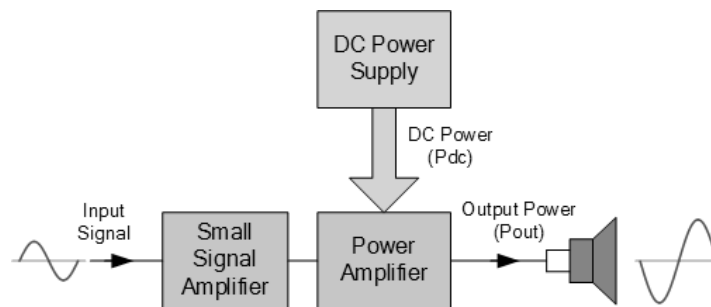
LARGE SIGNAL AND POWER AMPLIFIER APPLICATIONS

1. Public address system
2. Radio receivers
3. Driving servomotors in industrial control systems
4. Tape players
5. T.V receivers
6. CRT etc

FEATURES OF LARGE SIGNAL AMPLIFIERS

- The main features of a large-signal amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

- The h-parameter analysis is applicable to the small signal amplifiers and hence cannot be used for the analysis of power amplifier. The analysis of power amplifier carried by drawing a load line on the output characteristics of the transistors used in it.
- Power amplifier, large signals are fed to the loads (loudspeaker) having low impedance. Hence power amplifier must have low impedance. Hence common collector or emitter follower circuit is very common in power amplifier. The common emitter circuit with a step down transformer for impedance matching is also commonly used in power amplifiers.
- Power amplifier develops an a.c power of the order of few watts. Similarly large power gets dissipated in the form of heat, at the junctions of the transistors used in the power amplifiers. Hence, the transistors used in power amplifier are of large size, having large power dissipation rating called power transistors. Such transistors have heat sinks.

  Heat sink: it is a metal cap having bigger surface area, press fit on the body of a transistor to get more surface area, in order to dissipate the heat to the surroundings. In general, the power amplifiers have bulky components.
- A faithful reproduction of signal, after the conversion, is important. Due to non linear nature of the transistor characteristics, there exists a harmonics distortion in the signal. Ideally signal should not be distorted. Hence, the analysis of signal distortion in the case of the power amplifiers is important.
- Many times, the power amplifiers are used in PAS (public address system) and may audio circuits to supply large power to the loud speaker. Hence power amplifiers are also called audio amplifiers or audio frequency power amplifiers.

DIFFERENCE BETWEEN VOLTAGE AMPLIFIER AND POWER AMPLIFIER

Voltage

- A power amplifier may cause a slight decrease in signal voltage, but it usually holds signal voltage relatively constant.

- A voltage amplifier significantly increases the amount of signal voltage.

Current

- A power amplifier significantly increases signal current, while a voltage amplifier will cause a slight increase in the amount of signal current.

Resistance

- A power amplifier causes a significant decrease in circuit output résistance. A voltage amplifier maintains a high resistance circuit. In a voltage amplifier, circuit resistance may vary slightly, either up or down.

Power

- A power amplifier significantly increases signal power. A voltage amplifier may cause a slight increase in the amount of signal power.

TYPES OF POWER AMPLIFIER CLASSES

| Class	A	B	C	AB
Conduction Angle	360°	180°	Less than 90°	180 to 360°
Position of the Q-point	Centre Point of the Load Line	Exactly on the X-axis	Below the X-axis	In between the X-axis and the Centre Load Line
Overall Efficiency	Poor 25 to 30%	Better 70 to 80%	Higher than 80%	Better than A but less than B 50 to 70%
Signal Distortion	None if Correctly Biased	At the X-axis Crossover Point	Large Amounts	Small Amounts

CLASS A AMPLIFIER

There are 2 types. i. Series fed or directly coupled class A amplifier

ii. Transformer coupled class A amplifier

In directly coupled type, the load is directly connected in the collector circuit. While in the transformer coupled type, the load is coupled to the collector using a transformer called an output transformer

I. SERIES FED OR DIRECTLY COUPLED CLASS A AMPLIFIER
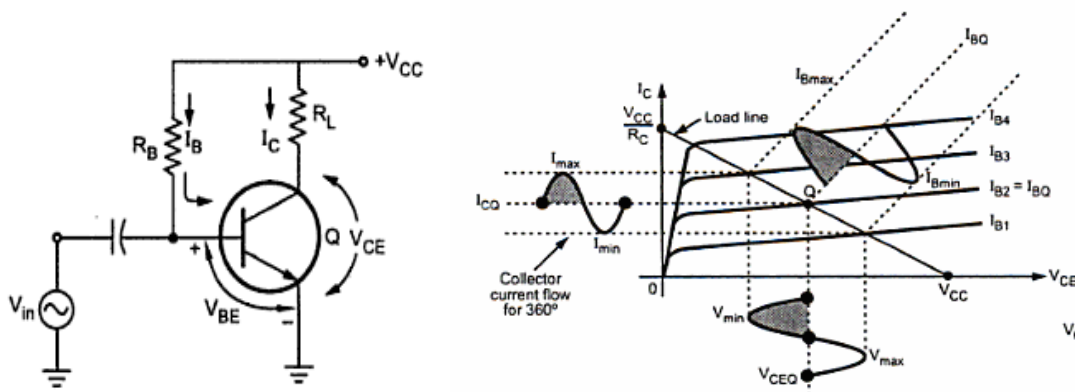
D.C.Operation

The collector supply voltage Vcc and resistance R_B decides the DC base-bias current I_{BQ}. The expression is obtained applying KVL to the b-e loop and with $V_{BE}= 0.7$ V

$$I_{BQ} = \frac{V_{CC} - 0.7}{R_B}$$

The corresponding collector current is then,

$$I_{CQ} = \beta\, I_{BQ}$$

From the equation below, the corresponding collector to emitter voltage is,

$$V_{CEQ} = V_{CC} - I_{CQ}R_L$$

Hence the Q point can be defined as $Q(V_{CEQ}, I_{CQ})$.

D.C. Power Input

- The d.c power input is provided by the supply. With no a.c. input signal, the d.c. current drawn is the collector bias current I_{CQ}. Hence d.c power input is,

$$P_{DC} = V_{CC}I_{CQ}$$

- It is important to note that even if a.c input signal is applied, the average current drawn from the d.c supply remains same. Hence the above equation represents d.c power input to the class A series fed amplifier.

A.C. Operation

- When an input a.c signal is applied, the base current varies sinusoidaly.
- Assuming that the nonlinear distortion is absent, the nature of the collector current and collector to emitter voltage also vary sinusoidally as shown graphically in the figure.
- The output current i.e. collector current varies around its quiescent value while the output voltage i.e collector current varies around its quiescent value.
- The varying output voltage and output current deliver an a.c. power to the load. Let us find the expressions for the a.c. power delivered to the load.

A.C. Power Output

- For an alternating output voltage and output current swings, shown n figure. We can write,

V_{min} = Minimum instantaneous value of the collector (output) voltage

V_{max} = Maximum instantaneous value of the collector (output) voltage

And V_{pp} = Peak to Peak value of a.c. output voltage across the load.

$$V_{PP} = V_{max} - V_{min}$$

- Now V_m = Amplitude (peak) of a.c. output voltage as shown in the figure.

$$V_m = \frac{V_{pp}}{2} = \frac{V_{max} - V_{min}}{2}$$

- Similarly we can write for the output current as,

I_{min} = Minimum instantaneous value of the collector (output) current

I_{max} = Maximum instantaneous value of the collector (output) current

and I_{pp} = Peak to Peak value of a.c. output current across the load.

$$I_{PP} = I_{max} - I_{min}$$

- Now I_m = Amplitude (peak) of a.c. output current as shown in the figure.

$$I_m = \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2}$$

- Hence the rms value of the alternating output voltage and current can be obtained as

$$V_{rms} = \frac{V_m}{2}$$

$$I_{rms} = \frac{I_m}{2}$$

- The a.c power delivered by the amplfier to the load can be expressed by using r.m.s values, maximum i.e. peak values and peak to peak values of output voltage and current.
- **Using r.m.s values**

$$P_{ac} = V_{rms}I_{rms}$$

- **Using peak values**

$$P_{ac} = V_{rms}I_{rms} = \frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}$$

- **Using peak to peak values**

$$P_{ac} = \frac{V_m I_m}{2} = \frac{\frac{V_{pp}}{2}\frac{I_{pp}}{2}}{2}$$

But as Vpp = (Vmax – Vmin) and Ipp = Imax – Imin; The a.c power can be expressed as below.

$$P_{ac} = \frac{(Vmax - Vmin)(Imax - Imin)}{8}$$

Efficeiency

- The efficiencyof an amplifier represents the amount of a,c power delivered or transferred to the load, from thed.c source i.e accepting the d.c. power input.
- The generalisedexpression for an efficiency of an amplifier is,

$$\%\eta = \frac{P_{ac}}{P_{dc}} \times 100$$

- Now for class A operation, we have deived theexpresion for Pac and Pdc, hence we ca write as,

$$\%\eta = \frac{(Vmax - Vmin)(Imax - Imin)}{8V_{cc}I_{CQ}}$$

Maximum Efficiency:

- For maximumefficiency calculation, assume maximum swings of both the output voltage and the output current.
- The maximum is an ideal value. For a practical circuit, it is much less than 25%, of the order of 10 to 15%

Power Dissipation:

- Power disipation in large signal amplifier is also large.
- The amount of power that must be dissipated by the transistor is the difference between the d.c power input Pdc and the a.c power delivered to the load Pac

$$P_D = P_{dc} - P_{ac}$$

- The maximum power dissipation occurs when there is zero a.c input signal.
- When a.c. input is zero, the a.c power output is also zero. But transistor operates at quiescent condition, drawing d.c input power from the supply equal to Vcc Ic$_Q$.
- This entire power gets dssipated in the form of heat. Thus d.c power input without a,c input signal is the maximum power dissipation.

$$(P_D)\,max = VccI_{CQ}$$

Advantages & Disadvantages:

The advantages of directly coupled class A amplifier are
- The circuit is simple to design and to implement
- The load is connected directly in the collector circuit hence the output transformer is not necessary. This makes the circuit cheaper.

The disadvantages are:

- The load resistance is directly connected in collector and carries the quiescent collector current. This causes considerable wastage of power.
- Power dissipation is more. Hence power dissipation arrangements like heat sink are essential.
- The output impedances is high hence circuit cannot be used for low impedance loads, such as loudspeakers.
- The efficiency is very poor, due to large power dissipation.

II) TRANSFORMER COUPLED CLASS A AMPLIFIER

- For maximum power transfer to the load, the impedance matching is necessary.
- For loads like loudspeaker, having low impedance values, impedance matching is difficult using directly coupled amplifier circuit. This is because loudspeaker resistance is in the range of 3 to 4 ohms to 16 ohms while the output impedance of series fed directly coupled class A amplifier is very much high.
- This problem can be eliminated by using transformer to deliver power to the load.
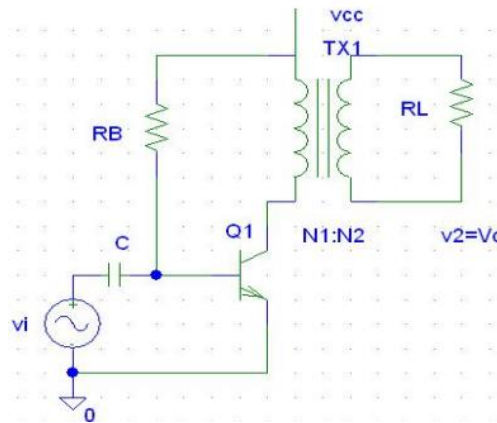
Let   N1 – number of turns in primary

N2 – number of turns in secondary

V1 – voltage applied to primary

V2 – voltage on secondary

I2 – Primary current
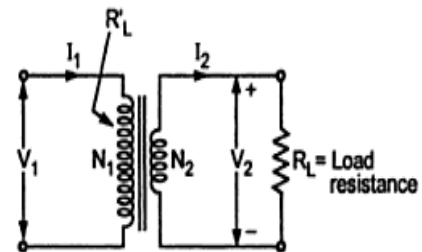
Turns Ratio:

- The ratio of number of turns on secondary to the number of turns on primary is called turns ratio of the transformer denoted by n.

$$n = Turns\ Ratio = \frac{N2}{N1}$$

Sometimes it is specified as $\frac{N2}{N1}:1\ or\ \frac{N1}{N2}:1$

Voltage Transformation: The transformer transforms the voltage applied on one side to other side proportional to the turns ratio. The transformer can be set up or step down transformer.

$$\frac{V2}{V1} = \frac{N2}{N1} = n$$

Current transformation: The current in the secondary winding is inversely proportional to the number of turns of the windings.

$$\frac{I2}{I1} = \frac{N1}{N1} = \frac{1}{n}$$

- Impedance Transformation: as current and voltage get transformed from primary to secondary, an impedance changes.

Now the impedance of the load on secondary is R_L . The primary and secondary winding resistances are assumed to be zero. This load impedance $R_{L'}$ gets reflected on the primary side and behaves as if connected n the primary side Such impedance transferred from secondary to primary is denoted as R_L'.

$$Now,\ R_L' = \frac{R_L}{n^2} = \left(\frac{N1}{N2}\right)^2 R_L$$

D.C. Operation

- It is assumed that the winding resistances are zero. Hence for d.c. purposes, the resistance is 0 ohm. There is no d.c. voltage drop across the primary winding of the transformer.
- The slope of the d.c load line s reciprocal od the d.c resistance in the collector circuit, which is zero in this case. Hence slope of the d.c. load line is ideally infinite. This tells that the d.c load line in the ideal condition is vertically straight line.

Applyimg Kirchoff's voltage law to the collector circuit we get,

Vcc- V$_{CE}$ = 0

i.e. Vcc = V$_{CE}$

- This is the d.c bias voltage V$_{CEQ}$ for the transistor.

$$\text{So } \mathbf{V_{CEQ} = V_{CC}}$$

- Hence the d.c load line is a vertical straight line passing through a voltage point on the X-axis which is $V_{CEQ} = V_{CC}$.
- The intersection of d.c load line and the base current set by the circuit is the quiescent operating point of the circuit. The corresponding collector current is I_{CQ}.

D.C Power Input:

- The d.c power input is provided by the supply voltage ith no signal input, the d.c current drawn is the collector bias current I_{CQ}. Hence the d.c power input is given by,

$$\mathbf{P_{DC} = Vcc \ I_{CQ}}$$

- The expression is same as derived earlier for directly coupled class A amplifier.

A.C. Operation

- For the a.c analysis, it necessary to draw an .c. load line on the output characteristics.
- For a.c purposes, the load on the secondary is the load impedance R_L ohms. And the reflected load on the primary i.e R_L' can be calculated.
- The load line drawn with a slope of $(-1/R_L)$ and passing through the operating point i.e quiescent point Q is called a.c load line. The d.c and a.c load lines are shown in the figure below:
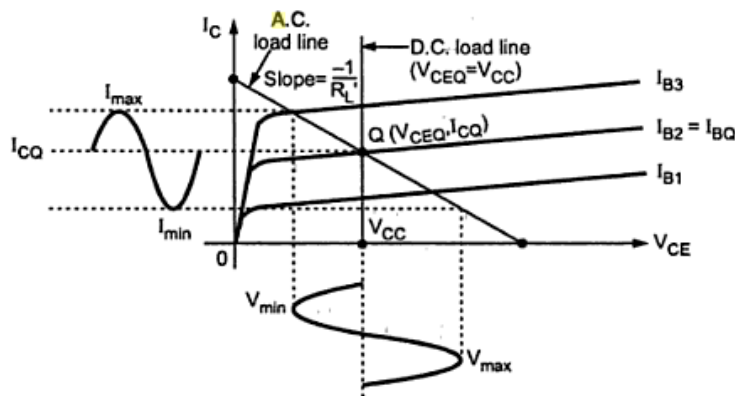
- The output current i.e collector current varies around its quiescent value ICQ, when a.c. input signal is applied to the amplifier. The corresponding output voltage also varies sinusoidally around its quiescent value V_{CEQ} which is V_{CC} in this case.

A.C Ouput Power

- The a.c power developed is on the primary side of the transformer. While calculating this power, the primary values of voltage and current and reflected load R_L' must be considered.

- The a,c power delivered to the load is on the secondary side of the transformer. While calculating load voltage, load current, load power the secondary voltage, current and the load R_L must be considered.
- The a.c. power delivered on the load is given as

$$P_{ac} = \frac{I_m{}^2 R_L{}'}{2}$$

- The generalized expression for a.c power output represented as

$$P_{ac} = \frac{(\text{Vmax} - \text{Vmin})(\text{Imax} - \text{Imin})}{8}$$

Efficiency

- The general expression for the efficiency remains same as directly coupled transformer

$$\%\eta = \frac{(\text{Vmax} - \text{Vmin})(\text{Imax} - \text{Imin})}{8V_{CC}I_{CQ}}$$

Maximum Efficiency

- The maximum efficiency for the practical circuit is about 30 to 35%

Power Dissipation:

- Power disipation in large signal amplifier is also large.
- The amount of power that must be dissipated by the transistor is the difference between the d.c power input Pdc and the a.c power delivered to the load Pac

$$P_D = P_{dc} - P_{ac}$$

Advantages &Disadvantages:

The advantages of transformer coupled class A amplifier circuit are:

- The efficiency of the operation is higher than directly coupled amplifier
- The d.c bias current that flows through the load in case of directly coupled amplifier is stopped in case of transformer coupled.
- The impedance matching required for maximum power transfer is possible.

The disadvantages are:

- Due to the transformer, the circuit becomes bulkier, heavier and costlier compared to directly coupled circuit.
- The circuit is complicated to design and implement compared to directly coupled circuit.
- The frequency response of the circuit is poor.

CLASS B AMPLIFIER

There are 2 types. They are:

      i). Push-pull class B amplifier

      ii). Complementary & symmetry class B amplifier

PUSH-PULL CLASS B AMPLIFIER

- The push pull circuit requires two transformers, one as input transformer called driver transformer and the other to connect the load called output transformer.
- The input signal is applied to the primary of the driver transformer. Both the transformers are centre tapped transformers. The push pull class B amplifier circuit is shown below:
- In the circuit, both Q1 and A2 transistors are of n-p-n type. The circuit can use both Q1 and Q of p-n-p type. In such case, the only change is that the supply voltage must be – Vcc, the basic circuit remains the same.
- Generally the circuit using n-p-n transistors is used. Both the transistors are n common emitter configuration.
- The driver transformer drives the circuit. The input signal is applied to the primary of the driver transformer. The centre tap on the secondary of the driver transformer is grounded.
- The centre tap on the primary of the output transformer is connected to the supply voltage +Vcc.
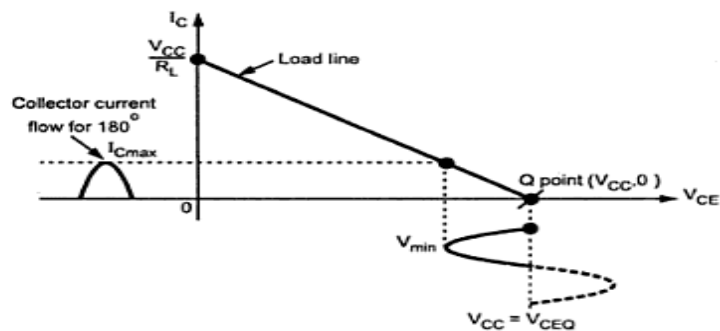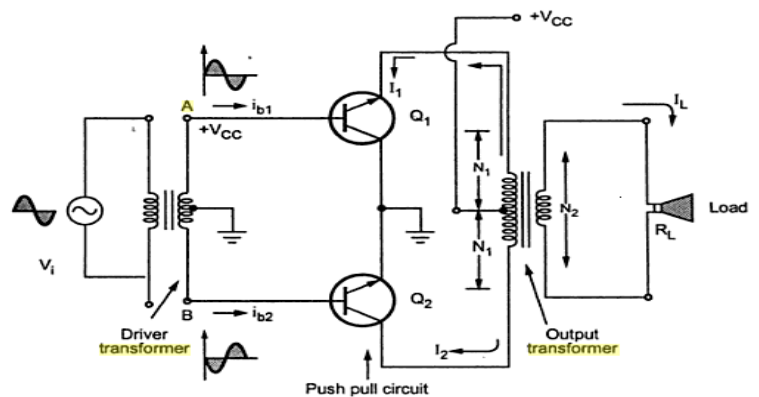
- With respect to the centre tap, for a positive half cycle of input signal, the point A shown in figure on the secondary of the driver transformer will be positive, While the point B will be negative.
- Thus the voltages in the two halves of the secondary of the driver transformer will be equal but with opposite polarity. Hence the input signals applied to the base of the transistors Q1 and A2 will be 180o out of phase
- The transistor Q1 conducts for the positive half cycle of the input producing positive half cycle across the load. While the transistor Q2 conducts for the negative half cycle across the load.
- Thus across the load, we get a full cycle for a full input cycle.
- The basic push pull operation is shown in figure.
- When point A is positive, the transistor Q1 gets driven into active region while the transistor Q2 is in cut-off region.
- While when point A is negative, the point B, hence the transistor Q2 gets driven into an active region while the transistor Q1 is in cut-off region.

D.C Operation

- The d.c biasing point i.e Q point is adjusted on the X-axis such that V_{CEQ} = Vcc and I_{CEQ} is zero. Hence the co-ordinates of Q point are (Vcc,0). There is no d.c base bias voltage.

D.C Power Input

- Each transistor output is in the form of half rectified waveform. Hence if I_m is the peak value of the output current of each transistor, the d.c or average value is I_M/π, due to half rectified waveform.
- The two currents, drawn by the two transistors from the d.c supply are in the same direction. Hence the total d.c or average current drawn from the supply is the algebraic sum of the individual average current drawn by each transistor.

$$I_{dc} = \frac{I_m}{\pi} + \frac{I_m}{\pi} = \frac{2I_m}{\pi}$$

- The total d.c power input is given by,

$$P_{DC} = Vcc \times I_{dc}$$

$$P_{DC} = \frac{2}{\pi}V_{CC}I_m$$

A.C. operation

- When the a.c signal is applied to the driver transformer, for positive half cycle Q1 conducts. The path of the current drawn by the Q1 is shown in the figure below:
- For the negative half cycle Q2 conducts. The path of the current drawn by the Q2 is shown n the figure below:

(a) Q_1 conduction   (b) Q_2 conduction
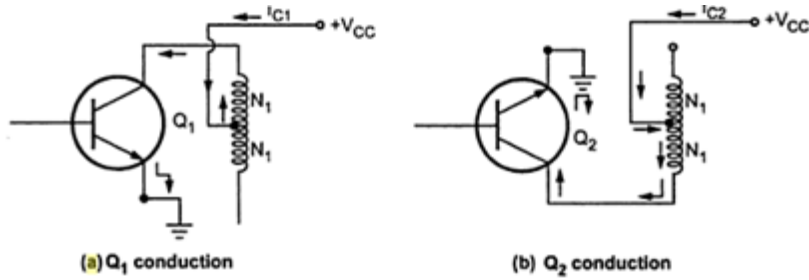
- The slope of the a.c load line is -1/RL' while the d.c load line is the vertical line passing through the operating point Q on the X-axis. The load lines are shown in the figure below:
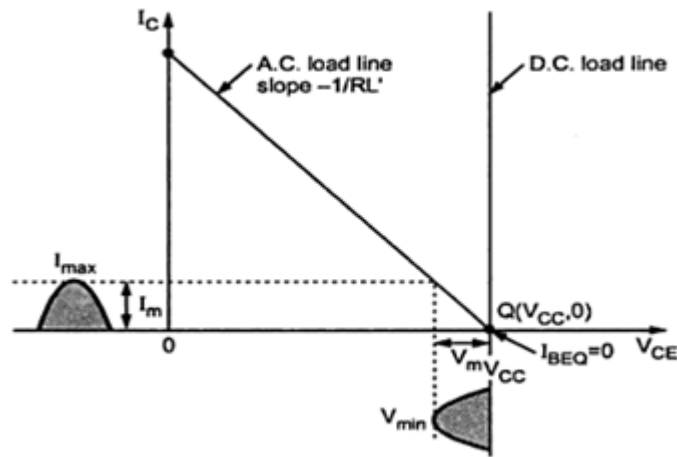
- The slope of the a.c. load line can be represented in terms of Vm and Im as,

$$R_L' = \frac{V_m}{I_m} \text{ Where Im – peak value of the collector current}$$

A.C. Power output

- The a.c. power output is expressed as,

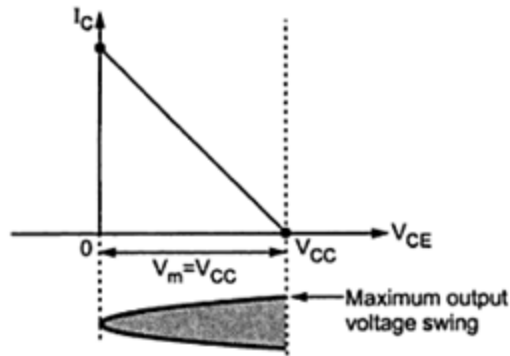$$P_{ac} = V_{rms}I_{rms} = I_{rms}^2 R_L' = \frac{V_{rms}^2}{RL'}$$

Efficiency

- The efficiency of the class B amplifier can be calculated using the basic equation

$$\%\eta = \frac{\pi}{4}\frac{V_m}{V_{CC}} \times 100$$

Maximum Efficiency

- The maximum value of Vm possible is equal to Vcc as shown in figure below:

- The efficiency is about 78.5%

Power Dissipation

- The power dissipation by both the transistors is the difference between a.c. power output and d.c. power input.

$$P_d = \frac{2}{\pi^2} \frac{V_{cc}^2}{R_L}$$

Advantages & Disadvantages:

- The efficiency is much highe than Class A operation.
- When there is no input signal, the power dissipation is zero.
- The even harmonics get cancelled. This reduces the harmonic distortion.
- As the d.c current components flow in opposite direction through the primary winding, there is no passibilty of d.c saturation of the core.

The disadvantages of the circuit are:

- Two centre tap transformers are necessary
- The transformers, make the circuit bulky and hence costlier.
- Frequency response is poor.

COMPLEMENTARY & SYMMETRY CLASS B AMPLIFIER

- The basic circuit of complementary symmetry class B amplifier is shown in figure below:
- The circuit is driven from a dual supply of Vcc. The transistor Q1 is n-p-n while Q2 is p-n-p type.
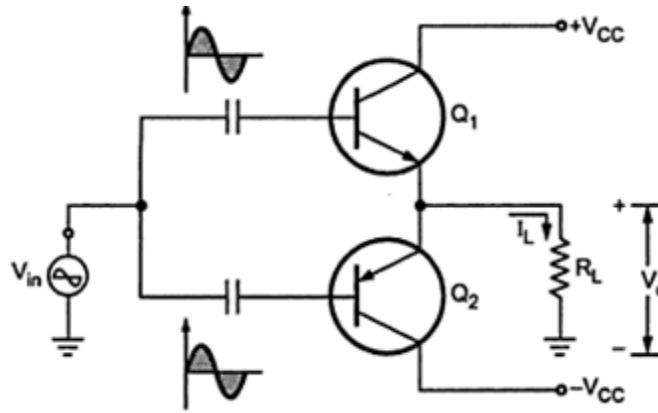
- In the positive half cycle of the input signal, the transistor Q1 gets driven into active region and starts conduction.
- The same signal gets applied to the base of the Q2 but as it is of complementary type, remains in off condition, during positive half cycle.
- This result into positive half cycle across the load R_L. This is shown in figure below.
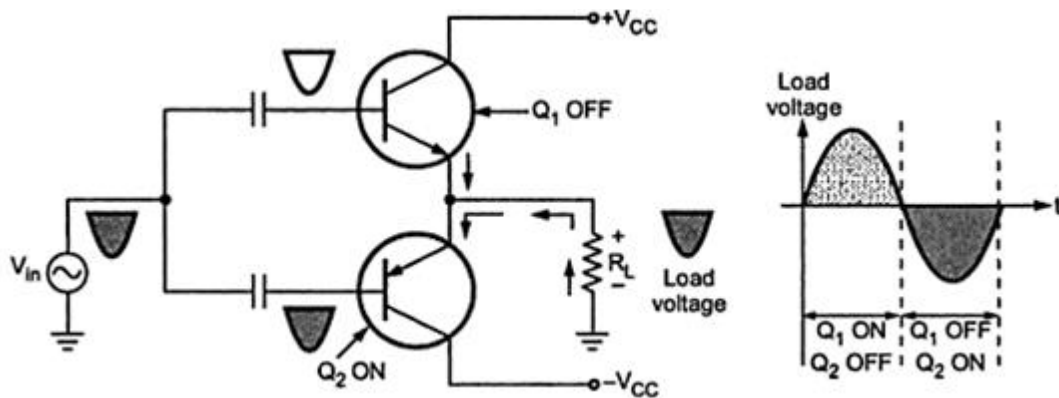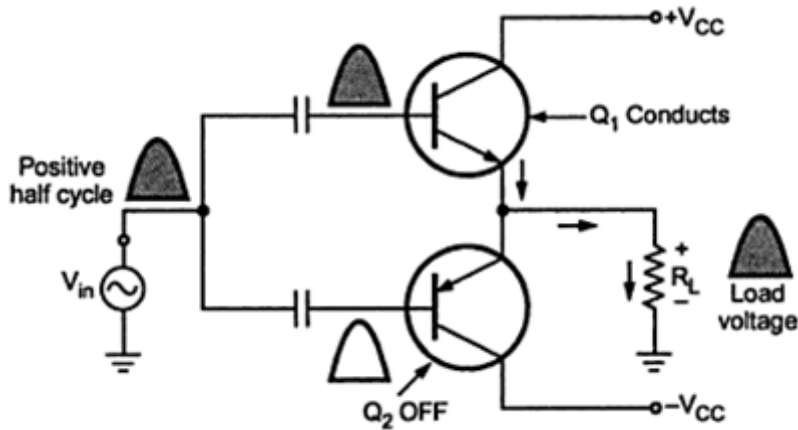
- During the negative half cycle of the signal, the transistor Q2 being p-n-p gets biased into conduction.
- While the transistor Q1 gets driven into cut off region. Hence only Q2 conducts during negative half cycle of the input, producing negative half cycle across the load RL,
- Thus for a complete cycle of input a complete cycle of output signal is developed across the load.

Advantages & Disadvantages

The advantages are:

- As the circuit is transformerless, its weight, size and cost are less.
- Due to common collector configuration, impedance matching is possible.
- The frequency response improves due to tranformerless class B amplifier circuit

The disadvantages are:

- The circuit needs two separate voltage supplies.
- The output is distorted to cross over distortion.

Cross-over distortion

- For a transistor to be in active region the base emitter junction must be forward biased.
- The junction cannot be made forward biased till the voltage applied becomes greater then cut-in voltage (Vf0 of the junction, which is generally 0.7V for silicon and 0.2 V for germanium transistors. Hence as long as the magnitude of the input signal is less than the cut-in voltage of the base emitter junction, the collector current remain zero and transistor remains in cut-off region.
- Hence there is a period between the crossing of the half cycles of the input signal, for which none of the transistors is active and the output is zero.
- Hence the nature of the output signal gets distorted and no longer remains same as that of input. Such a distorted output wave form due to cut-in voltage is shown in figure
- Such a distortion in the output signal is called a cross-over distortion. Due to cross-over distortion each transistor conducts for less than a half cycle rather than the complete half cycle.
- The part of the input cycles for which the two transistor conduct alternately is shown shaded in the figure. The cross over distortion is common in both the types of class B amplifiers
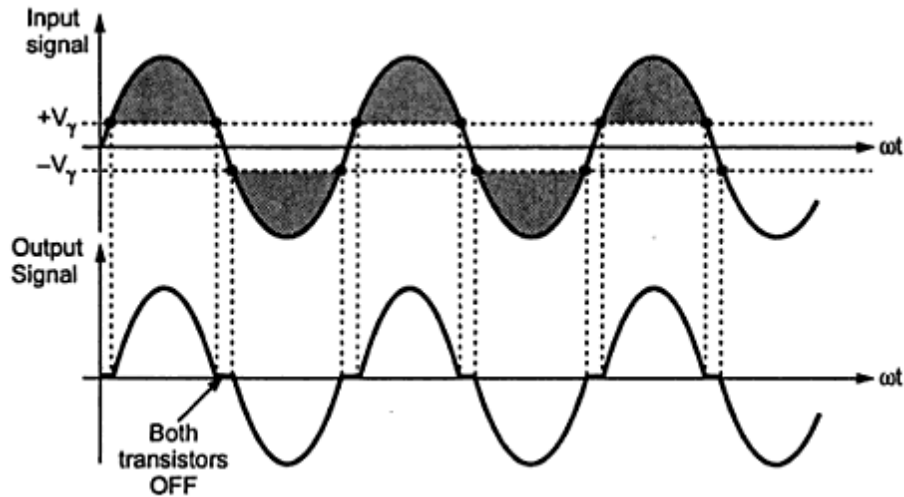
Biasing class B/ AB Amplifiers for eliminating Cross-over Distortion

- To eliminate the cross-over distortion some modification are necessary, in the basic circuits of the class B amplifiers.
- The basic reason for the cross over distortion is the cut-in voltage of the transistor junction. To overcome this cut-in voltage, a small forward biased is applied to the transistors. The practical circuits used to apply such forward biased, in the two types of class B amplifies.
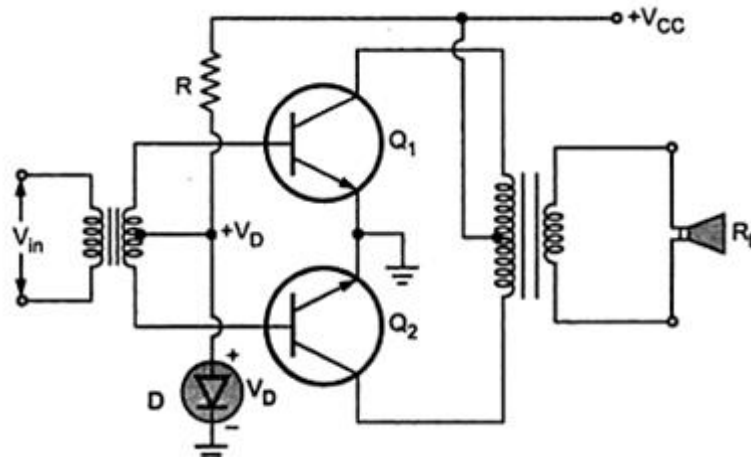

- The forward biased across the base-emitter junction of each transistor is provided by using a diode as shown in the figure.
- The drop across the diode D is equal to the cut-in voltage of the base-emitter junction of the transistor. Hence both the transistors conduct for full cycle, eliminating the cross-over distortion.
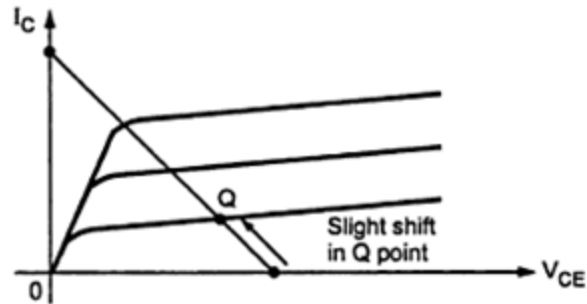
- Due to the forward biased provided to eliminate the cross-over distortion, the Q point shifts upwards on the load line as shown in figure above.
- Hence the operation of the amplifier no longer remains class B but becomes class AB operation.
- But as the amplifier handles the large signals in the range of volts, compared to these signals the shift n Q point is negligibly small.

COMPLEMENTRY SYMMETRY CLASS B AMPLIFIER:

- In push pull, transformer coupled type, the drop across forward biased one diode is sufficient, to provide necessary cut-in voltage. But in case of complementary symmetry circuit, base emitter junctions of both Q1 and Q2 are required to provide a fixed Bias.
- Hence for silicon transistors a fixed bias of $0.7+0.7 = 1.4$ V is required. This can be achieved by using a potential divider arrangement as shown in the figure.
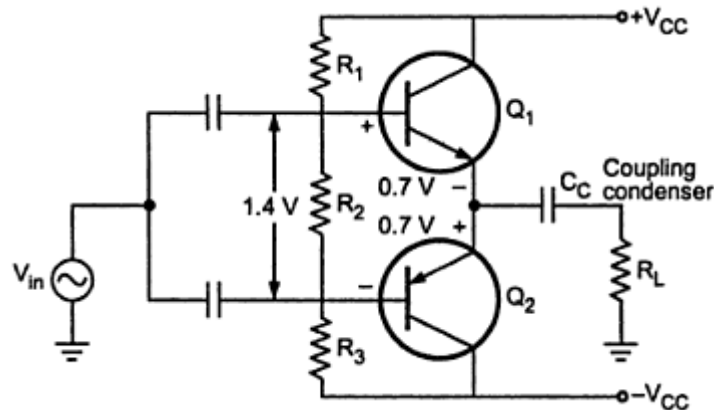
- But in this circuit, the fixed bias provided is fixed qual to say 1.4 V.
- While the junction cut-in voltage changes with respect to the temperature. Hence there is still possibility of a distortion when there is temperature change. Hence instead of R2, the two diodes can be used to provide the required fixed bias.
- As the temperature changes, along with junction characteristics, the diode characteristics get changed and maintain the necessary biasing required to overcome the cross-over distortion

when there is temperature change. The arrangement of the circuit with the two diodes is shown in the figure below
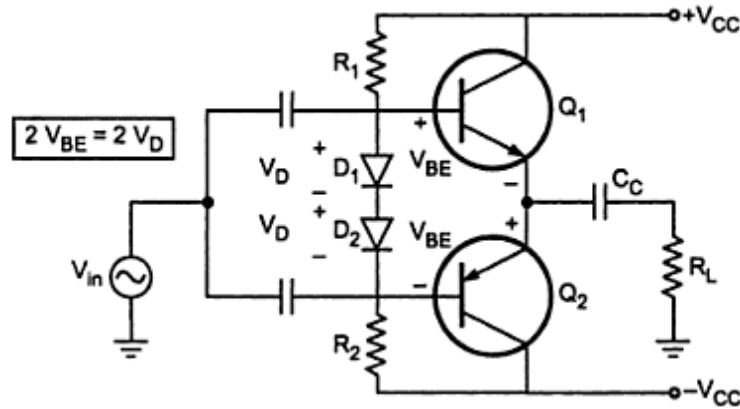
CLASS C AMPLIFIER

- Biasing resistor Rb pulls the base of Q1 further downwards and the Q-point will be set some way below the cut-off point in the DC load line.
- As a result the transistor will start conducting only after the input signal amplitude has risen above the base emitter voltage (Vbe~0.7V) plus the downward bias voltage caused by Rb.
- That is the reason why the major portion of the input signal is absent in the output signal.
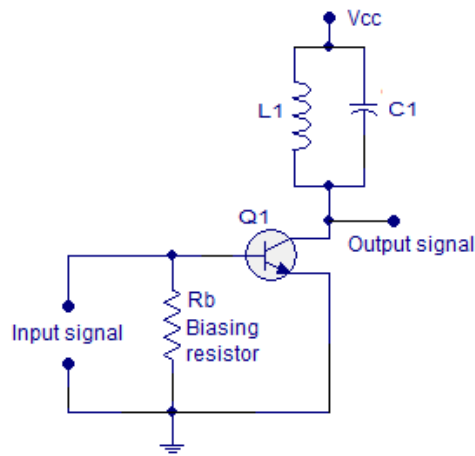
Class C power amplifier   www.circuitstoday.com

- Inductor L1 and capacitor C1 forms a tank circuit which aids in the extraction of the required signal from the pulsed output of the transistor.
- Actual job of the active element (transistor) here is to produce a series of current pulses according to the input and make it flow through the resonant circuit. Values of L1 and C1 are so selected that the resonant circuit oscillates in the frequency of the input signal.
- Since the resonant circuit oscillates in one frequency (generally the carrier frequency) all other frequencies are attenuated and the required frequency can be squeezed out using a suitably tuned load.

- Harmonics or noise present in the output signal can be eliminated using additional filters. A coupling transformer can be used for transferring the power to the load.

Advantages of Class C power amplifier.
- High efficiency.
- Excellent in RF applications.
- Lowest physical size for a given power output.

**Disadvantages of Class C power amplifier.**
- Lowest linearity.
- Not suitable in audio applications.
- Creates a lot of RF interference.
- It is difficult to obtain ideal inductors and coupling transformers.
- Reduced dynamic range.

Applications of Class C power amplifier.
- RF oscillators.
- RF amplifier.
- FM transmitters.
- Booster amplifiers.
- High frequency repeaters.
- Tuned amplifiers etc.

CLASS D AMPLIFIERS

- The figure below shows the basic concept of class D amplifier. The amplifier consists of two complementary symmetry transistors driving a load RL. This means one transistor is p-n-p and other is n-p-n
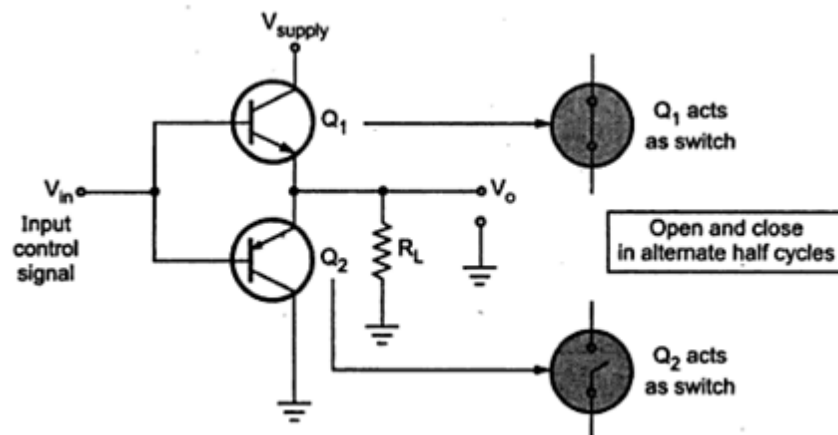
- The transistors are biased in such a way that they behave as ideal switches.

- When transistor is ON, it is biased to saturation so that voltage across it is zero while current is high. When transistor is OFF, it is biased to cut-off so that current trough it is zero while voltage is high.
- Thus when input goes positive Q1 conducts heavily acting as closed switch while Q2 is OFF.
- While when input goes negative, Q2 conducts heavily acting as closed switch while Q1 is OFF. Thus the load voltage V_o across RL has one of two possible values which are V_{Supply} or 0V.
- This is a type of digital output having two levels high and low.
- The transistors dissipate almost zero power as in any of the states, either voltage is zero or current is zero for the transistors.
- Thus entire power input is available to the load. Hence efficiency of class D amplifiers is almost 100%. The figure of merit which is the ratio of the maximum power dissipated in transistor to that delivered to the load, is zero.
- These facts make the class D amplifier as an ideal amplifier.
- Practically class D amplifiers are designed to operate with digital or pulse type of signals. The basic block diagram of unit used along with class D amplifier in the application circuits is shown in the figure below:
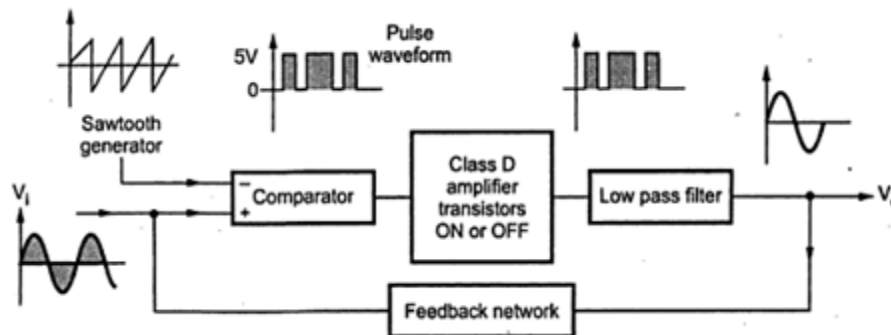

- The op-amp comparator is used for which one input is saw tooth type while other is sinusoidal.
- The comparator converts sinusoidal signal to digital pulse type signal with the help of saw tooth waveform. This is called chopping of sinusoidal signal to produce digital signal. This signal drives the class D amplifier.
- When pulse signal is high the transistors are ON and when it is low, the transistors are OFF. Thus most of the power supplied is delivered to he load by producing high power output signal.
- The digital signal is converter back to the original sinusoidal signal using low pass filter. Using feedback network, it is fed back to the comparator.
- Practically instead of power BJT, power MOSFET devices are used as driver for class D amplifier.
- The class D amplifiers are used in the pulse and digital circuits.

DISTORTION IN AMPLIFIERS:

- The input signal applied to the amplifiers is alternating in nature.
- The basic features of any alternating signal are amplitude, frequency and phase.
- The amplifier output should be reproduced faithfully i.e. there should not be the change or distortion in the amplitude, frequency and phase of the signal.
- Hence the possible distortions in any amplifier are amplitude distortion, phase distortions and frequency distortion.
- While the change in gain of the amplifier with respect to the frequency is called frequency distortion
- The dynamic characteristics of a transistor are a straight line over the operating range.
- But in practical circuits, the dynamic characteristic is not perfectly linear.
- Due to such non-linearity in the dynamic characteristics, the waveform of the output voltage differs from that of the input signal.
- Such a distortion is called nonlinear distortion or amplitude distortion or harmonic distortion.

Harmonic Distortion

- The harmonic distortion means the presence of the frequency components in the output waveform, which are not present in the input signal.
- The component with frequency same as the input signal is called fundamental frequency components which are integer multiples of fundamental frequency component. These components are called harmonic components or harmonics.
- For example if the fundamental frequency component. These components at f Hz and additional frequency components at 2f Hz, 3f Hz, 4f Hz and so on.
- The 2f component is called second harmonic, the 3f component is called third harmonic and so on. The fundamental frequency component is not considered as a harmonic.
- Out of all the harmonic components, the second harmonic has the largest amplitude.
- As the second harmonic amplitude is largest, the second harmonic distortion is more important in the analysis of A.F power amplifiers. The figure shows the various harmonic components.
- It can be seen from the figure that the distorted waveform can be obtained by adding the fundamental and the harmonic components.
- The percentage harmonic distortion due to each order can be calculated by comparing the amplitude of each order of harmonic with the amplitude of the frequency component

(a) Fundamental   (b) 2nd Harmonic   (c) 3rd Harmonic   (d) Distorted waveform
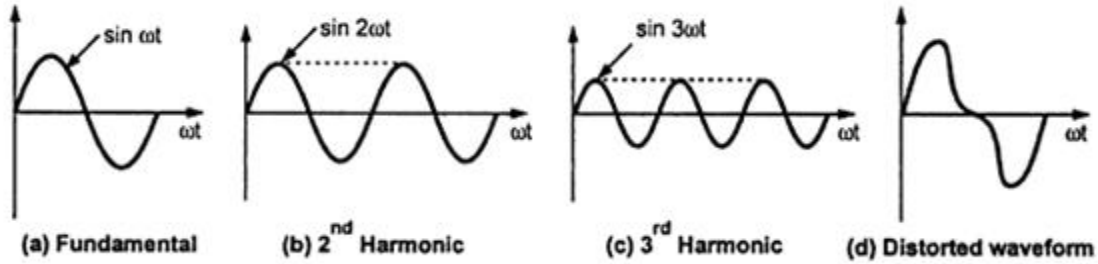
- If the fundamental frequency component has an amplitude of B1 and the nth harmonic component has an amplitude of Bn then the percentage harmonic distortion due to nth harmonic component is expressed as,

$$\% \, n^{th} \, harmonic \, distortion = \%D_n = \frac{|B_n|}{|B_1|} \times 100$$

Total Harmonic Distortion:

- When the output signal gets distorted due to various harmonic distortion components, the total harmonic distortion, which is the effective distortion due to all the individual components is given by,

$$\%D = \sqrt{D_2{}^2 + D_3{}^2 + D_4{}^2 + \cdots} \times 100$$

Where D = total harmonic distortion

Power output due to Distortion

- When the distortion is negligible, the power delivered to the load is given by,

$$P_{ac} = \frac{I_m{}^2 R_L}{2}$$

But **Im** = Peak value of the output current

$$= \frac{I_{pp}}{2} = \frac{I_{max} - I_{min}}{2}$$

But $B1 = \frac{I_{max} - I_{min}}{2}$

Im = B1 = Fundamental frequency component

$$P_{ac} = \frac{1}{2} B1^2 R_L$$

- With distortion, the power delivered to the load increase proportional to the amplitude of the harmonic component

$$(P_{ac})_D = P_{ac}[1 + D^2]$$

- This is the power delivered to the load due to the harmonic distortion.

Heat Sink for power transistors:

- The maximum power handled by a particular power transistor and the temperature of the transistor junctions are closely related.
- This is because of the fact that the junction temperature inccreases due to the power dissipation. The collector dissipation can be obtained as

$$P_d = V_{CE}I_C$$

- Let T$_J$ be the junction temperature which due to power dissipation. Manufacture provides the maximum permissible value of TJ and corresponding maximum available value of the power dissipation Pd.
- If the temperature keeps on increasing, at a certain temperature, the crystalline structure is destroyed and there is no change of recovery. The lower limit of a semiconductor is taken as,

$$-65^\circ C \leq T_J \leq (T_J)_{max}$$

Where $(T_J)_{max}$ is specified by the manufactures.

- Thus practically it is necessary to keep the junction temperature less than $(T_J)_{max}$ specified for the power transistor used in the power amplifier
- The heat sink draws heat from the power transistor via thermal condition and expels the heat into the ambient air via thermal convection and heat radiation.
- The figure below shows a power transistor with a heat sink.
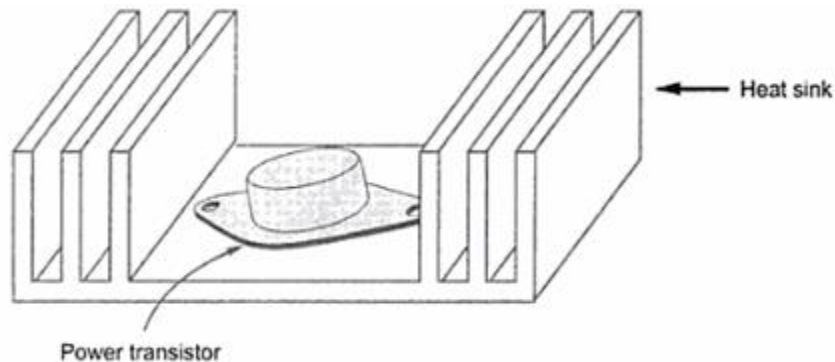
- If the heat developed is transformed to the surroundings instantaneously, the collector dissipation rating would be infinite. But in practice such ideal situation is not possible due to thermal lag.

The important advantages of heat sink are,

- The temperature of the case gets lowered.
- The power handling capacity of the transistors can approach the rated maximum value.

Thermal Analogy of power Transistors

- The heat dissipation problem is very much analogous to a simple electric circuit and ohm's law.
- An electric flow when there exists a potential difference while the heat flows when there exists a temperature difference (T2 – T1). Then similar to a electric resistance a thermal resistance can be obtained as,

$$\theta = \frac{T_2 - T_1}{P_d} \, °C/W$$

Where Pd is the heat dissipated or heat flow, due to the power dissipation. From the above relation we can write,

$$T_2 - T_1 = \theta P_d \, °C$$

$$P_d = \frac{T_2 - T_1}{\theta} \, W \text{ or } mW$$

- Now to develop the thermal-electric analogy let us define some parameters as

TJ = Junction Temperature

TC = Case Temperature

TA = Ambient Temperature

θ_{JA} = Total thermal Resistance

θ_{JC} = Transistor thermal Resistance

θ_{CS} = Insulator thermal Resistance

θ_{SA} = Heat Sink thermal Resistance

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- Then similar to a electric resistance a thermal resistance can be obtained as,

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- From the above figure relation we can write,

$$T_2 - T_1 = \theta \, P_d \, °C$$
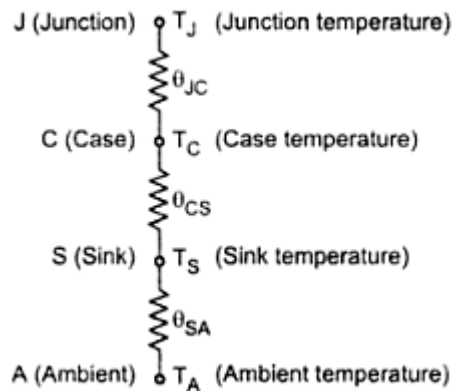
- Special grease is often used to establish good heat conducting path between the case and the heat sink.

- Hence the temperature of heat sink and case are considered different. From the property of series circuit we can write,

$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \, °CW$

Applying the Kirchhoff" law we get,

$T_J = T_A + \theta_{JA} P_d \, °C$

Pd is the collector power dissipation ie.

- The power dissipated at the collector junction.

- The equation shows that the junction temperature floats on the ambient temperature and higher the value of the ambient temperature lower is the value of allowable power dissipation.

CONVERSION OF EFFICIENCY CALCULATIONS

- A measure of the ability of an active device to convert the dc power of the supply into the ac (signal) power delivered to the load is called the conversion efficiency or theoretical efficiency.

- It denoted as ŋ, is called the collector efficiency for a transistor amplifier and drain-circuit efficiency for a FET stage.

$$\% \eta = \frac{Signal\ Power\ delivered\ to\ the\ load}{DC\ Power\ supplied\ to\ the\ ouput\ circuit}$$