DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Subject Name: **ELECTRONIC DEVICES AND CIRCUITS**

Subject Code: **EE T34**

UNIT –I SEMICONDUCTOR THEORY AND PN DIODES

Introduction to Semiconductor materials–atomic theory–energy band structure of insulators, conductors and semiconductors–intrinsic and extrinsic semiconductors–N-type and P-type semiconductors.

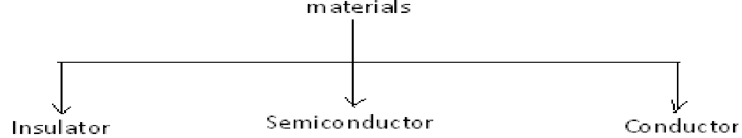
SEMICONDUCTOR DIODES:

Construction – forward and reverse bias operation – mathematical model of a PN diode–Silicon versus Germanium diodes – Effects of temperature on diode operation– Static and dynamic resistances–Diode equivalent models– Specification sheets–Transition and diffusion capacitances–Diode switching-reverse recovery time–Diode applications.

(11 MARKS)

1. Explain the behavior of insulators, conductors and semiconductors by drawing the energy band structure. [Nov/Dec 2014] [Nov 2013]

Based on the electrical conductivity all the materials in nature are classified as insulators, semiconductors, and conductors.



Insulator:

- An insulator is a material that offers a very low level (or negligible) of conductivity when voltage is applied. Eg: Paper, Mica, glass, quartz.
- The energy band structure of an insulator is shown in the fig.1.1. Band structure of a material defines the band of energy levels that an electron can occupy. Valance band is the range of electron energy where the electron remains bonded to the atom and do not contribute to the electric current.
- Conduction band is the range of electron energies higher than valance band where electrons are free to accelerate under the influence of external voltage source resulting in the flow of charge.
- The energy band between the valance band and conduction band is called as forbidden band gap. It is the energy required by an electron to move from balance band to conduction band i.e. the energy required for a valance electron to become a free electron.

$$1 \ \text{eV} = 1.6 \times 10^{-19} \text{ J}$$

- For an insulator, as shown in the fig.1.1 there is a large forbidden band gap of greater than 15ev.
- Because of this large gap there a very few electrons in the CB and hence the Conductivity of insulator is poor.
- Thus insulators have very high resistivity a room temperature
- Typical resistivity level of an insulator is of the order of 10^{10} to 10^{12} Ω-cm.
- However if the temperature is raised ,some of the valence electrons may acquire energy and jump into the conduction band
- It causes the resistivity of the insulators to decrease.
- Therefore insulators have negative temperature coefficient of resistance.

Conductors:

- A conductor is a material which supports a generous flow of charge when a voltage is applied across its terminals. i.e. it has very high conductivity. Eg: Copper, Aluminum, Silver, and Gold.
- The resistivity of a conductor is in the order of 10^{-4} and 10^{-6} Ω-cm.
- The Valance and conduction bands overlap (fig1.1) and there is no energy gap for the electrons to move from valance band to conduction band.
- This implies that there are free electrons in Conduction Band even at absolute zero temperature (0K).
- Therefore at room temperature when electric field is applied large current flows through the conductor.

Semiconductor:

- A semiconductor is a material that has its conductivity somewhere between the insulator and conductor.
- Two of the most commonly used semiconductors are Silicon (Si=14 atomic no.) and germanium (Ge=32 atomic no.). Both have 4 valance electrons.
- The resistivity level is in the range of 10 and 10^4 Ω-cm.
- The forbidden band gap is in the order of 1eV. For eg,the energy gap for Si, Ge and Ga As is 1.21, 0.785 and 1.42 eV, respectively at absolute zero temperature (0K).
- A small energy gap means that a small amount of energy is required to free the electrons from valence band to conduction band.
- At 0K and at low temperatures, the valance band electrons do not have sufficient energy to move to Conduction Band.
- Thus semiconductors act as insulators at 0K. As the temperature increases, a large number of valance electrons acquire sufficient energy to leave the Valence Band, cross the forbidden energy gap and reach Conduction Band.
- These are now free electrons as they can move freely under the influence of electric field.
- At room temperature there are sufficient electrons in the Conduction Band and hence the semiconductor is capable of conducting some current at room temperature.
- Semiconductors also have negative temperature coefficient of resistance .It means the conductivity of semiconductor increases with the increase in temperature.

Insulator	Semiconductor	Conductor
10^{-6} Ω-cm (Cu)	50Ω-cm (Ge)	10^{12} Ω-cm (mica)
	50×10^3 Ω-cm (Si)	

Typical resistivity values

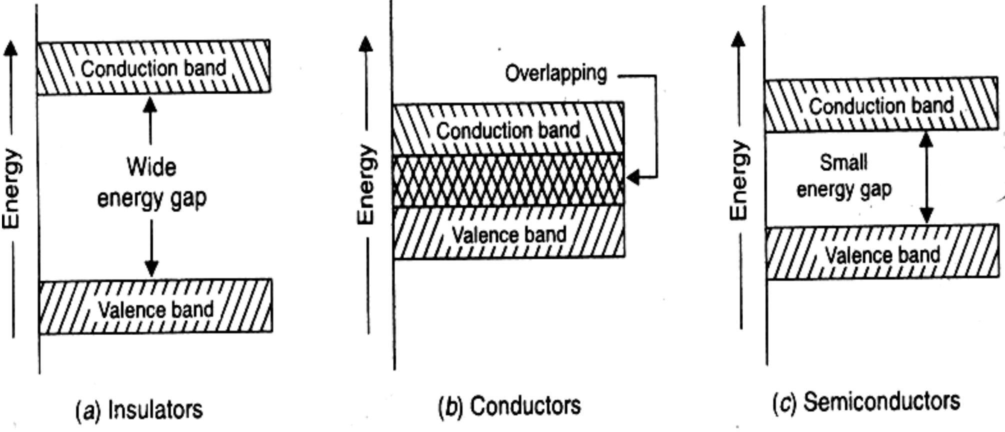


Fig:1.1

Semiconductors are classified in to two types

(i) Intrinsic Semiconductors (ii) Exterinsic semi-conductors

a. n-type semi-conductors
b. p-type semi-conductors

2. Explain the operation of N type extrinsic semiconductor.[April 2015]

- Intrinsic semiconductor has very limited applications as they conduct very small amount of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding small amounts of impurity to the intrinsic semiconductor.
- By adding impurities it becomes impure or extrinsic semiconductor.
- This process of adding impurities is called as doping.
- The amount of impurity is added at a rate of only one atom of impurity per 10^6 to 10^{10} semiconductor atoms.
- The purpose of adding impurity is to increase either the number of free electrons or holes in semiconductor.

N type semiconductor:

- If the added impurity is a pentavalent atom then the resultant semiconductor is called N-type semiconductor. Examples of pentavalent impurities are Phosphorus, Arsenic, Bismuth, Antimony etc.
- A pentavalent impurity has five valance electrons. Fig 1.2a shows the crystal structure of N-type semiconductor material where four out of five valance electrons of the impurity atom(antimony) forms covalent bond with the four intrinsic semiconductor atoms.
- The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy.

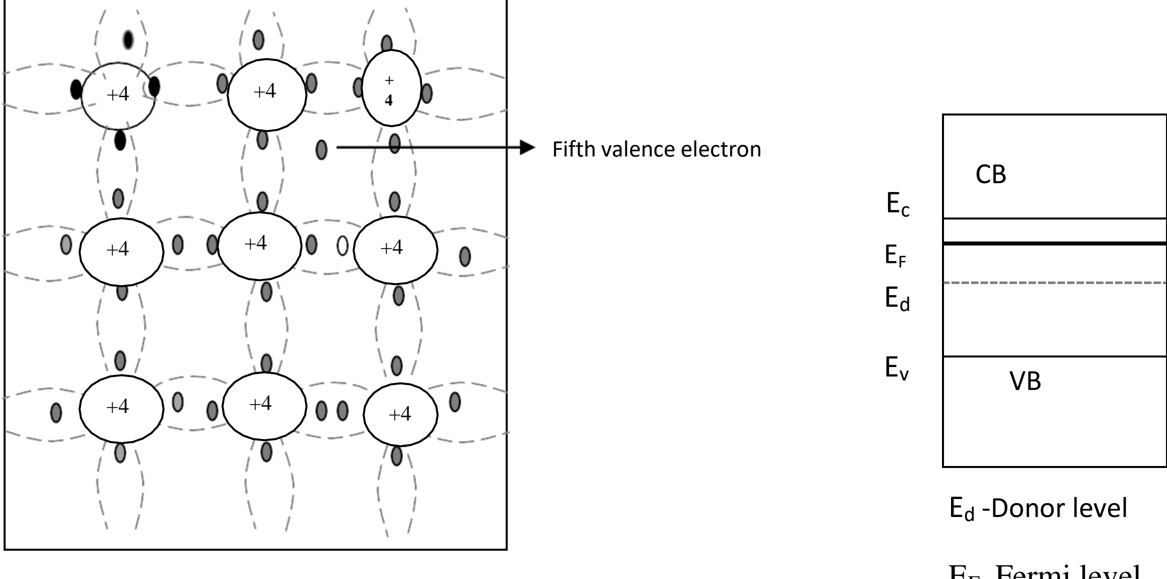


Fig. 1.2a Crystal structure of N type Semiconductor

Fig. 1.2bEnergy band diagram of N type

- The energy required to detach the fifth electron form the impurity atom is very small of the order of 0.01ev for Ge and 0.05 eV for Si.
- The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level E_d slightly less than the conduction band.
- The difference between the energy levels of the conducting band and the donor energy level is the energy required to free the fifth valence electron (0.01 eV for Ge and 0.05 eV for Si).
- At room temperature almost all the fifth electrons from the donor impurity atom are raised to conduction band and hence the number of electrons in the conduction band increases significantly.
- Thus every antimony atom contributes to one conduction electron without creating a hole.
- Because of the greater number of electrons in the conduction band than that of holes in the valence band and hence the Fermi level shifts upwards below the conduction band.
- After the donation, the impurity atom becomes a positively charged ion and is known as donor ion.
- The position of the donor ion is fixed in the crystal lattice and these are known as immobile ions.
- Thus current in N type semiconductor is dominated by electrons which are referred to as majority carriers and holes as minority carriers.

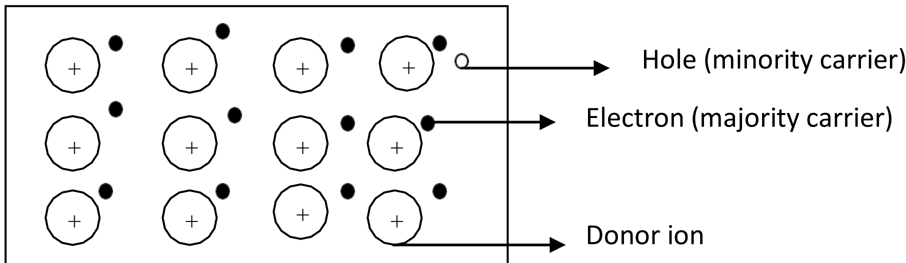


Fig. 1.2c Crystal Structure of N Type Semiconductor

3. Explain the operation of P type extrinsic semiconductor.[April 2015]

- Intrinsic semiconductor has very limited applications as they conduct very small amount of current at room temperature. The current conduction capability of intrinsic semiconductor can be increased significantly by adding a small amounts impurity to the intrinsic semiconductor.
- By adding impurities it becomes impure or extrinsic semiconductor. This process of adding impurities is called as doping.
- The amount of impurity is added at a rate of only one atom of impurity per 10^6 to 10^{10} semiconductor atoms.

- The purpose of adding impurity is to increase either the number of free electrons or holes in semiconductor.

P type semiconductor:

- If the added impurity is a trivalent atom then the resultant semiconductor is called P-type semiconductor. Examples of trivalent impurities are Boron, Gallium, indium, Aluminium .
- The crystal structure of P type semiconductor is shown in the fig1.3a. The three valance electrons of the impurity (boron) forms three covalent bonds with the neighbouring atoms and a vacancy exists in the fourth bond giving rise to the holes.
- The hole is ready to accept an electron from the neighboring atoms.
- Each trivalent atom contributes to one hole generation and thus introduces a large no. of holes in the valance band.
- At the same time the no. electrons are decreased compared to those available in intrinsic semiconductor because of increased recombination due to creation of additional holes.

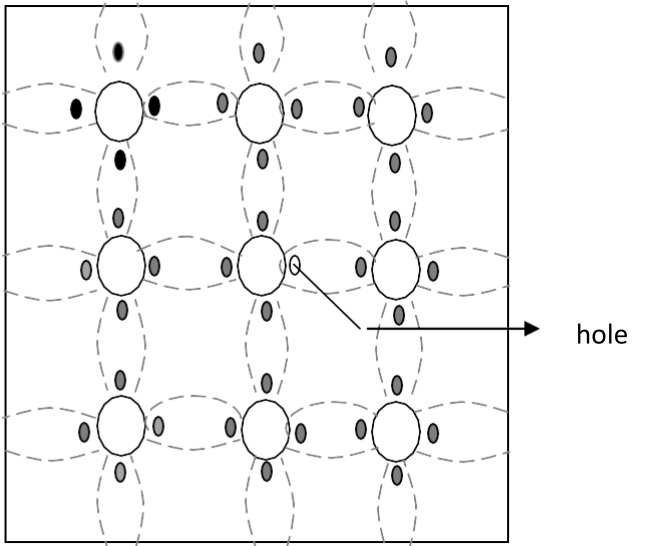


Fig. 1.3a Crystal structure of P type semiconductor

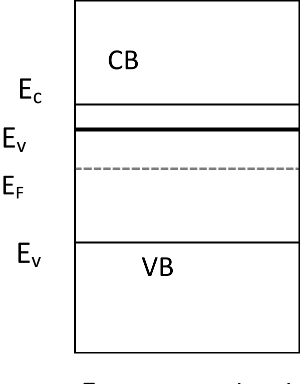


Fig. 1.3 cEnergy band diagram of N type

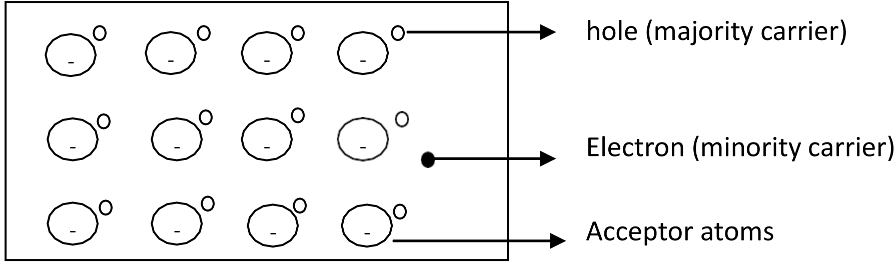


Fig. 1.3b crystal structure of P type semiconductor

- The fifth electron is loosely bound to the impurity atom. This loosely bound electron can be easily excited from the valance band to the conduction band by the application of electric field or increasing the thermal energy.
- The energy required to detach the fifth electron form the impurity atom is very small of the order of 0.01ev for Ge and 0.05 eV for Si.
- The number of electrons in the conduction band decreases below a level.
- Because of the greater number of holes in the valence band than that of electrons in conduction band, the Fermi level shifts downwards towards top of the valence band.
- As hole moves away from the parent atom, it acquires a negative charge.
- This negative charged atom is known as acceptor ion. These does not take place in conduction and it becomes an immobile ion.
- Thus in P type semiconductor, holes are majority carriers and electrons are minority carriers.
- Since each trivalent impurity atoms are capable accepting an electron, these are called as acceptor atoms. The following fig 1.3b shows the pictorial representation of P type semiconductor.
- The conductivity of N type semiconductor is greater than that of P type sc as the mobility of electron is greater than that of hole.
- For the same level of doping in N type semiconductor and P type semiconductor, the conductivity of an N type semiconductor is around twice that of a P type semiconductor.

4. Explain the operation of intrinsic semiconductor.

- The materials whose electrical properties lie between those of conductors and insulators are known as semiconductors.
- At absolute zero temperature (i.e) at 0K there are no electrons in the conduction band of semiconductors and valence band is completely filled. Thus the semiconductors behave like perfect insulators at 0K.
- However if the temperature is increased, the width of the energy gap reduces and consequently some of the electrons jump into conduction band.
- The electrical conductivity of semiconductors lies in the range of 10^{-3} to 10^{-6} per ohm per cm.
- A pure form of semiconductors is called as intrinsic semiconductor. Conduction in intrinsic semiconductor is either due to thermal excitation or crystal defects. Si and Ge are the two most important semiconductors used. Other examples include Gallium arsenide GaAs, Indium Antimonide (InSb) etc.
- For germanium, the impurity level is less than 1 part in 10^8 parts. For silicon it is less than 1 part in 10^{12} parts

- Let us consider the structure of Si. A Si atomic no. is 14 and it has 4 valance electrons.
- These 4 electrons are shared by four neighboring atoms in the crystal structure by means of covalent bond. Fig. 1.4a shows the crystal structure of Si at absolute zero temperature (0K).
- In that structure all the valence electrons are tightly held by the parent atoms and through covalent bonds by other atoms
- Hence a pure Semiconductor acts has poor conductivity (due to lack of free electrons) at low or absolute zero temperature.

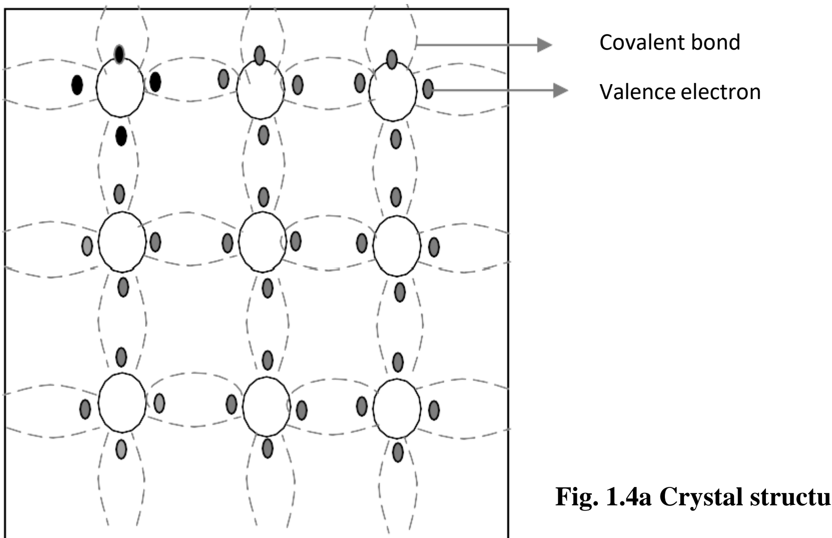


Fig. 1.4a Crystal structure of Si at 0K

- At room temperature some of the covalent bonds break up to thermal energy as shown in fig 1.4b.
- The valance electrons that jump into conduction band are called as free electrons that are available for conduction.

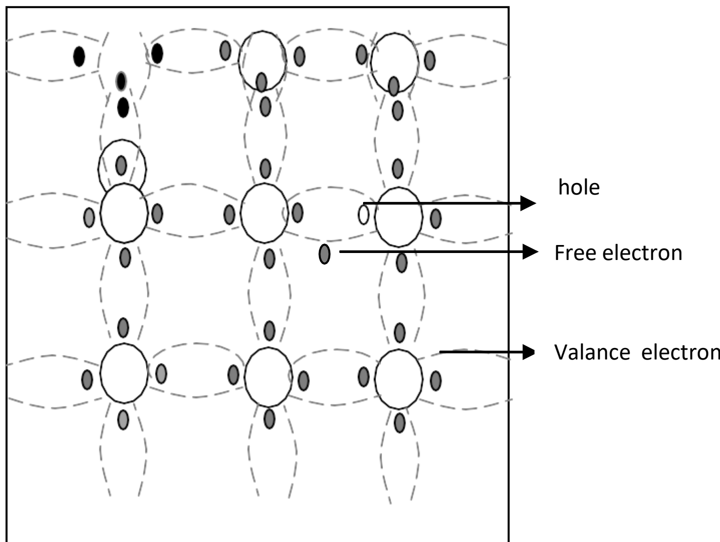


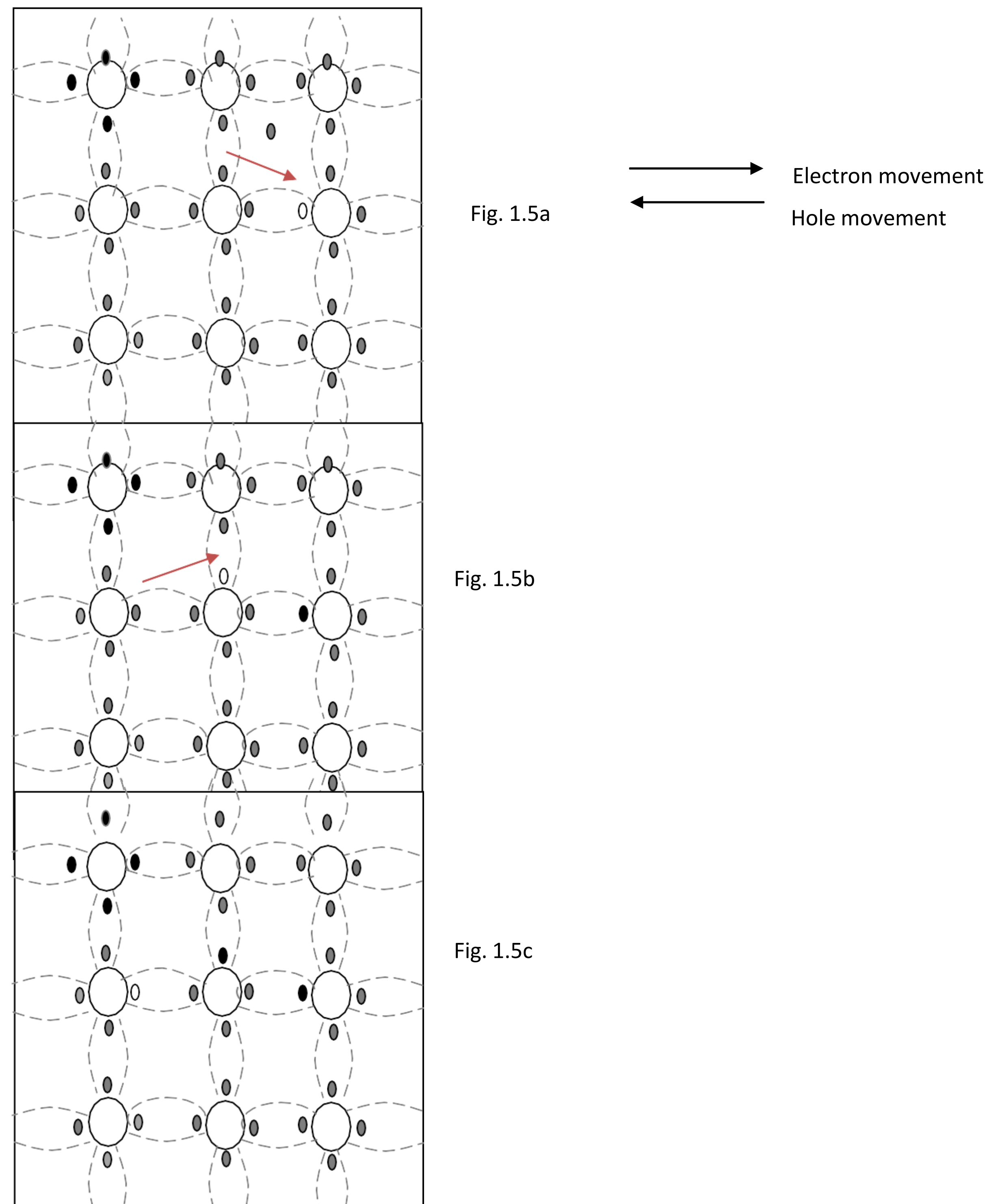
Fig. 1.4b crystal structure of Si at room temperature0K

- The energy required to break the covalent bond is equal to band gap energy. The value of E_G is 1.1 eV and 0.72 eV for germanium.
- The vacancy of an incomplete covalent bond left behind the dislodged electron is hole. The absence of electrons in covalent bond is represented by a small circle usually referred to as hole which is of positive charge.

- Even a hole serves as carrier of electricity in a manner similar to that of free electron.
- The combination of such a free electron and a hole is called electron hole pair.

The mechanism by which a hole contributes to conductivity is explained as follows:

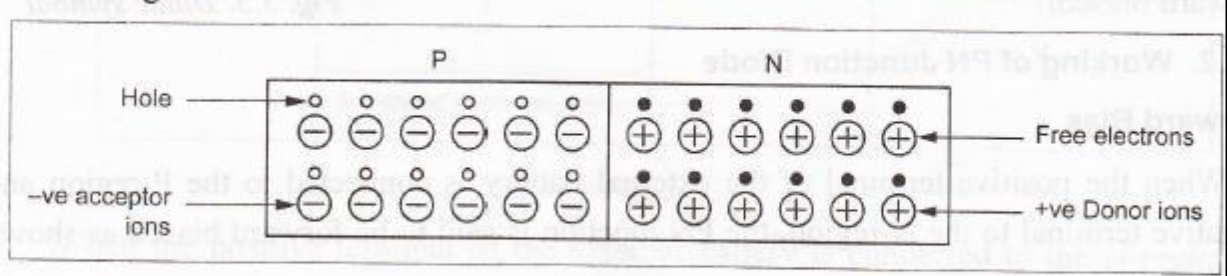
- When a bond is in complete so that a hole exists, it is relatively easy for a valance electron in the neighboring atom to leave its covalent bond to fill this hole. An electron moving from a bond to fill a hole moves in a direction opposite to that of the electron.
- This hole, in its new position may now be filled by an electron from another covalent bond and the hole will correspondingly move one more step in the direction opposite to the motion of electron.
- Here we have a mechanism for conduction of electricity which does not involve free electrons. This phenomenon is illustrated in fig1.5



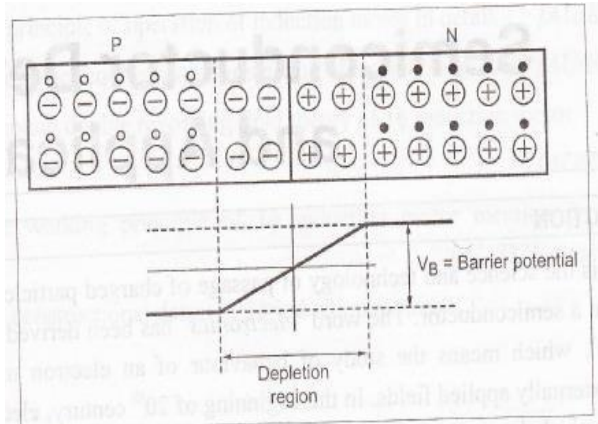
- Fig 1.5a show that there is a hole at ion 6.Imagine that an electron from ion 5 moves into the hole at ion 6 so that the configuration of 1.5b results.
- If we compare both fig1.5a &fig 1.5b, it appears as if the hole has moved towards the left from ion6 to ion 5.
- Further if we compare fig 1.5b and fig 1.5c, the hole moves from ion5 to ion 4. This discussion indicates the motion of hole is in a direction opposite to that of motion of electron.
- Hence we consider holes as physical entities whose movement constitutes flow of current.
- In a pure semiconductor, the number of holes is equal to the number of free electrons.

5. Explain the construction and working of PN diode with a neat sketch. [Nov/Dec 2014] [April 2015]

- A **PN junction** is formed from a piece of semiconductor (Ge or Si) by diffusing p-type material (Acceptor impurity Atoms) to one half side and N type material to (Donar Impurity Atoms) other half side. The plane dividing the two zones is known as 'Junction'.
- The p region is called the anode and n region is called the cathode.
- The P-region of the semiconductor contains a large number of holes and N region, contains a large number of electrons. A PN junction just immediately formed is shown in Fig.



- When PN junction is formed, there is a tendency for the electrons in the N-region to diffuse into the p-region, and holes from P-region to N-region. This process is called diffusion.
- While crossing the junction, the electrons and holes recombines with each other, leaving the immobile ions in the neighbourhood of the junction unneutralized as shown in Fig.

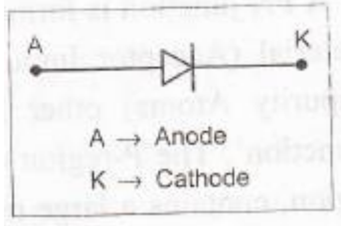


- These immobile + ve and –ve ions, set up a potential across the junction. This potential is called potential barrier or junction barrier.

- Due to the potential barrier no further diffusion of electrons and holes takes place across the junction.
- Potential barrier is defined as a potential difference built up across the PN junction which restricts further movement of charge carriers across the junction.
- The potential barrier for a silicon PN junction is about 0.7 volt, whereas for Germanium PN junction is approximately 0.3 volt.

Symbol of Diode:

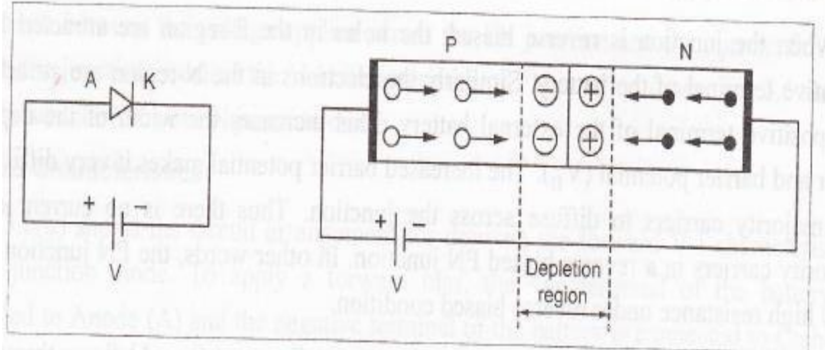
- The symbol of PN junction diode is shown in Fig .The P-type and N-type regions are referred to as Anode and Cathode respectively. The arrowhead shows the conventional direction of current flow when the diode is forward biased.



Working of PN Junction Diode:

Forward Bias:

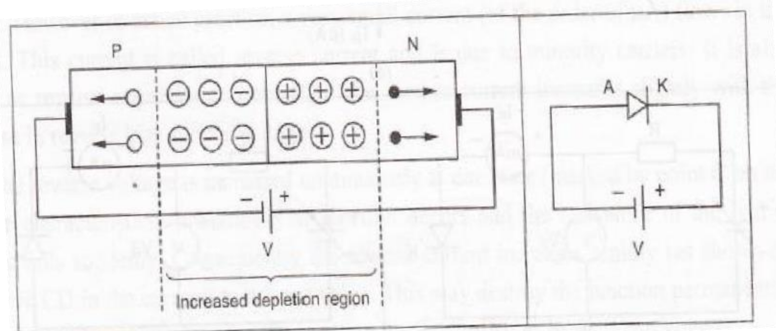
- When the positive terminal of the external battery is connected to the P-region and negative terminal to the N-region, the PN junction is said to be forward biased as shown in Fig.



- When the junction is forward biased, the holes in the p-region are repelled by the positive terminal of the battery and are forced to move towards the junction.
- Similarly the electrons in the N-region are repelled by the negative terminal of the battery and are forced to move towards the-junction.
- This reduces the width of the depletion layer and barrier potential. If the applied voltage is greater than the potential barrier v_r, then the majority carriers namely holes in P-region and electrons in N-region cross the barrier. During crossing some of the charges get neutralized the remaining charges after crossing, reach the other side and constitute current in the forward direction. The PN junction offers very low resistance under forward biased condition.
- Since the barrier potential is very small (nearly 0.7 V for silicon and 0.3 V for Germanium junction), a small forward voltage is enough to completely eliminate the barrier. Once the

potential barrier is eliminated by the forward voltage, a large current starts flowing through the PN junction.

Reverse Bias:

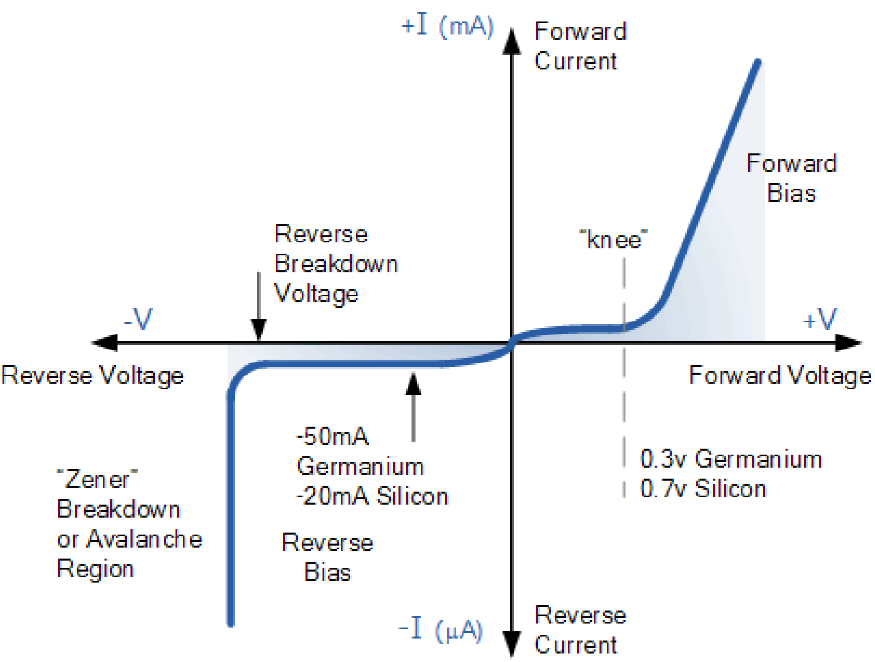


- When the positive terminal of the external battery is connected to the N-region and negative terminal to the p-region, the PN junction is said to be reverse biased.
- When the junction is reverse biased, the holes in the P-region are attracted by the negative terminal of the battery. Similarly the electrons in the N-region are attracted by the positive terminal of the external battery.
- This increases the width of the depletion layer and barrier potential (Vs).

- The increased barrier potential makes it very difficult for the majority carriers to diffuse across the junction. Thus there is no current due to majority carriers in a reverse biased PN junction. In other words, the PN junction offers very high resistance under reverse biased condition.

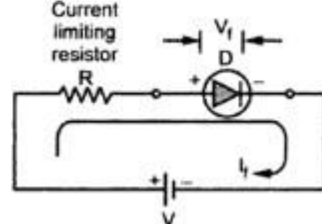
- In a reverse biased PN junction, a small amount of current (in µA) flows through the junction because of minority carriers. (i.e., electrons in the P-region and holes in the N region). The reverse current is small because the number of majority carrier in both regions is small.

- **V-I characteristics of PN-Junction Diode:**



- A graph between the voltage applied across the PN junction and the current flowing through the junction is called the V-I characteristics of PN junction diode. Fig. shows the V-I characteristics of PN junction diode.

Forward Characteristics:

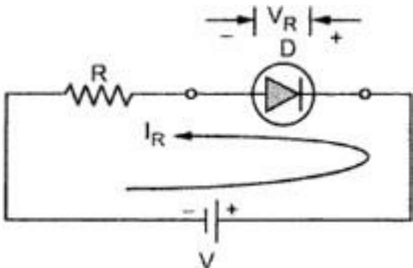


- Fig. shows the circuit arrangement for drawing the forward V-I characteristics of PN junction diode. To apply a forward bias, the +ve terminal of the battery is connected to Anode (A) and the negative terminal of the battery is connected to Cathode (K). Now, when supply voltage is increased the circuit current increases very slowly and the curve is non linear

- The slow rise in current in this region is because the external applied voltage is used to overcome the barrier potential (0.7 V for Si; 0.3V for Ge) of the PN junction' However once the potential barrier is eliminated and the external supply voltage is increased further, the current flowing through the PN junction diode increases rapidly . This region of the curve is almost linear. The applied voltage should not be increased beyond a certain safe limit, otherwise the diode will burnout.

- The forward voltage at which the current through the PN junction starts increasing rapidly is called by **knee voltage**. It is denoted by the letter V_B.

Reverse Characteristics:



- Fig shows the circuit arrangement for drawing the reverse V-I characteristics of PN junction diode. To apply a reverse bias, the +ve terminal of the battery is connected to cathode (K) and - ve terminal of the battery is connected to anode (A).

- Under this condition the potential buried at the junction is increased. Therefore the junction resistance becomes very high and practically no. current flows through the circuit. However in actual practice, a very small current (of the order of μA) flows in the circuit. This current is called reverse current and is due to minority carriers. It is also called as reverse saturation current (I). The reverse current increases slightly with the increase in reverse bias supply voltage.

- If the reverse voltage is increased continuously at one state breakdown of junction occurs and the resistance of the barrier regions falls suddenly. Consequently the reverse current increases rapidly to a large value. This may destroy the junction permanently. The reverse voltage at which the PN junction breaks is called as break down voltage.

6. Explain the temperature effects on characteristics. [Nov/Dec 2014][April 2015]

Diode terminal characteristics equation for diode junction current:

$$I = I_0(e^{\frac{v}{\eta v_T}} - 1)$$

Where V_T = Volt-equivalent of temperature. Its value is given by the relation, T/11600 where T is absolute temperature. At room temperature V_T is equal to 26 mV;

V –External voltage. It is positive for forward bias and negative for reverse bias

Io –Reverse saturation current, A

k - Boltzmann's constant (1.38x 10^{-23}J/K)

q - electron charge 1.6x10^{-19} C

η = empirical constant, 1 for Ge and 2 for Si

At room temperature, V_T is equal to 26 mV, substituting the value of V_T is

$$I = I_0(e^{\frac{40v}{\eta}} - 1)$$

When η =1

$$I = I_0(e^{\frac{40v}{}} - 1)$$

η =2

$$I = I_0(e^{\frac{20v}{}} - 1)$$

When diode is reverse biased,

$$I = I_0(e^{\frac{-V}{\eta v_T}} - 1)$$

$\approx I_o$

Temperature Effects on Diode

Temperature can have a marked effect on the characteristics of a silicon semiconductor diode as shown in Fig. 1.6. Temperature has following effects on the diode parameters,

- The cut in voltage decreases as the temperature increases. The diode conducts at smaller voltages at large temperature.
- The reverse saturation current increases as temperature increases.

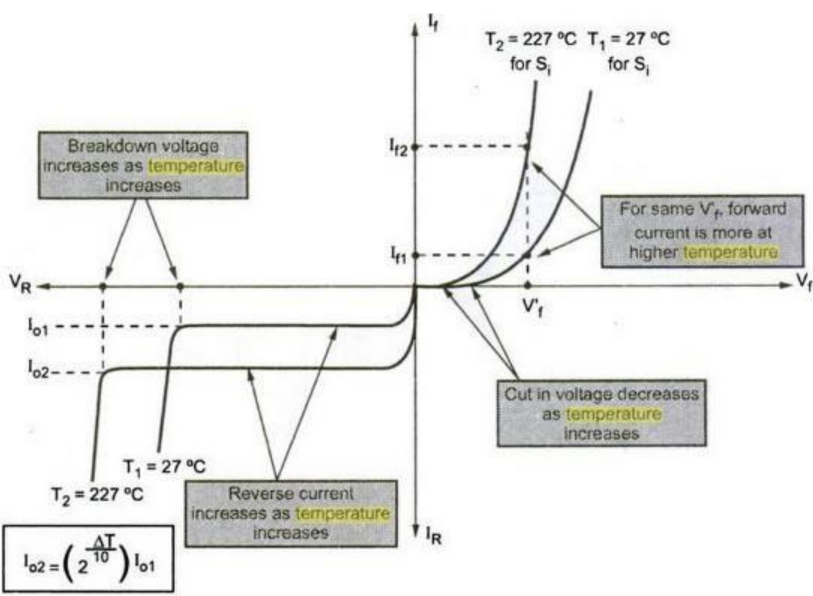
It has been found experimentally that the reverse saturation current Io will just about double in magnitude for every 10°C increase in temperature

$I_{02}=2^{(\frac{\Delta T}{10})}I_{01}$

I_{01}, I_{02} are the reverse current at T_1°C, T_2°C

$\Delta T = T_2 - T_1$.

- The voltage equivalent of temperature V_T also increases as temperature increases.
- The reverse breakdown voltage increases as temperature increases



- It is not common for a germanium diode with an Io in the order of 1 or 2 A at 25°C to have a leakage current of 100 A _ 0.1 mA at a temperature of 100°C.
- Typical values of Io for silicon are much lower than that of germanium for similar power and current levels.
- The result is that even at high temperatures the levels of Io for silicon diodes do not reach the same high levels obtained. For germanium—a very important reason that silicon devices enjoy a significantly higher level of development and utilization in design.
- Fundamentally, the open-circuit equivalent in the reverse bias region is better realized at any temperature with silicon than with germanium.
- The increasing levels of Io with temperature account for the lower levels of threshold voltage, as shown in Fig above
- Simply increase the level of Io in and not rise in diode current. Of course, the level of TK also will be increase, but the increasing level of Io will overpower the smaller percent change in TK.
- As the temperature increases the forward characteristics are actually becoming more ―ideal,‖

7. Explain static and dynamic resistance of diode [Nov/Dec 2015]

DC or Static Resistance

- A real diode does not behave a perfect insulator when reverse biased and does not behave as perfect conductor when forward biased.
- It means that diode has a definite value of resistance when forward biased.
- The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time.

- The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D as shown in Fig. below and applying the following Equation:

$$R_D = \frac{V_D}{I_D}$$

- The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics.
- The resistance levels in the reverse-bias region will naturally be quite high. Since ohmmeters typically employ a relatively constant-current source, the resistance determined will be at a preset current level (typically, a few mill amperes).

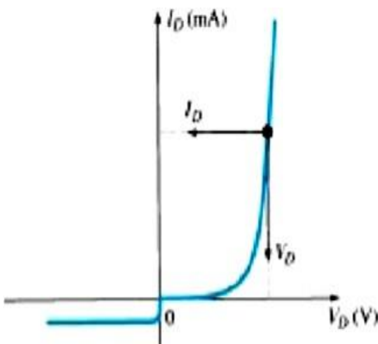


Figure 1.7 determining the dc resistance of a diode at a particular operating point.

AC or Dynamic Resistance

- It is obvious from Equation that the dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest.
- If a sinusoidal rather than dc input is applied, the situation will change completely.
- The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage as shown in Fig. 1.7.
- With no applied varying signal, the point of operation would be the Q-point appearing on Fig. 1.7 determined by the applied dc levels.
- The designation Q-point is derived from the word quiescent, which means ―still or unvarying.‖
- A straight-line drawn tangent to the curve through the Q-point will define a particular change in voltage and current that can be used to determine the ac or dynamic resistance for this region of the diode characteristics.

  In equation form,

$$r_d = \frac{\Delta v_d}{\Delta I_d}$$

  Where Δ is finite change in quantity.

- In addition to the forward resistance, the diode also possesses reverse resistance which is very large when compared to the forward resistance.
- Its value is in several meghohms.

The a.c resistance can be determined from the following:

Bulk resistance:

The resistance of the P and N type semiconductor materials of which diode is made of is known as body or bulk resistance. It also includes resistance introduced by the connection between the semiconductor material and the external metallic conductor also called contact resistance.

$$r_B = r_P + r_N$$

where

r_P-ohmic resistance of the P type semiconductor

r_N-ohmic resistance of the N type semiconductor

- This typically ranges from 0.1 ohm for high power devices to 2 ohm for low power device.

  Junction resitance:

  $r_j = 26/I_F$

where I_F is forward current in milliamperes.

From the relation it is observed that junction resistance is variable resistance.

The a.c resitance will be equal to the sum of junction and bulk resistance.

$$R_{ac} = r_j + r_B$$

8. Explain equivalent circuit of diode in detail.

- An equivalent circuit is a combination of elements properly chosen to best represent the actual terminal characteristics of a device, system, or such in a particular operating region.
- In other words, once the equivalent circuit is defined, the device symbol can be removed from a schematic and the equivalent circuit inserted in its place without severely affecting the actual behaviour of the system.
- The result is often a network that can be solved using traditional circuit analysis techniques.

Piecewise-Linear Equivalent Circuit

- One technique for obtaining an equivalent circuit for a diode is to approximate the characteristics of the device by straight-line segments.
- The resulting equivalent circuit is naturally called the piecewise-linear equivalent circuit. It should be obvious that the straight-line segments do not result in an exact duplication of the actual characteristics, especially in the knee region.
- However, the resulting segments are sufficiently close to the actual curve to establish an equivalent circuit that will provide an excellent first approximation to the actual behaviour of the device.
- The ideal diode is included to establish that there is only one direction of conduction through the device, and a reverse-bias condition will result in the open- circuit state for the device.

- Since a silicon semiconductor, diode does not reach the conduction state until V_D reaches 0.7 V with a forward bias, a battery V_T opposing the conduction direction must appear in the equivalent circuit as shown in Fig. 1.32.
- The battery simply specifies that the voltage across the device must be greater than the threshold battery voltage before conduction through the device in the direction dictated by the ideal diode can be established.
- When conduction is established, the resistance of the diode will be the specified value of r_{av}.

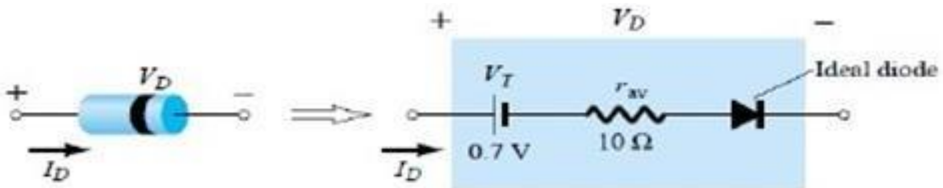


Figure 1.32 Components of the piecewise-linear equivalent circuit.

- The approximate level of r_{av} can usually be determined from a specified operating point on the specification sheet. For instance, for a silicon semiconductor diode, if I_F _ 10 mA (a forward conduction current for the diode) at V_D _ 0.8 V, we know for silicon that a shift of 0.7 V is required before the characteristics rise.

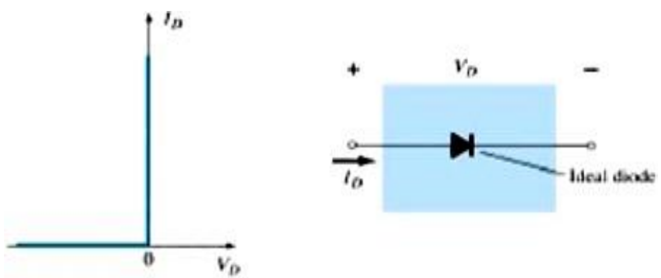


Figure 1.34 Ideal diode and its characteristics.

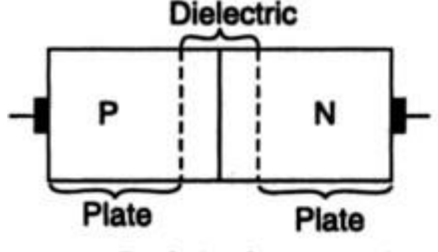
9. Explain transition and diffusion capacitance in detail

- Electronic devices are inherently sensitive to very high frequencies. Most shunt capacitive effects can be ignored at lower frequencies because the reactance X_C=1/2πfC is very large (open-circuit equivalent).
- This, however, cannot be ignored at very high frequencies. X_C will become sufficiently small due to the high value of **f** to introduce a low-reactance –shorting‖ path.
- Capacitors store electric charge in the form of electric field. This charge storage is done by using two electrically conducting plates (placed close to each other) separated by an insulating material called dielectric.

- The depletion region of the p-n junction diode has high resistance. Hence, the depletion region acts like the dielectric or insulating material. Thus, p-n junction diode can be considered as a parallel plate capacitor.
- In the p-n semiconductor diode, there are two capacitive effects to be considered.
- In the reverse-bias region we have the transition- or depletion region capacitance (C_T), while in the forward-bias region we have the diffusion (C_D) or storage capacitance.

Transition capacitance (C_T):

- When a PN junction is formed, a layer of positive and negative impurity ions called depletion layer is formed on either side of the junction.
- The depletion layer acts as dielectric medium between P region & N region.
- The P & N region on either side of the junction acts as two plates of a capacitor separated by a dielectric i.e. depletion layer.



Depletion layer capacitance.

- The capacitance formed in a junction area is called depletion layer capacitance.
- It is also called ***depletion region capacitance, space charge capacitance, transition region capacitance.***
- The capacitance of parallel plate capacitor is given by $\mathbf{C_T} = \frac{CA}{W}$

  $\mathcal{E}$ = Permittivity of material

  A = cross section area of junction

  W = Width of depletion layer
- When **no external voltage** is applied, the width of depletion region of PN diode is of the order of **0.5 microns** with a capacitance of **C_T = 20pF.**
- When reverse bias voltage applied to the p-n junction diode is increased, a large number of holes (majority carriers) from p-side and electrons (majority carriers) from n-side are moved away from the p-n junction. As a result, the width of depletion region increases whereas the size of p-type and n-type regions (plates) decreases.
- The capacitance of the reverse bias p-n junction diode decreases when voltage increases.
- The value of C_T ranges from **5 to 200pF.**
- Since the thickness of depletion layer depends on the amount of reverse bias, C_T can be controlled with the help of applied bias.

- This property of variable capacitance is used in varicap or varactor diode.

- This capacitance is voltage dependent and is given by

$$C_T = \frac{k}{Vk+VR}$$

Where,
V_K= Knee voltage,
V_R= Applied reverse voltage
K = Constant depending on semiconductor,

N=1/2 for alloy junction
= 1/3 for diffused junction

Diffusion capacitance (C_D):

- The capacitance that exists in a forward biased junction is called diffusion capacitance or storage capacitance, whose value is usually much larger than C_T which exists in a reverse biased junction.
- When forward bias voltage is applied to the p-n junction diode, electrons (majority carriers) in the n-region will move into the p-region and recombines with the holes. In the similar way, holes in the p-region will move into the n-region and recombines with electrons. As a result, the width of depletion region decreases.
- This depletion region acts like dielectric or insulator of the capacitor and charge stored at both sides of the depletion layer acts like conducting plates of the capacitor.
- Diffusion capacitance is proportional to diode forward current, I.
- The diffusion capacitance is given by $\mathbf{C_D} = \frac{I}{\eta V_T}$

τ = *the mean life time for holes & electrons*

The diffusion capacitance at low frequencies is given by the formula:

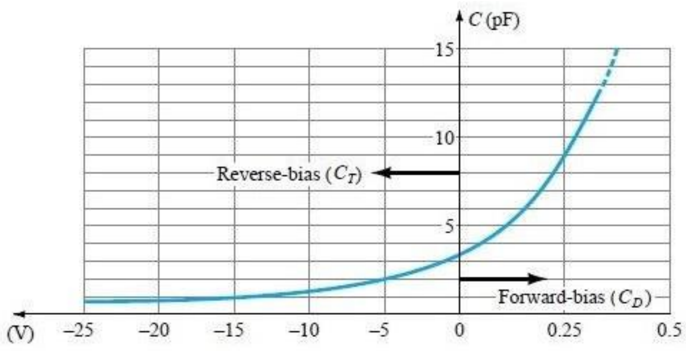
$$C_D = \tau^* g/2 \text{ (low frequency)}$$

The diffusion capacitance at high frequencies is inversely proportional to the frequency and is given by the formula:

$$C_D = g(\tau/2\omega)^{1/2}$$

- Diffusion capacitance is also defined as rate of change of injected charge with applied voltage i.e. $\mathbf{C_D = dQ/dV}$, where dQ represents the change in the number of minority carriers stored outside the depletion region when a change in voltage across the diode dV is applied.

- The effect of C_D is negligible for a reverse biased PN junction.
- As the value of C_D is inversely proportional to frequency, it is high at low frequencies and it decreases with the increase in frequency.
- The values of C_D ranges from **10 to 1000 pF.**



Transition and diffusion capacitance versus applied bias for a silicon diode.

10. Explain the drift and diffusion currents for PN diode. [April 2015]

Drift Current:-

In a conductor or Semiconductor, at room temperature, a free electron will move toward the positive terminal under the influence of electric field, But it will continually collide with atoms along the way. The presence of electric field does not stop the collisions and random motion, but it does cause the electron to drift in the direction of applied electric force. This current is known as Drift Current.

Diffusion Current:

- Consider a piece of semiconductor which is non uniformly doped. Due to such doping, one type of charge carriers occurs at one end of a semiconductor.
- The charge carriers are either electrons or holes.They have the same polarity or hence experience a force of repulsion between them.
- As a result the charge carriers move gradually from region of high carrier density to low carrier density. This process is called diffusion. The movement of charge carriers under the process of diffusion constitutes a current called diffusion current.

Without electric field non – uniform concentration of change

$J_p = - q D_p dp/dx$

$J_n = q D_n dn/dx$

Derive the current Equation of a Diode

$p_n(x) = P_{no} + P_n(o)\, e^{-x/LP}$

$p_n(x)$ = Concentration of holes at distance n

p_{no} = Thermal Equilibrium value

L_p = Diffusion length for holes in the a – material

$p_p = p_n e^{Vj/VT}$

Law of function Derivation

$p_{po} = p_{no}.e^{V0/VT}$

$p_{no} = p_n(0) \; e^{-V/VT}$

$p_n(o) = p_{no}. e^{V/VT}$

$I_{pn}(0) = qA\ D_p.\ p_{no}/L_p[e^{V/VT}-1]$

$I_{np}(0) = qA\ Dp.\ n_{po}/L_n\ [e^{V/VT}-1]$

$I = I_{np}(0) + I_{np}(0)$

$I = I_0 [e\ V/V_T-1]$

$I_0 = qA\ D_p.\ p_{no}/L_p + qA\ Dp.\ n_{po}/L_n$

11. Discuss the application of diode. [Nov/Dec 2014]

<u>Signal rectifier</u>

- If the input is not a sine wave, we usually do not think of it as a rectification in the sense as it was for power supply.
- For instance, we might want to have a series of pulses corresponding to the rising edge of a square wave (see Fig. 10, left hand side and right hand side of the capacitor C).
- While both, the rising and the falling, pulses are in the output after differentiation performed by CR circuit. The simplest way is to rectify the differentiated wave.

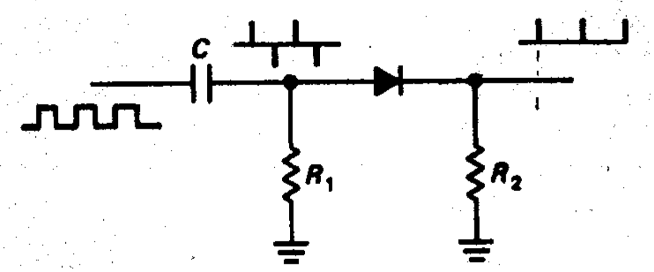


Fig.10. A series of pulses' rectifier.

We should remember about forward drop voltage of the diode: This circuit gives no output for signal for input smaller then, forward drop voltage, let us say 0.5 V pp (peak to peak). If this is a problem, there are various tricks that help to combat this limitation. For instance:

1. use Schottky diodes with smaller forward drop voltage (approximately 0.2V),
2. use so called circuit solution, which means modifying the circuit structure and compensating the drop,
3. Use matched-pair compensation, use transistors, FETs.

Diode gates

- Another application of diode is to pass the higher of two voltages without affecting the lower.
- A good example is battery backup, a method of keeping s device running (for instance a precision electronic clock) in case of power failure. Figure 11 shows a circuit that does the job.

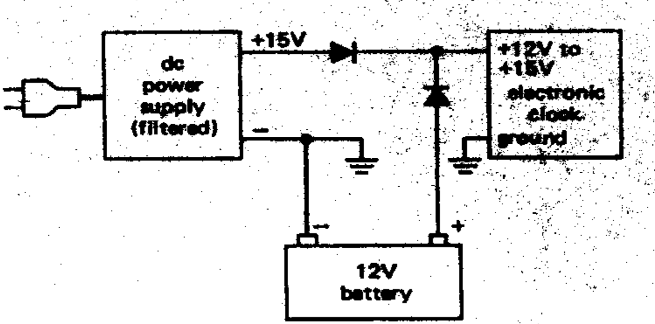


Fig.11. Diode OR gate, battery backup.

[**OR gate**: *The output of OR gate is HIGH if either input (or both) is HIGH. In general, gates can have any number of inputs. The output is LOW only if all inputs are LOW*].

1. The battery does nothing until the power fails.
2. Then the battery takes over the control, without interruption.

Diode clamps

Sometimes it is necessary to limit the range of signal (for instance not to exceed certain voltage limit and not to destroy a device). The circuit in Fig. 12 will accomplish this.

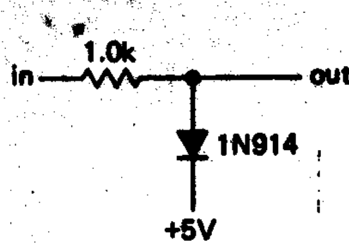


Fig.12. Diode voltage clamp.

- The diode prevents the output from exceeding ≅ 5.6V, with no effect on voltages smaller than this, including negative voltages.
- The only limitation is that the input must not be so negative that the reverse breakdown voltage is exceeded. Diode clamps are the standard equipment on all inputs in the CMOS family of digital logic (Complementary Metal Oxide Semiconductor).
- Without them, the delicate input circuits are easily destroyed by static electricity.

12. Describe diode switching with timing diagram. [Nov/Dec 2015]

- Diodes are often used in a switching mode.

- When the diode is switched from F.B to R.B, it takes a finite time to attain a steady state.The time consists of transient and interval of time before diode attains steady state.
- The behavior of diode during this time is called switching characteristics of diode.
- When the applied bias voltage to the PN diode is suddenly reversed in the opposite direction, the diode response reaches a steady state after an interval of time called ***recovery time.***
- The ***forward recovery time*** **(T_{fr})** is defined as the time required for forward voltage or current to reach a value after switching diode from its reverse to forward biased state.
- The ***reverse recovery time*** **(T_{rr})** is defined as the time required for reverse voltage or current to reach a value after switching diode from its forward to reverse biased state.
- Most diodes switch very quickly into the forward biased condition; however there is a longer turnoff time owing to the junction diffusion in reverse biased condition.
- When the PN junction diode is forward biased, the minority electron concentration in the P region is approximately linear.

Event 1:

Till t_1, the forward voltage V_F is applied and diode is forward biased.

Event2:

The applied voltage is suddenly reversed and reverse voltage $-V_R$ is applied.

- Because of stored electronic charge, the reverse current I_R is initially of the same magnitude as the forward current I_F.
- When the pulse switches from positive to negative, the diode conducts in reverse instead of switching off sharply.
- The reverse current I_R initially equals the forward current I_F , then it gradually decreases towards zero.
- The high level of reverse of reverse current occurs because at the instant of reverse bias there are charge carriers crossing the junction depletion region, and these must be removed.
- During the interval from t_1 to t_2 , the injected minority carrier have remained stored & hence this time interval is called ***storage time t_s***

Event 3:

- From T_2 onwards the diode voltage starts to reverse and the diode current starts decreasing.
- After the instant $t = t_3$ the diode gradually recovers and ultimately reaches the steady state.
- The time interval between t_2 & t_3 when the diode has recovered nominally is called ***transition time t_t.***
- The total time required by the diode is the sum of storage time and transition time,to recover completely from change of state is called reverse recovery time. The typical values of reverse **recovery time T_{rr}** for switching diode ranges from **4ns to 50ns.**

$$T_{rr} = t_s + t_t$$

- The switching time t_{rr} limits the operating frequency of the diode.

- To minimize the effect of reverse current the time period of operating frequency should be at least ten times t_{rr}

$$T=10t_{rr}$$

$$f_{max}=1/10t_{rr}$$

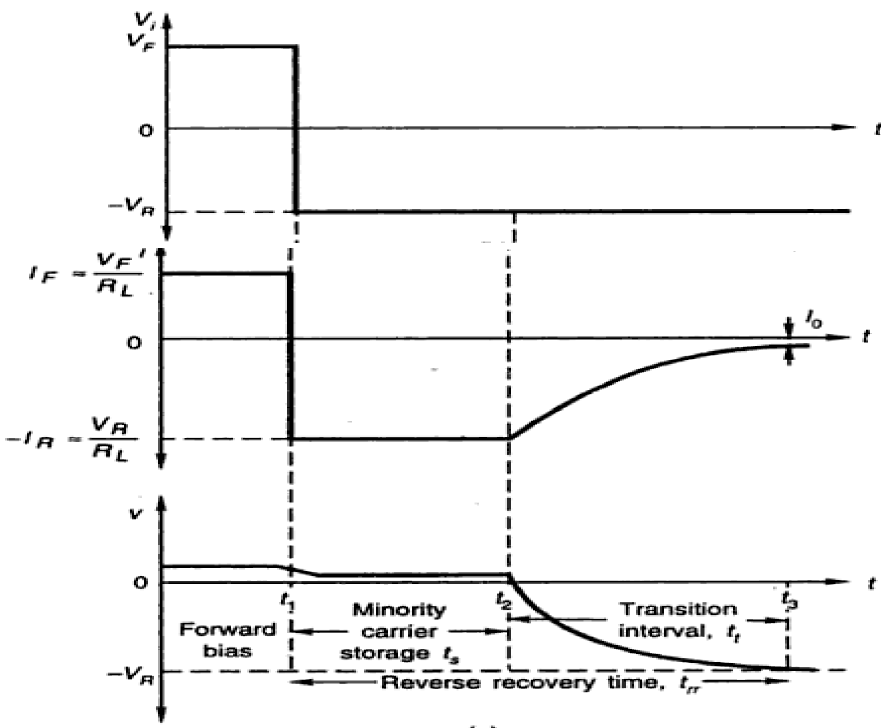


Figure: Switching characteristics of PN junction diode

(2marks)

1. **Define forbidden energy gap**

   The energy gap between the valence band and conduction band is defined as forbidden energy gap. For insulators. it is around 6ev, for semiconductors, its value is comparatively low. Germanium has energy gap 0.7ev and silicon has 1.1ev . For conductors, since conduction and valence bands are overlapping the energy gap is zero.

2. **What is doping? [Nov/Dec 2014]**

   The process of adding impurity to pure semiconductor is known as doping. As a result of it the characteristics of semiconductor is changed and hence the conductivity increases.

3. **Define Fermi level. [Nov/Dec 2014]**

   The Fermi level is defined as the maximum energy level, which is occupied by electron at absolute zero temperature. In P- type semiconductor the Fermi level will be above the top of the valence band. In N-type it lies below the bottom of the conduction band.

4. **What are donor and acceptor impurities?**
   Pentavalent impurities (Antimony, Arsenic) have five valence electrons. They can donate one excess electron to adjacent atoms to complete lattice structure, therefore they are called donor impurities.
   Trivalent impurities (Indium, Gallium) has three valence electrons. They have tendency to accept one electron from adjacent atoms to complete lattice structure, therefore they are known as acceptor impurities.

5. **State mass action law.**
   Mass action law states that in a semiconductor the product of the number of holes and the number of electrons is constant and is independent of the amount of donor and acceptor impurity doping.
   $np = n_i^2$
   where n= free electron concentration
   p= hole concentration; n_j = intrinsic concentration
6. **Define the term the drift current.**
   If a steady electric field is applied across a semiconductor, it causes the free electrons to move towards the positive terminal and the holes move towards the negative terminal of the battery. This combined effect causes a current flow in the semiconductor. The current produced in this manner is known as drift current.
   Drift current density due to electrons
   $J_n = q\, n\, \mu_n\, E$
   Drift current density due to holes
   $J_p = q\, p\mu_p\, E$
   J_n = Drift current density due to electrons
   J_p = Drift current density due to holes
   q = Charge of the carrier
   μ_n = Mobility of electrons
   μ_p = Mobility of holes
   E = Applied electric field strength.
7. **What is diffusion current? (Nov 2014)**
   In a semiconductor it is possible to have a non uniform distribution of carriers. A concentration gradient exists if the number of either holes or electrons is greater in one region as compared to the rest of the region. The holes and electrons then tend to move from a region of higher concentration to lower concentration region.
   This process is known as diffusion and the electric current produced due this process is known as diffusion current.
8. **What is a PN junction diode? [Nov/Dec 2015]**
   A PN junction diode is a two terminal device consisting of a PN junction formed either of Germanium or Silicon crystal. A PN junction is formed by diffusing P type material to one half side and N type material to other half side.
9. **Define and explain peak inverse voltage (PIV) (Nov 2013)**
   Peak inverse voltage is the maximum reverse voltage that can be applied to the PN junction without damage to the junction. If the reverse voltage across the junction exceeds to its peak inverse voltage, the junction may be destroyed due to excessive heat.

10. Differentiate drift and diffusion current

Drift current	Diffusion current
1. Developed due to potential gradient	Developed due to concentration gradient
2. Phenomenon found both in semiconductors and metals	Only in semiconductros
3. $J_n = qn\, \mu_n E$ $J_p = q\, p\, \mu_p E$	$J_n = q\, D_n\, dn / dx$ $J_p = q\, D_p\, dp / dx$

11. Define valence electron.
Electrons that are in shells close to nucleus are tightly bounced to the atom and have low energy. Whereas electrons that are in shells farther from the nucleus have large energy and less tightly bound to the atom. Electrons with highest energy level exist in the outermost shell of an atom. These electrons determine the electrical and chemical characteristic of each particular type of atom. These electrons are known as valence electrons.
12. What is meant by energy band?
In a single isolated atom, the electron in any orbit possesses define energy. Due to an interaction between atoms the electrons in a particular orbit of one atom have slightly different energy levels from electrons in the same orbit of an adjoining atom. This is due to the fact that no two electrons see exactly the same pattern of surrounding charges. Since there are billions of electrons in any orbit, slightly different energy levels form a cluster or band known as energy band.
13. What are conductors, Insulators and semiconductors?
A conductor is a material, which easily allows the flow of electric current. The best conductors are copper, silver, gold and aluminum.
An Insulator is a material that does not conduct electric current. In these materials valence electrons are tightly bound to the atoms.
A semiconductor is a material that has an electrical conductivity that lies between conductors and insulators. A semiconductor in it's pure state is neither a good conductor not a good insulator. The most common semiconductors are silicon, Germanium, and carbon.
14.What are the classifications of semiconductors?
Semiconductors are classified as intrinsic and extrinsic semiconductors. A pure semiconductor is called intrinsic semiconductor. A doped semiconductor is called extrinsic semiconductor.
15.How the extrinsic semiconductors are classified?
(a) n-type semiconductor
(b) p-type semiconductor
16.How an *n*-type semiconductor can be obtained?
A n-type semiconductor can be obtained by adding pentavalent impurities to an intrinsic semiconductor. These are atoms with five valence electrons. Typical examples for pentavalent atoms are Arsenic.Phosphorous, Bismuth and Antimony.
17.How a p-type semiconductor can be obtained?
A p-type semiconductor can be obtained by adding trivalent impurities to an intrinsic semiconductor. These are atoms with three valence electrons. Typical examples for trivalent atoms are boron(B),indium(In) and gallium(Ga).
18.What is depletion region?
When a pn junction is formed free electrons from the n-side diffuse across the junction, and fill the holes on the p-side and create positive ions. Similarly the holes from p-side diffuse across the junction and recombine with electrons in n-side and create negative ions. Since negative ions are created on p-side of the junction, the region close to the junction acquires a negative charge. Similarly the positive ions created on the n-side gives a positive charge near the junction. As these

charges build up a point is reached where the total negative charge in p-region repels any further diffusion of electrons (negatively charged particals) into the p-region (like charges repels) and the diffusion stops. At this point the positive ions on n-side and negative ions on p-side are immobile (fixed).They cannot serve as current carriers. That is the region is almost completely depleted of carriers. This region near the junction is called the depletion region. The width of the depletion region is about $1_{\mu m}(10^{-6}m)$.

19. What is barrier potential?

The intimate contact between p and n materials from a depletion layer near the junction.Since the depletion layer contains positive charges on the right side of the pn junction and negative ions on the left side of the pn-junction an electric field is formed. The electric field producers a barrier to the free flow of electrons in the n-region, and energy must be spent to move an electron through the electric field. That is an external energy must be applied to move an electro through the electric field. The external energy depends on the potential difference of the electric field across the depletion region. This potential difference which is required to move electrons through the electric field is known as barrier potential ($V_\circ$) and it is expressed in volts.

20.What is the barrier potential for Ge and Si?

The barrier potential for GE is 0.3V and for Si 0.7V.

21.What is meant by forward bias?

When the positive terminal of a battery is connected to p- side of the device and the negative terminal is connected to n-side of the device then the device is said to be forward biased. At forward bias, large current will flow in the range of milli amperes (10^{-3}A). Forward bias is equivalent to short circuit

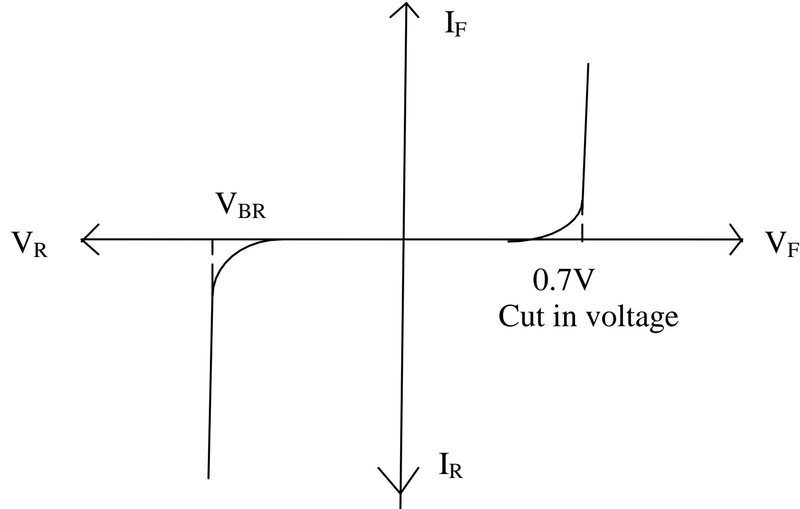
22. What is meant by reverse bias?

When the negative terminal of a battery is connected to p-side device and positive terminal is connected to n-side then the device is said to be reverse biased. At reverse bias, small current will flow in the range of micro amperes (10^{-6}). Reverse bias is equivalent to open circuit.

23. What is meant by break down voltage?

If the reverse biased voltage is increased, the velocity of minority charge carriers crossing the junction increases. These carriers acquire high kinetic energy and collide with the atom. As a result the valence electron in the atom observes sufficient energy and leave the parent atom. These additional carriers also get sufficient energy from the applied reverse biased and collide with other atom and generate some more carriers. This collision and generation of carriers is a cumulative effect, which result in large amount of reverse current. This phenomena, known as breakdown occurs at a particular reverse voltage for a pn junction. This known as reverse breakdown voltage.

24. Draw the V-I characteristics of a diode.



25. Define static and dynamic resistance of a diode.

The static resistance R_F of a diode is defined as the ratio V/I of the voltage to the current that can be obtained by finding the reciprocal of the slope of a line joining the operating point to the orgin. But it is not a useful parameter as the resistance varies widely with V and I. The dyanamic resistance is defined as the reciprocal of the slope of volt-ampere characteristics.

$$R_F = \frac{V_D}{I_D}$$

26. What are the applications of a diode.

In rectification, clampers, clippers, switching circuits, comparators, voltage doublers and diode gates.

27. Explain how a reverse biased pn junction exhibits a capacitor?

The width of the depletion layer can be controlled using reverse biased voltage. Since the depletion layer is an insulator, the pn junction can be thought of as a parallel plate capacitor and p and n regions act like plates of a capacitor (p-region positive plate, n-region negative plate).

28. Discuss how capacitance varies with reverse biased voltage.

The depletion region increases as reverse voltage applied to diode increases. Since capacitance varies inversely with dielectric thickness($C_T = \frac{EA}{w}$;as w increases c decreases), the junction capacitance will decrease as the voltage across pn junction increases.

29. Define knee voltage.

It is the forward voltage of a PN diode at which the current thorough the junction starts increasing rapidly.

30. Define breakdown voltage.

It is the reverse voltage of a PN junction diode at which the junction breaks down with sudden rise in the reverse current

31. Define transition capacitance of a diode.

Transition Capacitance (C_T) or Space-charge Capacitance: When a PN- junction is reverse-biased, the depletion region acts like an insulator or as a dielectric.

The P- and N-regions on either side have low resistance and act as the plates. Hence it is similar to a parallel-plate capacitor. This junction capacitance is called transition or space-charge capacitance (C_T).

It is given by $C_T = \varepsilon A/D$

Where, A = Cross-sectional area of depletion region.

D = Width (or) thickness of depletion region.

Its typical value is 40 pF.

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Subject Name: **ELECTRONIC DEVICES AND CIRCUITS** Subject Code: **EE T34**

UNIT – II BIPOLARJUNCTION TRANSISTORS

Construction and operation– NPN and PNP transistors– CB, CE and CC configurations– transistor characteristics and regions of operation–Specification sheet–Biasing of BJTs– operating point–stabilization of operating point–different biasing circuits and DC load line characteristics –Bias compensation techniques–thermal stability and thermal runaway.

(2 marks)

1. Why base is made thin in BJT? [Nov/Dec 2014]

Transistor consists of three portions namely emitter, base and collector. Among them base forms the middle part. It is very thin and lightly doped because it allows most of the emitter current carriers towards the collector. Since base is acting as an interface it doesn't need more area.

2. What is meant by biasing a transistor? Why is it necessary?[Nov/Dec 2015]

For normal operation base emitter junction should be forward biased and collector base junction should be reverse biased .The proper flow of zero signal collector current and the maintenance of collector-emitter voltage during the passage of signal is called the transistor biasing. The amount of biasing required is significant for the establishment of the operating or Q-point which decides the mode of operation.

3. Define the different operating regions of transistor. . [Nov/Dec 2014]

Active region: It is defined in which transistor collector junction is biased in reverse direction and emitter junction in forward direction.

Cutoff region: The region in which the collector and emitter junctions are both reverse-biased

Saturation region : The region in which both the collector and emitter junctions are forward biased.

4. Define Base width modulation (Early effect) . [Nov 2013]

In a CB configuration, an increase in collector voltage increases the width of the depletion region at the output junction diode. This will decrease the effective width of the base. This is known as early effect. Due to this effect recombination rate reduces at the base region and charge gradient is increased within the base.

5. Explain the significance of Base width modulation (Early effect) . [Nov 2013]

a) It reduces the charges recombination of electrons with holes in the base region, hence the current gain increases with the increase in collector -base voltage
b) The charge gradient is increased within base; hence the current due to minority carriers injected across emitter junction increases.

6. What are the three types of configurations? [Nov/Dec 2015]

Common base configuration, Common emitter configuration Common collector configuration

7. Among CB, CE, CC which is most important?

The CE configuration is important. The reasons

i) High current gain
ii) Output to input impedance ratio is moderate therefore easy coupling is possible between various transistor stages
iii) It finds excellent usage in audio frequency applications hence used in receivers and transmitters

8. Give the advantages of CE configuration. . [Nov 2013]

i. High output impedance

ii. High current gain

iii. High power gain

9. What is thermal runaway? [Nov 2013]

The reverse saturation current in a semiconductor doubles for every 100 C rise in temperature I as temperature increases the leakage current increases I and the collector current also increases. The increase in collector produces an increase in power dissipation at the collector - base junction. This I in turn further increases the temperature of the collector-base junction causing the collector current to further increase. This process may become cumulative and it is possible for the transistor to burn out. This process is known as Thermal runaway.

10. How thermal runaway can be avoided?

Thermal runaway can be avoided using a stabilization or heat sink with the transistor.

11. How a transistor is used as a switch?

A transistor should be operated in saturation and cutoff regions to use it as a switch .While operating in saturation region transistor carry heavy current hence considered as ON state. In cutoff it doesn't carry current and it is equivalent to open switch.

13. Which configuration is known as emitter follower and why it is named so?

CC configuration is known as emitter follower, whatever may be the signal applied at the input, may produce same signal at the output. In other words, the gain of the circuit is unity. So that the common collector circuit - the so called emitter follower is named as emitter follower. (Output follows the input)

14. Why do the output characteristics of CB transistor have a slight upward slope?

The emitter and collector are forward biased under the saturation region. Hence a small change in collector voltage causes a significant change in collector current .Therefore a slight upward slope is found in the output characteristics.

15. Compare the performance of CE, CB, CC

Parameters	**CB**	**CE**	**CC**
Current gain (A_i)	Low	High	High
Voltage gain (V_i)	High	High	Low
Input resistance (R_i)	Low	Medium	High
Output resistance (R_o)	High	Medium	Low

16. Compare BJT and JFET (May 2010)

BJT	**JFET**
Low input impedance	High input impedance
High Output impedance	Low output impedance

Bipolar device	Unipolar device
Noise is more	Less noise
Cheaper	Costlier
Gain is more	Gain is less
Current controlled device	Voltage controlled device

17. Mention the advantages of FET over BJT? (Nov 2013)

i) The noise level is very low in FET since there are no junctions.

ii) FET has very high power gain iii) Offers perfect isolation between input and output since it has very high input impedance.

iv) FET is a negative temperature coefficient device hence avoids thermal runaway.

18. Explain why an ordinary transistor is called bipolar?

Because the transistor operation is carried out by two types of charge carriers(majority and minority carriers),an ordinary transistor is called bipolar.

19. Why transistor is called current controlled device?

The output voltage, current and power is controlled by the input current in a transistor so it is called the current controlled device.

20. Why silicon type transistors are more used than germanium type?

Because silicon transistor has smaller cutoff current I_{CBO}, small variations in I_{CBO} due to variations in temperature and high operating temperature as compared to those in case of germanium type.

21. Why CC configuration is called a voltage buffer?

Because of its high input impedance and low output impedance, the common collector finds wide application as a buffer amplifier between a high impedance source and low impedance load. Its other name is emitter follower.

22. What do you mean by operating point?

Quiescent point is a point on the dc load line which represents V_{CE} and I_C in the absence of ac signal and variations in V_{CE} and I_C take place around this point where ac signal is applied.

23. Why heat sinks are used in power amplifiers? Heat sink is a specially designed metal sheet over which the power transistor is mounted so that it dissipates heat more effectively and protects the power transistor from overheating. It increases the area of contact with the atmosphere.

(11 MARKS)

1. With diagram explain construction and operation of NPN transistor. [Nov/Dec 2015]

- A **bipolar (junction) transistor** (BJT) is a three-terminal electronic device constructed of doped semiconductor material and may be used in amplifying or switching applications.
- Bipolar transistors are so named because their operation involves both electrons and holes.
- Charge flow in a BJT is due to bidirectional diffusion of charge carriers across a junction between two regions of different charge concentrations.
- By design, most of the BJT collector current is due to the flow of charges injected from a high-concentration emitter into the base where there are minority carriers that diffuse towards the collector and so BJTs are classified as minority-carrier devices.

Construction:

- The BJT consists of silicon (or germanium) crystal in which a thin layer of **N type** silicon is **sandwiched between** two **layers of P type** silicon. This transistor is referred to as **PNP.**
- Alternatively in a **NPN transistor**, a layer of **P type** material is **sandwiched** between **two layers of N type** material.
- The three terminals of the transistor are as follows:

Emitter-Heavily doped so that it can inject large charge carriers to the base.

Base-It is **lightly doped** and very thin and it passes most of the injected charge carriers from the emitter into the collector.

Collector-It is **moderately doped**

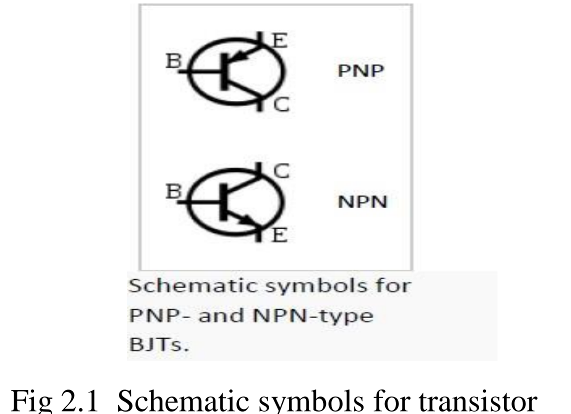


Fig 2.1 Schematic symbols for transistor

Operation:

Applying external voltage to a transistor is called biasing. In order to operate transistor properly as an amplifier, it is necessary to correctly bias the two PN junctions with external voltages. Depending upon external bias voltage polarities used, the transistor works in one of the three regions.

S.NO	REGION	EMITTER BASE	COLLECTOR BASE	OPERATION OF TRANSISTOR
1.	Active region	Forward biased	Reverse biased	Acts as an amplifier
2.	Cut-off region	Reverse biased	Reverse biased	Acts as an open switch

3.	Saturation region	Forward biased	Forward biased	Acts as a closed switch

To bias the transistor in its active region the emitter base junction is forward biased, while the collector-base junction in reverse-biased as shown in Fig 2.2.Fig 2.2.shows the circuit connections for active region for both NPN and PNP transistors.

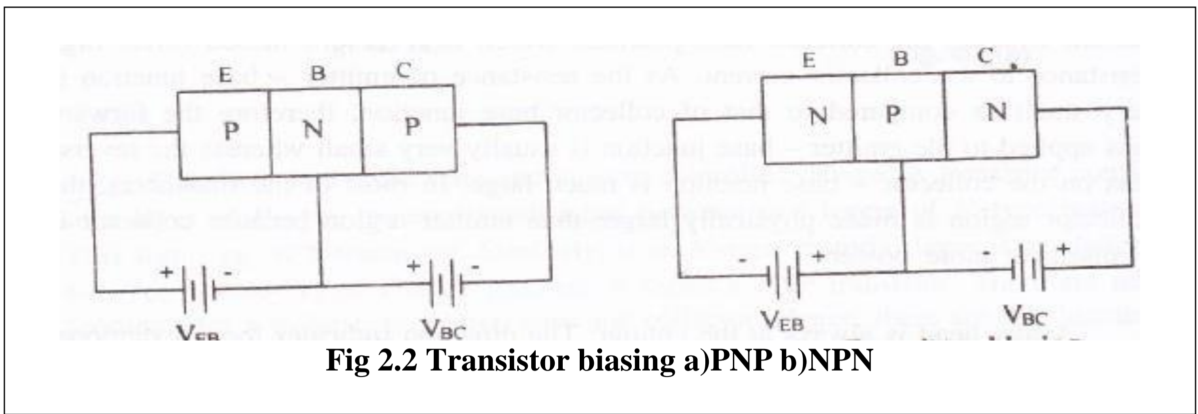


Fig 2.2 Transistor biasing a)PNP b)NPN

Operation of NPN transistor:

- As shown in fig 2.3 the NPN transistor is biased in the forward active mode. The emitter – base junction is forward biased only if V_{EB} is greater than barrier potential which is 0.7V for Si and 0.3 V for germanium.
- Forward bias applied to the emitter base junction of an NPN transistor causes a lot of electrons from the emitter region to cross over to the base region.
- This constitutes the emitter current I_E
- As the base is lightly doped with P-type impurity, the number of holes in the base region is very small and hence the number of electrons that combine with holes in the P – type base region is also very small.
- Hence a few electrons combine with holes to constitute a base current I_B.
- The remaining electrons (more than 95%) crossover into the collector region to constitute a collector current I_C.
- Thus the base and collector current summed up give the emitter current i.e. $I_E= (I_C+I_B)$.
- This collector current is also called as injected current because this current is produced due to electrons injected from the emitter region.
- There is also another component of collector current due to thermally generated carriers. This is called reverse saturation current and is quite small.
- The equation gives the fundamental relationship between the currents in a bipolar transistor circuit.
- Also, this fundamental equation shows that there are current amplification factors α and β in common base transistor configuration and common emitter transistor configuration respectively for the static (d.c) currents, and for small changes in the currents.

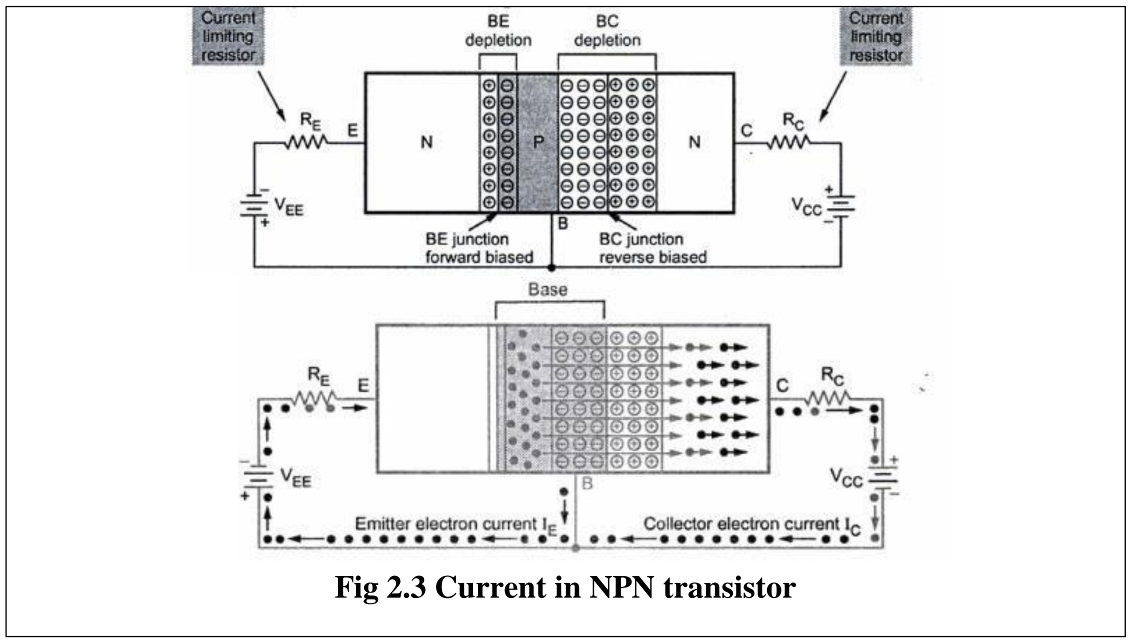


Fig 2.3 Current in NPN transistor

Large – signal current gain (α):

The large signal current gain of a common base transistor is defined as the ratio of the negative of the collector – current increment to the emitter – current change from cut off (I_E=0) to I_E,i.e.

$$\alpha = -\frac{(I_c - I_{CBO})}{I_E - 0}$$

where ,I_{CBO} (or I_{CO}) is the reverse saturation current flowing through the reverse biased collector – base junction. i.e. the collector to base leakage current with emitter open.

As the magnitude of I_{CBO} is negligible when compared to I_E, the above expression can be written as

$$\alpha = \frac{I_C}{I_E}$$

- Since I_C and I_E are flowing in opposite directions, α is always positive.
- Typical value of α ranges from 0.90 to 0.995.
- Also, α is not a constant but varies with emitter current I_E, collector voltage V_{CB} and the temperature.

Operation of PNP transistor:

- As shown in fig.2.4 the forward bias applied to the emitter- base junction of a PNP transistor causes a lot of hoses from the emitter regions to cross over to the base region as the base is lightly doped with N-type impurity.
- The number of electrons in the base regions is very small and hence the number of holes combined with electrons in the N – type base region is also very small. Hence a few holes combined with electrons to constitute a base current I_B.
- The remaining holes (more than 95%) cross over in to the collector region to constitute a collector current I_C. Thus the collector and base current when summed up gives the emitter current. I.e. I_E= (I_C+I_B).
- In the external circuit of the PNP bipolar junction transistor, the magnitudes of the emitter current I_E, the base current I_B and the collector current I_C are related by

$$I_E=I_C+I_B$$

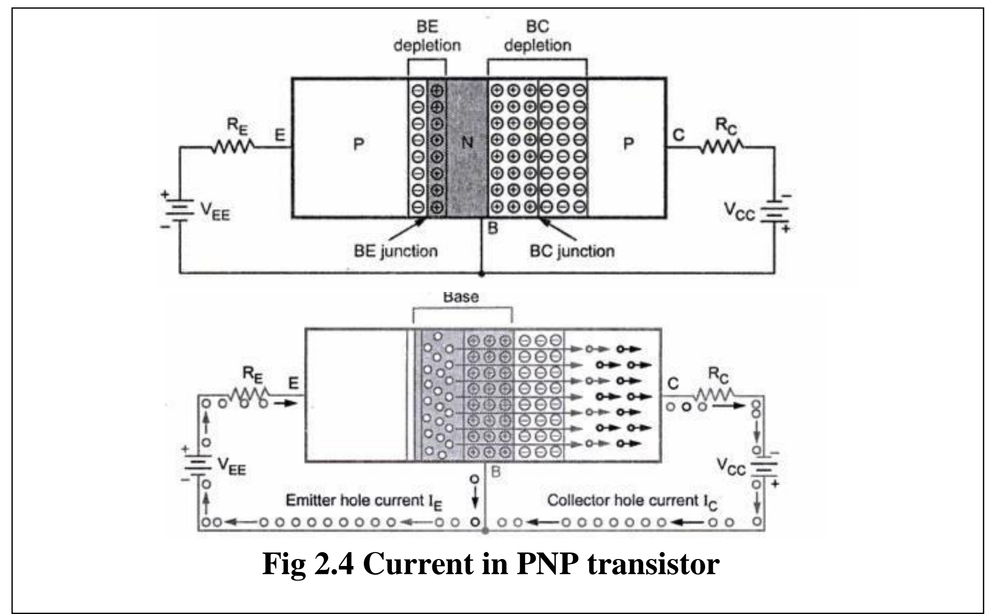
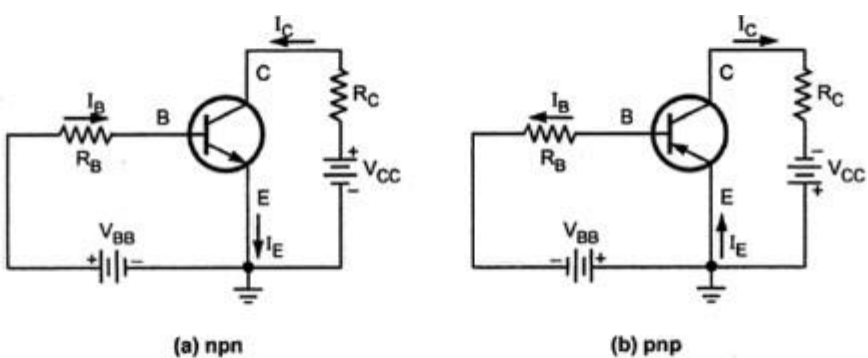


Fig 2.4 Current in PNP transistor

2. Explain the input and output of a transistor in CE configuration. Discuss the parameters and various regions involved in it.[Nov/Dec 2014]



The input is applied between base and emitter, and output is taken from collector and emitter. Here the emitter of transistor is common to both input and output circuits and hence the name common emitter configuration.

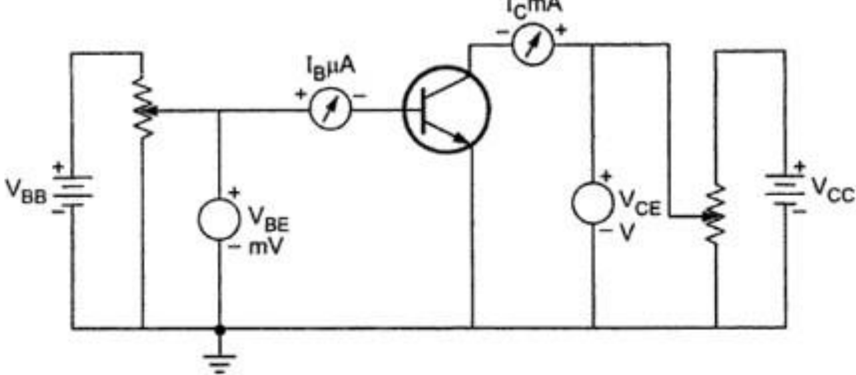
Here, $I_c = \beta_{dc} I_B + [1+\beta_{dc}] I_{CBO}$ where $\beta_{dc} = \frac{\alpha_{dc}}{1-\alpha_{dc}}$

The term "$(\beta_{dc}+1) I_{CBO}$" is the **reverse leakage current** in common-emitter configuration. It is designated as I_{CEO}

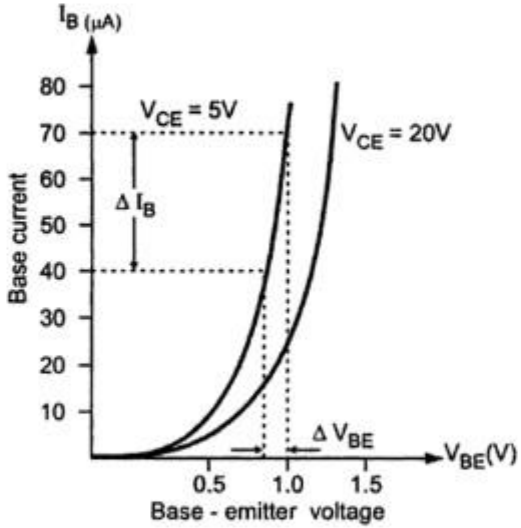
$$I_{CEO} = (\beta_{dc}+1) I_{CBO}$$

Neglecting I_{CBO} we have

$$I_C = \beta_{dc} I_B \quad \text{and} \quad I_E = I_B + I_C = (1+\beta_{dc}) I_B$$



Input Characteristic:



- The curve between input current I_B and input voltage V_{BE} at constant collector emitter voltage V_{CE}.
- After the cut in voltage the base current increases rapidly with small increase in base emitter voltage. It means the dynamic input resistance is small in CE configuration.
- It is the ratio of change in emitter to base voltage (ΔV_{BE}) to the corresponding change in emitter current (ΔI_B) for a constant collector to base voltage (V_{CE}).
- $R_i = \frac{\Delta V_{BE}}{\Delta I_B}$ at constant V_{CE}
- For a fixed value of V_{BE} , base current decreases as V_{CE} is increased. A larger value of V_{CE} results in large reverse bias at collector base p-n junction.
- This reduces the depletion region and reduces the effective width of the base. Hence there are fewer recombination in the base region reducing the base current.

Output characteristics:

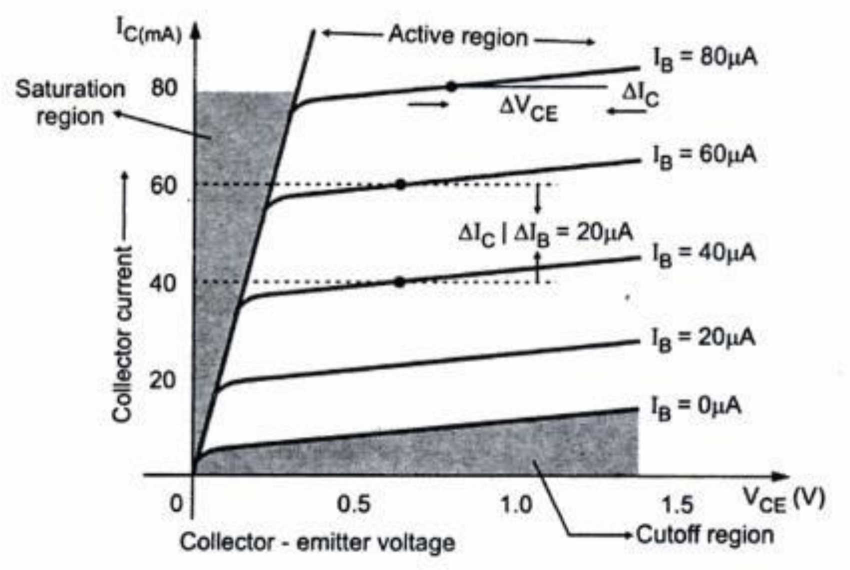


Fig. 5.28 Output characteristics of the transistor in CE configuration

2. The value of β of the transistor can be found at any point on the characteristics by taking the ratio I_C to I_B at that point, i.e. $\beta = \beta_{dc} = \frac{I_C}{I_B}$. This is known as DC beta

for the transistor. For a fixed value of V_{CE}, if we take the ratio of small change in I_C, ΔI_C to small change in I_B, ΔI_B, we get AC beta;

$$\beta_{ac} = \left. \frac{\Delta I_C}{\Delta I_B} \right|_{\Delta V_{CE}=0} \qquad \text{... (5.19)}$$

Generally dc and ac values of beta of the transistor are nearly equal.

3. From the output characteristics we can see that change in collector-emitter voltage (ΔV_{CE}) causes the little change in the collector current (ΔI_C) for constant base current I_B. Thus the output dynamic resistance is high in CE configuration.

$$r_o = \left. \frac{\Delta V_{CE}}{\Delta I_C} \right|_{I_B = \text{constant OR } \Delta I_B = 0} \qquad \text{... (5.20)}$$

4. The output characteristics of common emitter configuration consists of three regions : Active, Saturation, and Cut-off.

(1) Active Region:

Active region : The region where the curves are approximately horizontal is the "active" region of the CE configuration. In the active region, the collector junction is reverse biased. As V_{CE} is increased, reverse bias increases. This causes depletion region to spread more in base than in collector, reducing the chances of recombinations in the base. This increases the value of α.

- If α_{dc} is truly constant then I_C would be independent of V_{CE}.

- But because of early effect, α_{dc} increases by 0.1% (0.001) e.g. from 0.995 to 0.996 as V_{CE} increases from a few volts to 10V. Then β_{dc} increases from 0.995 / (1-0.995) = 200 to 0.996 / (1-0.996) = 250 or about 25%.
- This shows that small change in a reflects large change in b. Therefore the curves are subjected to large variations for the same type of transistors.

(2) Cut Off:

- Cut off in a transistor is given by $I_B = 0$, $I_C = I_{CO}$. A transistor is not at cut off if the base current is simply reduced to zero (open circuited) under this condition,

$$I_C = I_E = I_{CO} / (1-\alpha_{dc}) = I_{CEO}$$

- The actual collector current with base open is designated as I_{CEO}. Since even in the neighborhood of cut off, a $_{dc}$ may be as large as 0.9 for Ge, then I_C=10 I_{CO}(approximately), at zero base current.
- Accordingly in order to cut off transistor it is not enough to reduce I_B to zero, but it is necessary to reverse bias the emitter junction slightly. It is found that reverse voltage of 0.1 V is sufficient for cut off a transistor. In Si, the α_{dc} is very nearly equal to zero, therefore, $I_C = I_{CO}$.
- Hence even with I_B= 0, $I_C = I_E = I_{CO}$ so that transistor is very close to cut off. In summary, cut off means $I_E = 0$, $I_C = I_{CO}$, $I_B = -I_C = -I_{CO}$, and V_{BE} is a reverse voltage whose magnitude is of the order of 0.1 V for Ge and 0 V for Si.
- In this region both the junctions of the transistor are reverse biased.

(3)Saturation Region:

- If V_{CE} is reduced to a small value such as 0.2V,then collector base junction becomes forward biased ,since the emitter base junction is already F.B by 0.7V.When both the junctions are forward biased the transistor operates in this region and the value ranges between 0.1 V to 03 V.

3. Explain the input and output of a transistor in CB configuration. Discuss the parameters and various regions involved in it.

- This configuration is also called as grounded base configuration.
- In this case the input is connected between the emitter and base while the output is taken across the collector and base.
- Thus the base of the transistor is common to both input and output circuits and hence the name, common base configuration. The common base circuit arrangement for NPN transistors is shown in Fig.2.5

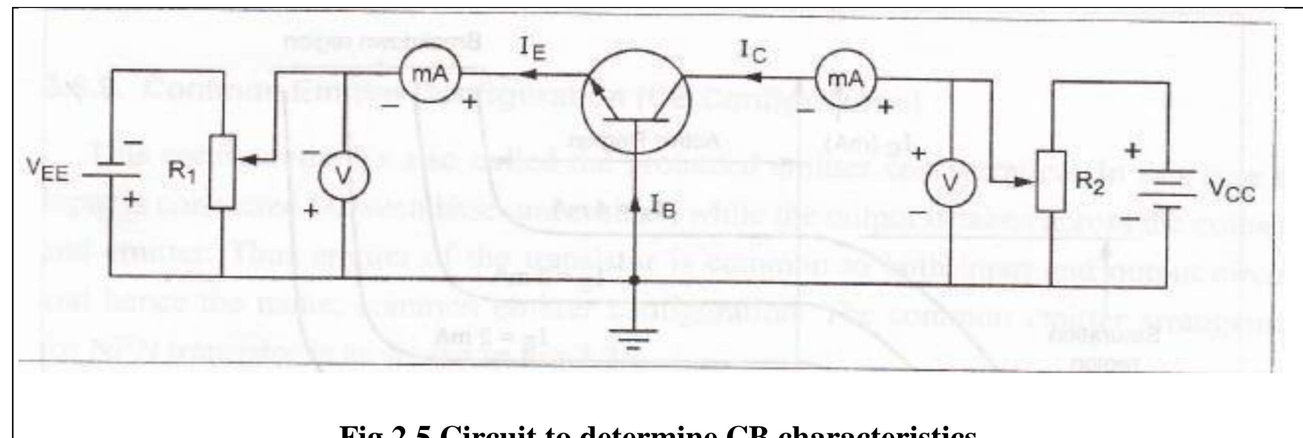
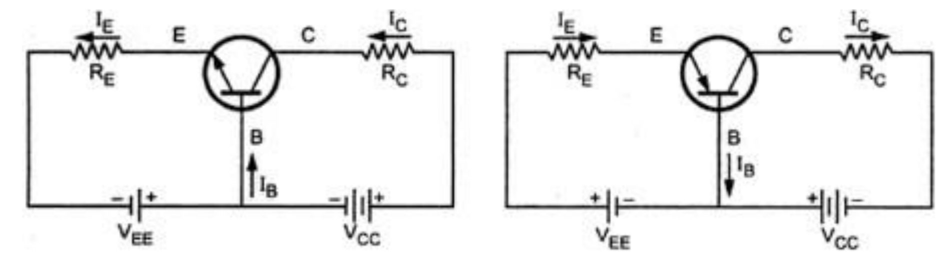


Fig 2.5 Circuit to determine CB characteristics



Current Amplification Factor (α):

The current amplification factor is defined as the ratio of changes in Collector current (ΔI_C) to the change in emitter current (ΔI_E) when the collector to base voltage (V_{CB}) is maintained at a constant value.

$$\alpha = (\Delta I_C) / (\Delta I_E) \text{ (at constant } V_{CB})$$

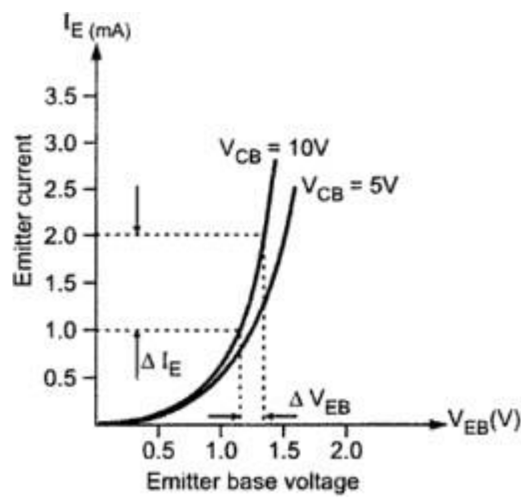
The value of α is always less than unity. The practical value of transistors lies between 0.95 and 0.99.

The circuit arrangement for determining the characteristics of a common base NPN transistors is shown in Fig 2.5.In this circuit, the collector to base voltage (V_{CB}) can be varied by adjusting the potentiometer R_2. The emitter to base voltage (V_{EB}) can be varied by adjusting the potentiometer R_l. The DC voltmeters and DC milliammeters are connected in the emitter and collector circuits to measure the voltages and currents

1. **Input Characteristics:**

The curves plotted between the emitter current (I_E) and the emitter to base voltage (V_{EB}) at constant collector to base voltage (V_{CB}) are known as input characteristics of a transistor in common base configuration.

- The collector base voltage (V_{CB}) is kept constant at zero volt and emitter current is increased from zero in suitable steps by increasing emitter to base voltage (V_{EB}).



- When V_{CB} is equal to zero and emitter-base junction is forward biased, the junction behaves as a forward biased diode so that the emitter current increases rapidly with small increase in emitter-base (V_{EB}).It means the input resistance is very small.
- **Input Resistance (R_i):**It is the ratio of change in emitter to base voltage (ΔV_{EB}) to the corresponding change in emitter current (ΔI_E) for a constant collector to base voltage (V_{CB}).
  - $R_i = \frac{\Delta V_{EB}}{\Delta I_E}$ at constant V_{CB}
- When V_{CB} is increased keeping V_{EB} constant, the width of the base region will decrease. This effect results in increase of I_E .Thus the curves shift towards the left as V_{CB} is increased.
- The width of the base region occupied by charge particles is known as electrical width of the base region. When V_{CB} increases the width of the depletion region in base region also increases which reduces the electrical base width. This is called early effect or base width modulation.

2. **Output Characteristics:**

- The curve plotted between the collector current (I_C) and the collector to base voltage (V_{CB}) at constant emitter current (I_E) are known as output characteristics of a transistor is common base configuration. The curves are known as the output or collector or static characteristics.

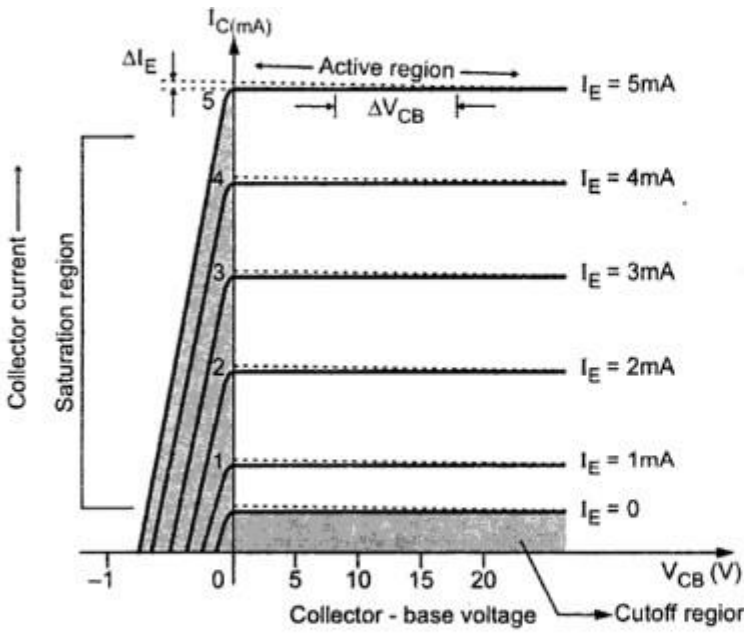


Fig. 5.19 CB output characteristics

The output characteristics are as shown in Fig. and it can be divided into three important regions namely (i) Saturation region (ii) Active region (iii) Cut-off region.

(1). Active region:

- In this region the collector base junction is reverse biased and the emitter base junction is forward biased.
- In this region collector current is approximately equal to emitter current and transistor works as an amplifier.
- Consider first that the emitter current is zero. Then the collector current is small and equals the reverse saturation current I_{CO} of the collector junction considered as a diode.
- If the forward current I_B is increased, then a fraction of I_E ie. $\alpha_{dc}I_E$ will reach the collector.
- In the active region, the collector current is essentially independent of collector voltage and depends only upon the emitter current.
- This provides very high dynamic output resistance which is the ratio of change in collector base voltage to the resulting change in collector current at constant emitter current.
- $V_O = \frac{\Delta V_{CB}}{\Delta I_C}$ at constant I_E
- Because a_{dc} is, less than one but almost equal to unity, the magnitude of the collector current is slightly less that of emitter current.
- The collector current slightly increases with voltage. This is due to early effect.
- At higher voltage collector gathers in a few more electrons.

- This reduces the base current. The difference is so small, that it is usually neglected. If the collector voltage is increased, then space charge width increases; this decreased the effective base width.
- Then there is less chance for recombination within the base region.
- It means that the circuit has very high output resistance about 500 K Ω.

(2). Saturation region:

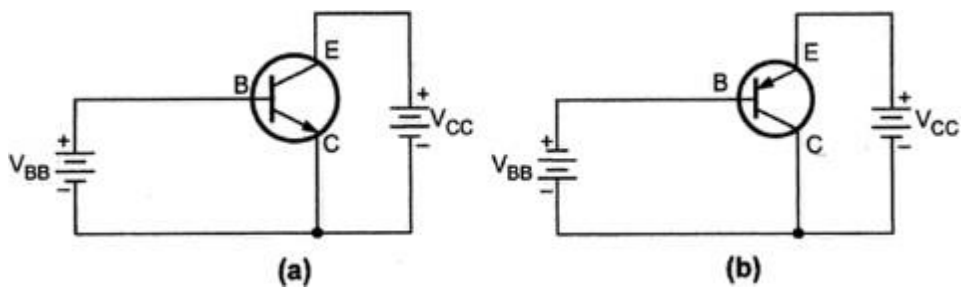
- The region to the left of the ordinate $V_{CB} = 0$, and above the $I_E = 0$, characteristic in which both emitter and collector junction are forward biased, is called saturation region.
- When collector diode is forward biased, there is large change in collector current with small changes in collector voltage.
- A forward bias means, that p is made positive with respect to n, there is a flow of holes from p to n. This changes the collector current direction.
- If diode is sufficiently forward biased the current changes rapidly. It does not depend upon emitter current.

(3). Cut off region:

- The region below $I_E = 0$ and to the right of V_{CB} for which emitter and collector junctions are both reversed biased is referred to cutoff region.
- The characteristics $I_E = 0$, is similar to other characteristics but not coincident with horizontal axis.
- The collector current is same as I_{CO}. I_{CBO} is frequently used for I_{CO}. It means collector to base current with emitter open. This is also temperature dependent.

4. Explain the input and output of a transistor in CC configuration. Discuss the parameters and various regions involved in it.

- The input is applied between base and collector, and output is taken from emitter and collector. Here the collector of transistor is common to both input and output circuits and hence the name common collector configuration



- The common emitter configuration has a current gain approximately equal to the β value of the transistor itself. In the common collector configuration the load resistance is situated in series with the emitter so its current is equal to that of the emitter current.

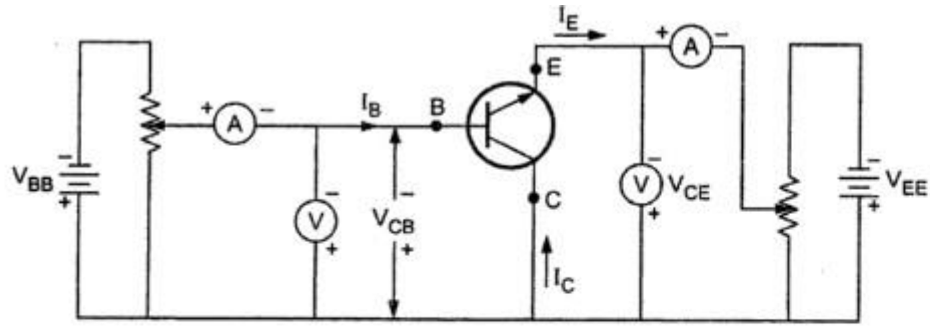
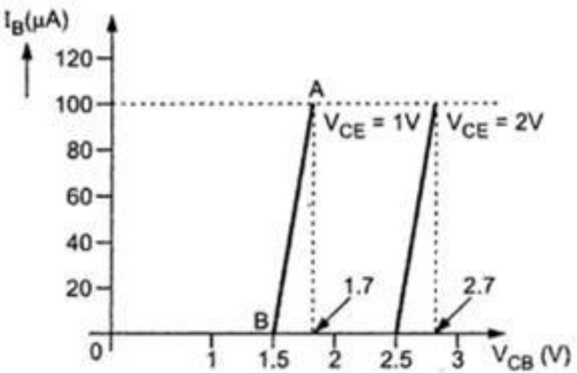


Fig. 5.38 Experimental setup for plotting CC characteristics

Input characteristics:



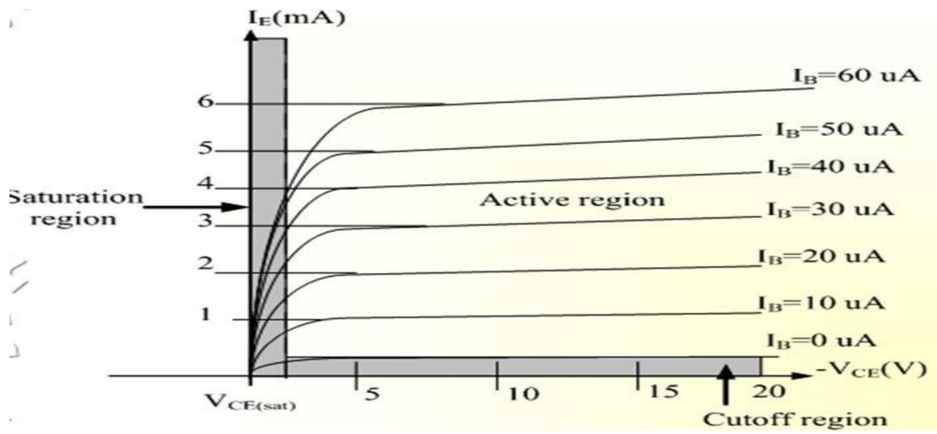
i. The input current I_B is plotted on the Y axis and the input voltage V_{CB} is plotted on the X axis for a constant output voltage V_{CE}.

ii. The base emitter junction is not forward biased upto V_{CB} =1.5volt. Therefore the base current is zero upto V_{CB} =1.5 volt at constant V_{CE} of 1volt.

iii. Then it increases rapidly as V_{CB} is inceased beyond 1.5volt. This is because junction V_{CB} is more and more forward biased.

iv.The input voltage V_{CB} is largely determined by the level of collector to emitter voltage V_{CE}

Output Characteristics:



i. It is a graph of output current I_E vs output voltage V_{EC} at constant value of input current I_B.

ii. Biasing of the 2 junctions of a transistor is done as follows.

Sl. No.	Region of operation	Base emitter junction	Collector base junction
1.	Cutoff region	Reverse biased	Reverse biased
2.	Active region	Forward biased	Reverse biased
3.	Saturation region	Forward biased	Forward biased

iii. The region below the curve for $I_B = 0$ is called cutoff region. In the active region, at a fixed value of V_{EC} if I_B is increased, it will cause I_E to increase substantially. In the saturation region, emitter current increases rapidly with increase in V_{EC}.

<u>The Common Collector Current Gain</u>

$$I_E = I_C + I_B$$

$$A_i = \frac{I_E}{I_B} = \frac{I_C + I_B}{I_B}$$

$$A_i = \frac{I_C}{I_B} + 1$$

$$A_i = \beta + 1$$

5. Explain about different Biasing compensation techniques.

This method of transistor compensation uses temperature sensitive resistive elements, thermistors rather than diodes or transistors. It has a negative temperature coefficient, its resistance decreases exponentially with increasing temperature as shown in the Fig. 6.38.

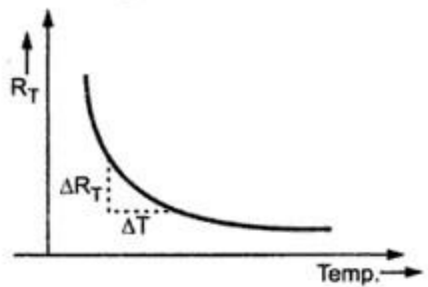
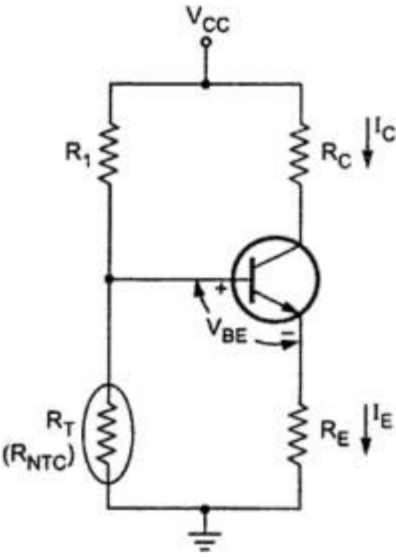


Fig. 6.38 Temperature Vs R_T resistance of thermistor

Slope of this curve = $\frac{\partial R_T}{\partial T}$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is negative. So we can say that thermistor has negative temperature coefficient of resistance (NTC).

Fig. 6.39 shows thermistor compensation technique.



As shown in Fig. 6.39, R_2 is replaced by thermistor R_T in self bias circuit.

With increase in temperature, R_T decreases.

Hence voltage drop across it also decreases. This voltage drop is nothing but the voltage at the base with respect to ground. Hence, V_{BE} decreases which reduces I_B. This behavior will tend to offset the increase in collector current with temperature.

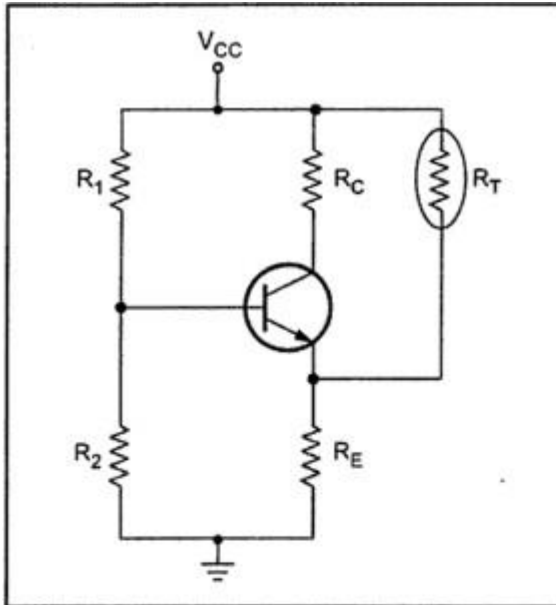


Fig. 6.40 Thermistor compensation technique

We know, from equation 6.9

$$I_C = \beta I_B + (1+\beta)I_{CBO}$$

In this equation, there is increase in I_{CBO} and decrease in I_B which keeps I_C almost constant.

Fig. 6.40 shows another thermistor compensation technique. Here, thermistor is connected between emitter and V_{CC} to minimize the increase in collector current due to changes in I_{CO}, V_{BE}, or β with temperature.

I_C increases with temperature and R_T decreases with increase in temperature. Therefore, current flowing through R_E increases, which increases the voltage drop across it. E – B junction is forward biased. But due to increase in voltage drop across R_E, emitter (N– type for NPN transistor) is made more positive, which reduces the forward bias voltage V_{BE}. Hence, base current reduces.

I_C is given by,

$$I_C = \beta I_B + (\beta + 1)I_{CBO}$$

As I_{CBO} increases with temperature, I_B decreases and hence I_C remains fairly constant.

6.7.3 Sensistor Compensation Technique

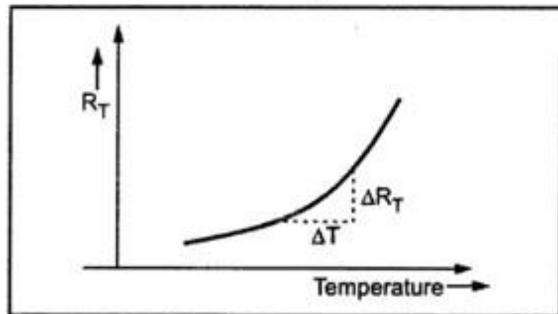


Fig. 6.41 Temperature Vs resistance of sensistor, R_T

This method of transistor compensation uses temperature sensitive resistive element, sensistors rather than diodes or transistors. It has a positive temperature coefficient, its resistance increases exponentially with increasing temperature as shown in the Fig. 6.41.

$$\text{Slope of this curve} = \frac{\partial R_T}{\partial T}$$

$\frac{\partial R_T}{\partial T}$ is the temperature coefficient for thermistor, and the slope is positive.

So we can say that sensistor has positive temperature coefficient of resistance (PTC)

Fig. 6.42 shows sensistor compensation technique.

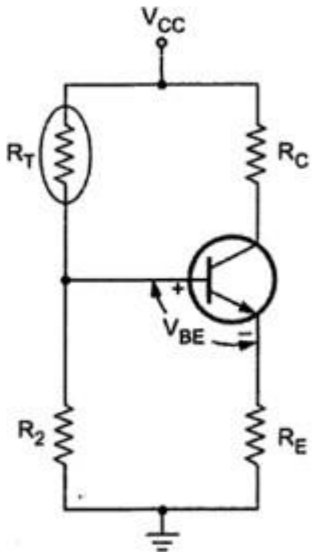
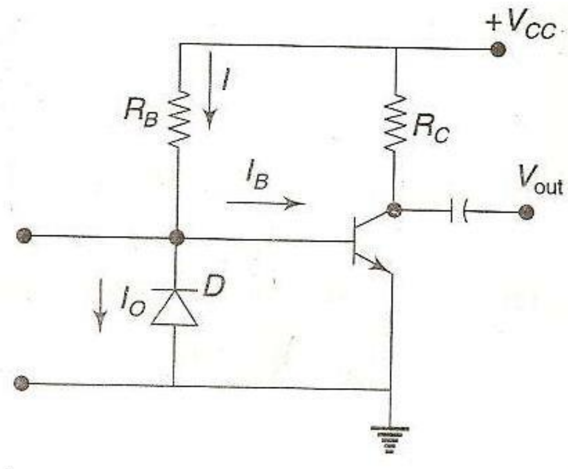


Fig. 6.42 Sensistor compensation technique

As shown in Fig. 6.42, R_1 is replaced by sensistor R_T in self bias circuit. Now, R_T and R_2 are the two resistors of the potential divider.

As temperature increases, R_T increases which decreases the current flowing through it. Hence current through R_2 decreases which reduces the voltage drop across it. Voltage drop across R_2 is the voltage between base and ground. So V_{BE} reduces which decreases I_B. It means, when I_{CBO} increases with increase in temperature, I_B reduces due to reduction in V_{BE}, maintaining I_C fairly constant.

3) Diode bias compensation



$I_R = I_D + I_B$ (I_D is reverse saturation Current increases with temp.)

When temperature increases, IC increases at the time, I_D also increases, making I_B to Reduce and controlling I_C.

6. Explain thermal runaway

6.8 Thermal Runaway

The maximum average power $P_{D(max)}$ which a transistor can dissipate depends upon the transistor construction and may lie in the range from a few milliwatts to 200 W.

As mentioned earlier, the power dissipated within a transistor is predominantly the power dissipated at its collector base junction.

Thus maximum power is limited by the temperature that the collector-base junction can withstand. For silicon transistor this temperature is in the range 150 to 225 °C, and for germanium it is between 60 to 100 °C. The collector-base junction temperature may rise because of two reasons :

1. Due to rise in ambient temperature
2. Due to self heating.

The self heating can be explained as follows :

The increase in the collector current increases the power dissipated at the collector junction. This, in turn further increases the temperature of the junction and hence increase

in the collector current. The process is cumulative and it is referred to as **self heating**. The excess heat produced at the collector base junction may even burn and destroy the transistor. This situation is called 'Thermal runaway' of the transistor.

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Subject Name: **ELECTRONIC DEVICES AND CIRCUITS** Subject Code: **EE T34**

UNIT-III: FIELD EFFECT TRANSISTOR

Construction–drain and transfer characteristics–Shockley's equation–comparison between JFET and BJT–MOSFET–depletion type and enhancement types–Biasing of FETs–biasing circuits.

(2 marks)

1. **Compare BJT and JFET (May 2014)**

BJT	**JFET**
Low input impedance	High input impedance
High Output impedance	Low output impedance
Bipolar device	Unipolar device
Noise is more	Less noise
Cheaper	Costlier
Gain is more	Gain is less

Current controlled device	Voltage controlled device

2. Mention the advantages of FET over BJT? (Nov 2013)

i) The noise level is very low in FET since there are no junctions.

ii) FET has very high power gain

iii) Offers perfect isolation between input and output since it has very high input impedence.

iv) FET is a negative temperature coefficient device hence avoids thermal runaway.

3. What is FET?

A field effect device in which (FET) is a three terminal semiconductor device in which current conduction is by one type of carriers (either holes or electrons) and is controlled by an electric field.

4. Define drain resistance of JFET?

Drain resistance (rd) is defined as the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in drain current (~Id) at constant gate to source voltage (V_{gs}) .$r_d = (\Delta V_{ds}) / (\Delta I_d)$ at constant V_{gs}

5. Define transconductance of JFET.

Transconductance (G_m) is defined as the ratio of small change in drain current (ΔId) to the corresponding change to gate source (ΔV_{gs}) at constant drain to source voltage (V_{ds})'

$$G_m = (\Delta Id) / (\Delta V_{gs}) \text{ at constant } V_{ds}$$

6. Define amplification factor of JFET? (May 2014)

Amplification factor (μ) is defined as the ratio of small change in drain to source voltage (ΔV_{ds}) to the corresponding change in gate to source voltage (ΔV_{gs}) at a constant drain current Id

$$\mu = (\Delta V_{ds}) / (\Delta V_{gs}) \text{ at constant } I_d$$

7. Write down the relationship between various FET parameters.

Amplification factor (μ)= Transconductance (g_m) x Drain resistance (r_d)

8. What are the applications of FET?

FET used as a low noise amplifier, as a buffer amplifier; in phase shift oscillator

9. Give the Shockley's equation for FET.

The Shockley's equation gives the relation between drain current (l_d) in the pinch of region and the gate to source voltage V_{gs}

$Id = I_{dss} [1 - V_{gs} / V_p]$

Where I_{dss} = maximum value of drain current when $V_{gs} = 0$

V_p = Pinch off voltage.

9. What is meant by Gate -Source threshold voltage and pinch off voltage of a JFET?

The voltage at which the channel is completely cut-off and the drain current becomes zero is called as Gate -Source threshold voltage.

In the output characteristics of FET, the drain current rises rapidly with drain source voltage. After reaching some value, it becomes constant. The drain source voltage above which drain current becomes constant is known as pinch off voltage. The corresponding Vgs is called Gate -Source threshold voltage.

10. Why the input impedance in FET is very high in comparison with BJT?

The input impedance of FET is extremely high because reverse bias is applied at input whereas in BJT , the output impedance is low due to applied forward bias.

11. How is FET used as VVR?

At low voltages, the depletion regions are thin and the drain current increases with voltages. So in the region where voltage is less then pinch off voltage (V_p) , FET is behaving as a voltage variable resistor (VVR). That is the drain to source resistance is controlled by V_{gs}

12. What is MOSFET? (May 2013)

The MOSFET is an abbreviation of Metal Oxide Semiconductor Field Effect Transistor. It is a three terminal semiconductor device similar to a FET with gate insulated from the channel. Therefore it is a also known as insulated Gate (IGFET)

13. Why is the input impedance of a MOSFET higher than that of FET?

The input impedance of a MOSFET is higher than that of FET since the gate is insulated from the channel by a thin layer of silicon di oxide

14. Depletion MOSFET is commonly known as Normally – ON = MOSFET ?

The depletion MOSFET can conduct even if the gate to source voltage (Vgs) is zero. Due to this reason depletion MOSFET is commonly known as Normally –ON MOSFET.

15. What is meant by inversion layer in E - MOSFET?

In the construction of E- MOSFET, there are two layers of conductor which sandwiched by Sio2 layer this can act as capacitor. When the gate is positive, it induces negative charges in the substrate which will form a part of drain current. This is called inversion layer.

16. Application of MOSFET?

i) It can be used as input amplifiers in oscilloscope, electronic voltmeters.
ii) It is used in computer memories in logic circuits
iii) It is used in phase shift oscillators.
iv) It is used in FM and TV receivers

17. Why E-MOSFET is normally called as OFF – MOSFET

When V_{gs} = 0, the biasing supply VDD this to force the force the free electron to move source to drain. But the P substrate has only few generated conduction band electrons. Aside from this minority carriers some surface leakage, the current between source and drain is zero hence E- MOSFET is called as OFF MOSFET.

18. Differentiate JFET and MOSFET?

JFET	MOSFET

Reverse bias for gate	Positive or negative gate voltage
Gate is formed as a diode	Gate is made as a capacitor
Operated only in depletion mode	Can be operated either in depletion mode or in enhancement mode
High input impedance	Very high input impedance due to capacitive effect

19. Differentiate Enhancement MOSFET and Depletion MOSFET

Enhancement MOSFET	**Depletion MOSFET**
Positive voltage at the gate	Negative voltage at the gate
Inversion layer is made	Depletion of majority carries happens
Negative charges are formed	Positive charges are formed

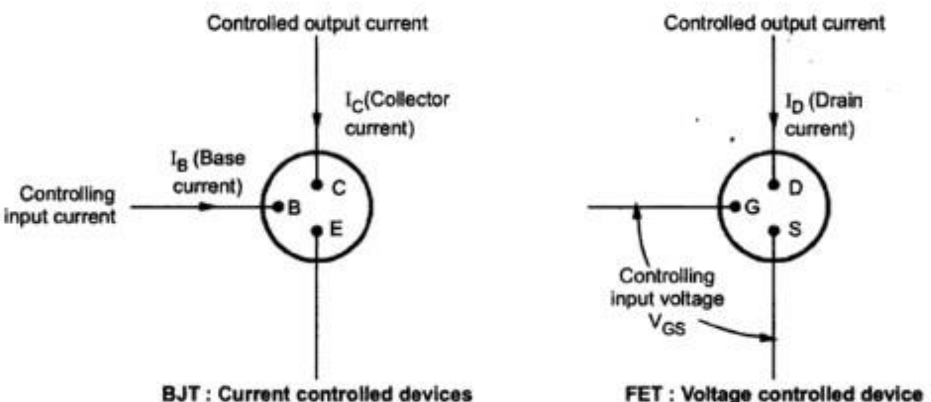
(11 MARKS)

The Field Effect Transistor abbreviated as **FET** is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device; however, the principle of operation of FET is completely different from that of BJT.

The three terminals of FET are named as Drain (D), Source (S) and Gate (G), as shown in the Fig. 7.1. Out of these three terminals gate terminal acts as a controlling terminal.

▶ Figure 7.1

Controlling element for BJT and FET



FET : Unipolar Device

We know that in BJT, the current is carried by both electrons and holes, and hence the name "**bipolar**" junction transistor. However in FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called **unipolar device**.

FET : Other Important Features

- Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is **more temperature stable** as compared to the BJT.
- FET has very high input impedance. Typically, it is in the range of one to several megaohms. Because FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required.
- FETs require less space than that for BJTs, hence they are preferred in integrated circuits.

In general, like BJTs the FETs can be used in switch, digital and linear amplifier applications. Because of Schottky barrier junction MESFETs have smaller transit time and faster response. Hence they are used in very high speed or high frequency applications, such as microwave amplifiers.

In JFET, there is a direct electrical connection between the gate terminal and the channel of a JFET. On the other hand, in MOSFETs, the gate is insulated from the channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, in MOSFETs, there is no direct electrical connection between the gate terminal and the channel. Due to this extra layer the input resistance of MOSFET is very very high.

The MOSFETs can be used in place of resistors in a circuit, so that circuits containing only MOSFETs can be designed. The MOSFET, compared to BJTs, can be made very small (that is, it occupies a very small area on an IC). Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high-density VLSI circuits, including microprocessors and memories, can be fabricated using MOSFETs. The MOSFET has made possible the hand-held calculator and the powerful personal computer. MOSFETs can also be used in analog circuits.

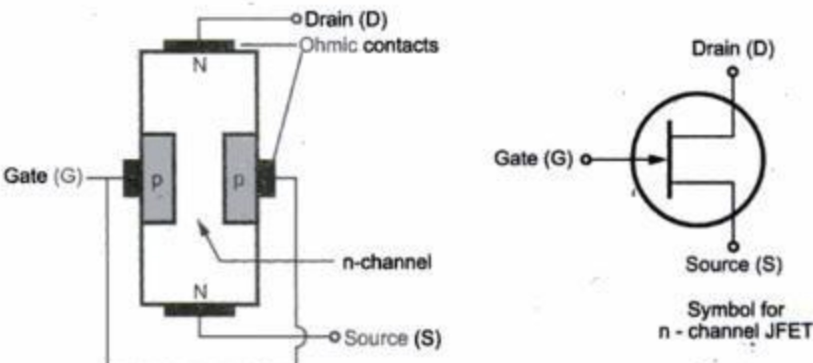
1. **Explain the construction of N channel JFET .Also explain the drain and transfer characteristics of N-channel JFET. [Nov/Dec 2014] .[April/May 2014]**

7.2.1 Construction of n-channel JFET and Symbol

The Fig. 7.3 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n type is taken and at its two ends, two ohmic contacts are made which are the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the **channel**. Since this channel is in the n type bar, the FET is known as **n-channel JFET.**

▶ Figure 7.3

Structure and symbol for n-channel JFET



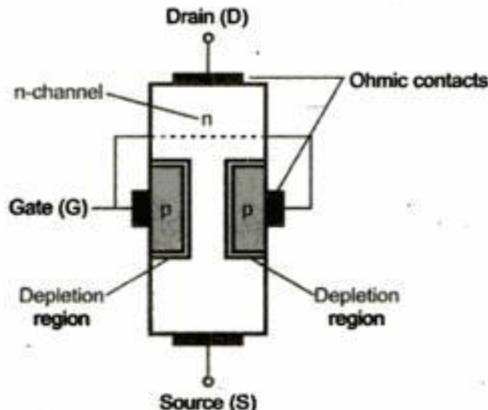
The electrons enter the channel through the terminal called **source** and leave through the terminal called **drain**. The terminals taken out from heavily doped electrodes of p type material are called **gates**. Usually, these electrodes are connected together and only one terminal is taken out, which is called **gate**, as shown in the Fig. 7.3.

UNBIASED JFET

In the absence of any applied voltage, JFET has gate channel junctions under no bias conditions. The result is a depletion region at each junction, as shown in Fig. 7.5.

Figure 7.5

Junction field effect transistor



This represents same depletion region of a diode under no bias conditions. Recall also that depletion region is that region which does not have any free carriers and therefore is unable to support conduction through the region.

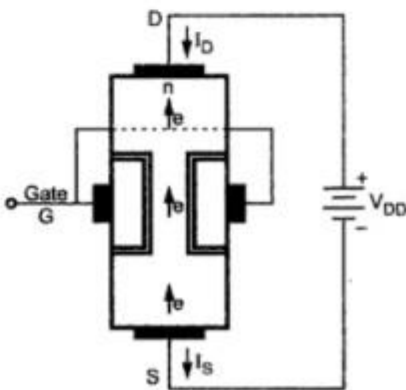
7.4 Operation of JFET

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit shown in Fig. 7.6. As shown in Fig. 7.6, voltage V_{DD} is applied between drain and source. Gate terminal is kept open. The bar is of n-type material. Due to the polarities of applied voltage as shown in Fig. 7.6, the majority carriers i.e. the electrons start flowing from the source to the drain. This flow of electrons makes the drain current, I_D.

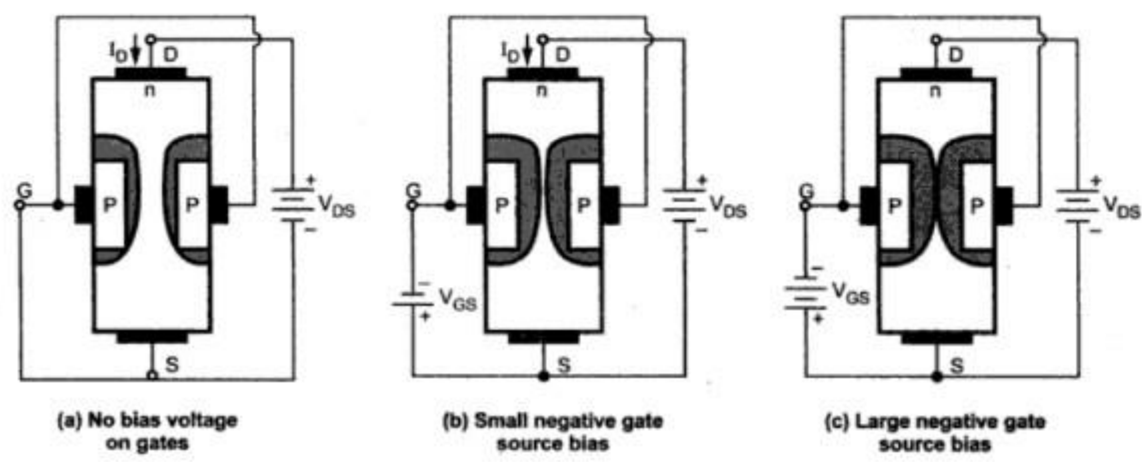
▶ Figure 7.6

n- channel JFET with gate open and V_{DD} is applied between drain and source



The majority carriers (electrons in n-channel JFET and holes in p-channel JFET) move from source to drain through the space between the gate regions. This space is commonly known as **channel**. The width of this channel can be controlled by varying the gate voltage. To see the effect of gate voltage on channel- width and on drain current I_D, consider the diagram shown in Fig. 7.7.

▶ Figure 7.7



(a) No bias voltage on gates

(b) Small negative gate source bias

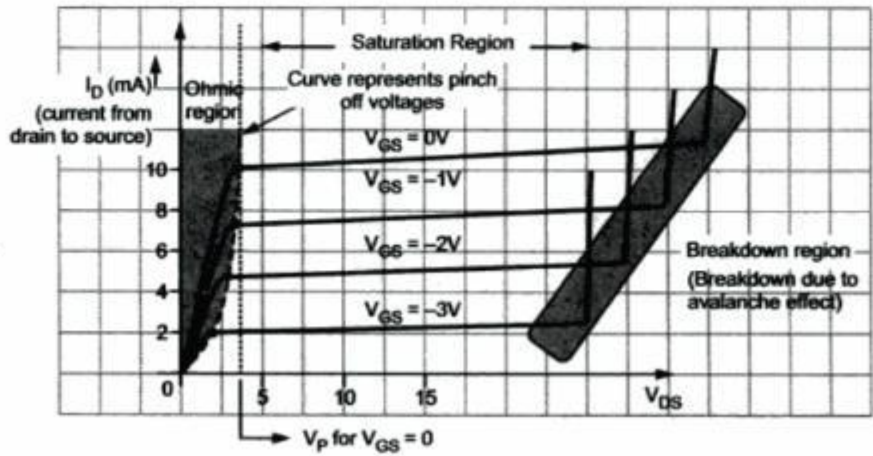
(c) Large negative gate source bias

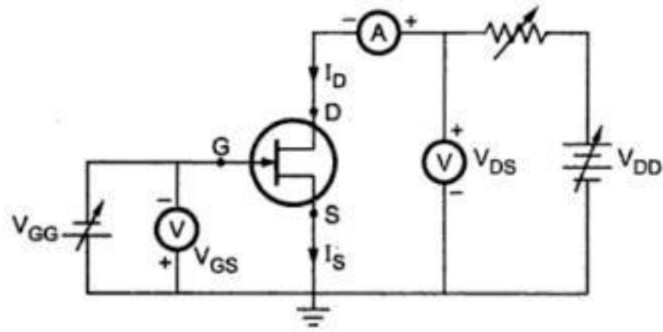
7.5.1 Drain V-I Characteristics for n-channel JFET

Fig. 7.8 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current I_D and drain to source voltage V_{DS} for different values of V_{GS}. Fig. 7.9 shows the experimental setup required to plot this characteristics.

► **Figure 7.8**

Drain V-I characteristics of n-channel JFET





From this characteristics we observe following points :

1. V_{GS} and V_{DS} both = 0 :

When V_{GS} = 0 the channel is entirely open. But V_{DS} = 0, so there is no attractive force for the majority carriers (electrons in n-channel JFET) and hence drain current does not flow.

2. Self pinch off at no bias (V_{GS} = 0) :

At V_{GS} = 0, in response to a small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly with V_{DS}. As V_{DS} increases, the voltage drop along the channel also increases. This increase in voltage drop increases the reverse bias on gate-source junction and causes the depletion regions to penetrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus, rate of increase in I_D with respect to V_{DS} is now reduced. This is shown by the curved shape in the characteristics.

At some value of V_{DS}, drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase the drain current I_D. I_D approaches the constant saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called **'Pinch-Off Voltage'**, V_p.

3. V_{GS} with negative bias :

When an external bias, of say –1V, is applied between the gate and the source, the gate channel junctions are further reverse biased, reducing the effective width of the channel available for the conduction. Because of this, drain current will reduce and pinch off voltage is reached at a lower drain current than when $V_{GS} = 0$, as shown in Fig. 7.8.

By applying several values of negative external bias voltage (V_{GS}), a family of curves are obtained as shown in Fig. 7.8. From Fig. 7.8 it can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.

Relation of $V_{GS(off)}$ and V_p

I_D is 0 when $V_{GS} = -V_p$. Because a 0 drain current corresponds to an off condition, the magnitude of V_p is equivalent to the magnitude of $V_{GS(off)}$. Most JFET data sheets specify a value only for $V_{GS(off)}$ and not for V_p. But once we know $V_{GS(off)}$, we also know V_p. For example, if $V_{GS(off)} = -4V$, then $V_p = 4V$.

The p-n junction between gate and source is reverse biased and the gate current is practically zero. Then the resistance between gate and source will be very large, ideally infinite. Thus **input impedance of FET is very large**. Compared to this, the input impedance of BJT is small. Also, we have seen that the drain current depends on V_{GS} and almost independent of V_{DS}. By changing V_{GS}, drain current can be varied. Hence FET is basically a **voltage-controlled device**. The input voltage controls the output current.

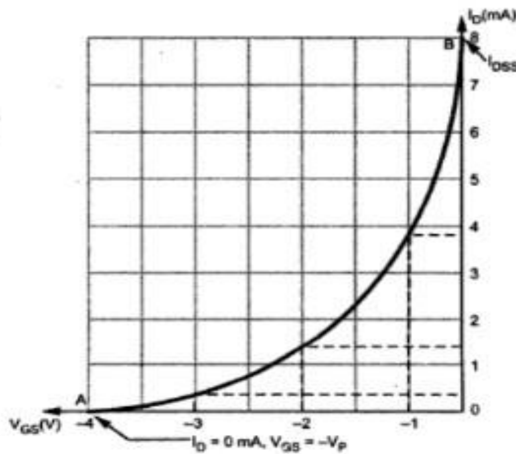
2. Explain the Transfer Characteristics of N channel JFET. [Nov/Dec 2014] [April/May 2014]

7.5.3 Transfer Characteristics for n-channel JFET

Fig. 8.12 shows the transfer characteristics of n-channel JFET. The curves represents relationship between the drain current I_D and gate to source voltage V_{GS}.

▶ Figure 7.12

Transfer characteristics of n-channel JFET



From this characteristics we observe following points :

1. The relationship between the drain current I_D and gate to source voltage V_{GS} is non-linear. This relationship is defined by **Shockley's** equation

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2 \qquad \dots (1)$$

The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}. From equation we can also write,

$$V_{GS} = V_P\left(1-\sqrt{\frac{I_D}{I_{DSS}}}\right) \qquad \dots (2)$$

In the equation values of I_{DSS} and V_p are constants, value of V_{GS} controls I_D .

2. A point A at the bottom end of the curve on the V_{GS}-axis represents $V_{GS(off)}$, and point B at the top end of the curve on the I_D axis represents I_{DSS} (maximum drain current at $V_{GS} = 0$). Thus, this curve shows the operating limits of a JFET.

These are : $I_D = 0$ when $V_{GS} = V_{GS(off)}$

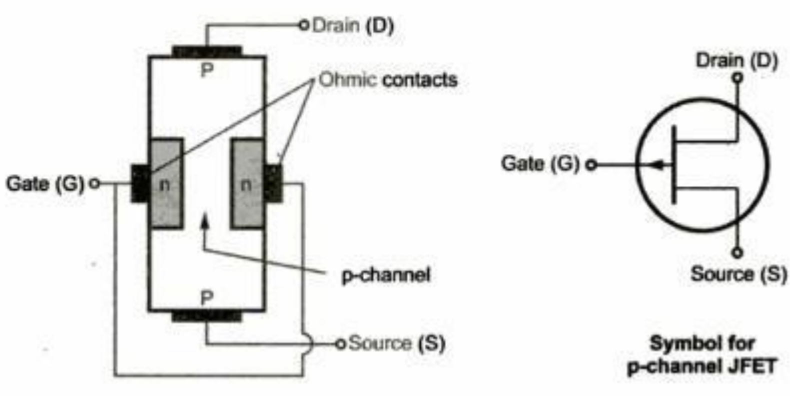
$I_D = I_{DSS}$ when $V_{GS} = 0$

3. **Explain about the P channel JFET in detail with its characteristics**

7.2.2 Construction of p-channel JFET and Symbol

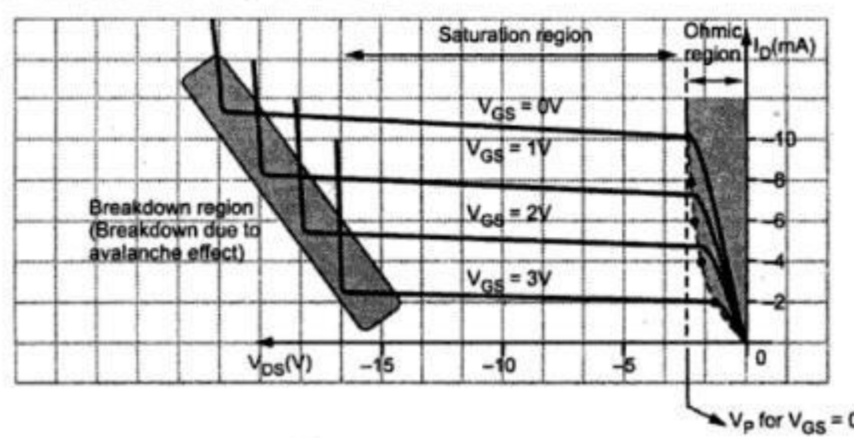
The device could be made of p type bar with two n type gates as shown in the Fig. 7.4. Then this will be **p-channel JFET**. The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in **n-channel JFET** the current is carried by electrons while in **p-channel JFET**, it is carried by holes.

Structure and symbol for p-channel JFET



▶ **Figure 7.11**

Drain/V-I charcteristics of p-channel JFET



4. Explain about JFET parameters.

7.6 JFET Parameters

The important parameters of JFET are as follows :

- Transconductance (g_m)
- Input reistance and capacitance
- Drain to source resistance (r_d)
- Amplification factor (μ)

7.6.1 Transconductance

The transconductance, g_m, is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant as shown in Fig. 7.15. (See Fig. on next page.)

Looking at Fig. 7.15, we can say that it is the slope of the transfer characteristic. Since the slope varies, g_m also varies. g_m has a greater value near the top of the curve than it does near the bottom. The transconductance g_m is defined as

$$g_m = \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}\text{ constant}} \qquad \ldots (1)$$

The transconductance g_m is also called **mutual conductance.** The practical unit for g_m is mS (millisiemen) or mA/V. For given g_m, we can calculate an approximate value for g_m at any point on the transfer characteristic curve using the following equation

$$g_m = g_{mo}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right] \qquad \ldots (2)$$

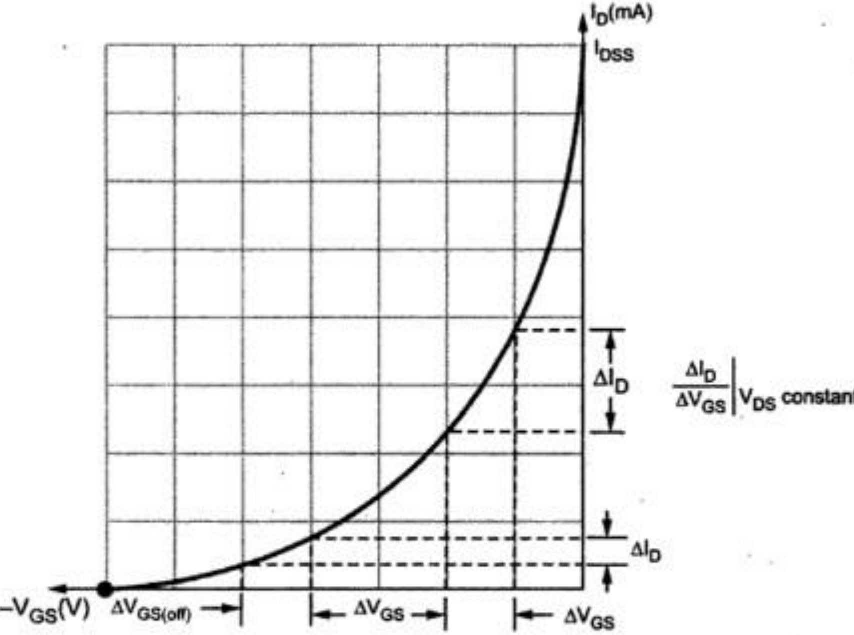
where g_{mo} is the value of g_m for $V_{GS} = 0$, and is given by,

$$g_{mo} = \frac{-2\,I_{DSS}}{V_p} \qquad \ldots (3)$$

This can be proved as given below. We know that,

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_p}\right]^2$$

Transconductance g_m varies depending on the bias point (V_{GS})



Differentiating this equation with respect to V_{GS} we get,

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2 I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$= g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] \qquad \text{where} \quad g_{mo} = \frac{-2 I_{DSS}}{V_p}$$

7.6.2 Input resistance and capacitance

We know tht a JFET operates with its gate source junction reverse-biased. Therefore, the input resistance at the gate is very high. This high input resistance is one advatnage of the JFET over the bipolar transistor. (Recall that a BJT operates with a forward biased base-emitter junction.) JFET data sheets often specify the input resistance by giving a value of the gate reverse current, I_{GSS}, at a cetain gate to surce voltage, V_{GS}. The input resistance can then be determined using the following equation, where the vertical lines indicate an absolute value.

$$R_{IN} = \frac{|V_{GS}|}{|I_{GSS}|}$$

For example, the 2N3909 data sheet in Fig. 8.20 lists a maximum I_{GSS} of 10nA for V_{GS} = 10V at 25°C. Therefore,

$$R_{IN} = \left|\frac{10V}{10nA}\right| = 1000\ M\Omega$$

From the Fig. 8.20 we can also observe that I_{GSS} is 1.0 μA for V_{GS} = 10 V at 100°C. This shows that I_{GSS} increases with temperature. Here,

$$R_{IN} = \left|\frac{10V}{1\mu A}\right| = 10\ M\Omega$$

7.6.3 Drain to Source Resistance

From the drain characteristic, the important parameter of JFET, drain resistance r_d, can be calculated. Fig. 7.16 shows the drain characteristics of n-channel JFET.

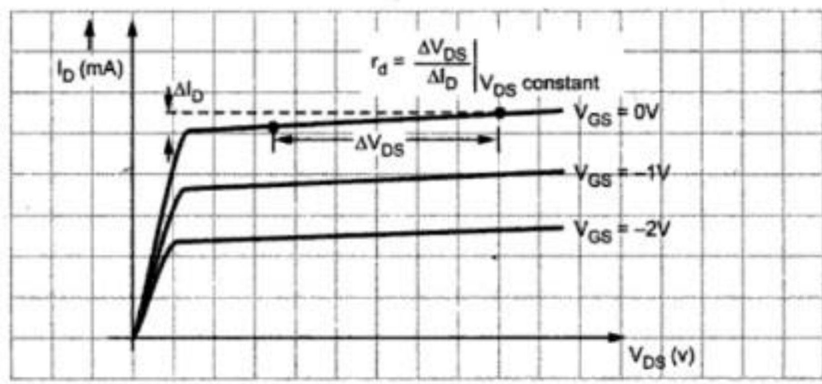
The drain resistance r_d is the ac resistance between drain and source terminals when the JFET is operating in the saturation region. It is the reciprocal of the slope of the drain characteristic in the saturation region. It is given by

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS\ constant}} \quad \ldots (4)$$

Since the characteristics in the saturation region is almost flat, r_d is not easily determined from the characteristics. Values of r_d range from about 50 $k\Omega$ to several hundred $k\Omega$. Since r_d is usually the output resistance of the JFET, it may also be expressed as an output admittance $|Y_{os}| = 1/r_d$.

Figure 7.16

Drain characteristics of n-channel JFET



7.6.4 Amplification Factor

The amplification factor, denoted by μ is defined as,

$$\text{Amplification factor } \mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_{D\ constant}}$$

$$\therefore \quad \mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\therefore \quad \mu = r_d \times g_m \quad \ldots (5)$$

Sr. No.	Parameter	BJT	FET
1	Control element	Current controlled device. Input current I_B controls output current I_C.	Voltage controlled device. Input voltage V_{GS} controls drain current I_D.
2	Device type	Current flows due to both, majority and minority carriers and hence **bipolar device.**	Current flows only due to majority carriers and hence **unipolar device.**
3	Types	npn and pnp	n-channel and p-channel.
4	Symbols	C, B, E (npn); C, B, E (pnp)	D, G, S (n-channel); D, G, S (p-channel)
5	Configurations	CE, CB, CC	CS, CG, CD
6	Input resistance	Less compare to JFET.	High compare to BJT.
7	Size	Bigger than JFET.	Smaller in construction than BJT, thus making them useful in integrated - circuits (IC).
8	Sensitivity	Higher sensitivity to changes in the applied signals.	Less sensitivity to changes in the applied voltage.
9	Thermal stability	Less	More
10	Thermal runaway	Exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temeperature in the device.	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device.
11	Relation between input and output	Linear	Non-linear
12	Ratio of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$
13	Thermal noise	More in BJT as more charge carriers cross junctions.	Much lower in JFET as very few charge carriers cross the junction.
14	Gain bandwidth product	High	Low

5. Briefly explain different BIASING OF FET

Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. However, the wide differences in maximum and minimum transfer characteristics make it necessary to keep drain current I_D stable at its quiescent value. In this chapter we see the different dc biasing techniques for FET amplifier. The general relationships that can be applied to the dc analysis of all FET amplifiers are :

$$I_G = 0A \qquad \dots (1)$$

$$I_D = I_S \qquad \dots (2)$$

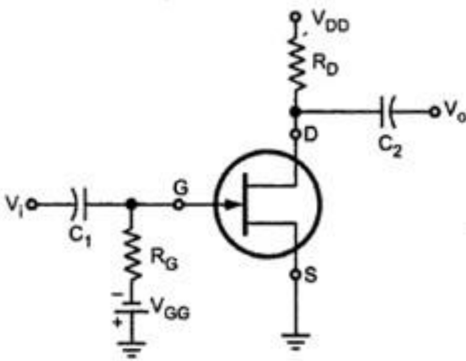
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2 \qquad \dots (3)$$

8.2.1 Fixed-bias Circuit

Fig. 8.1 shows the fixed bias circuit for the n-channel JFET. This is the simplest biasing arrangement. To make gate-source junction reverse-biased, a separate supply V_{GG} is connected such that gate is more negative than the source.

Figure 8.1

Fixed bias circuit for n-channel circuit

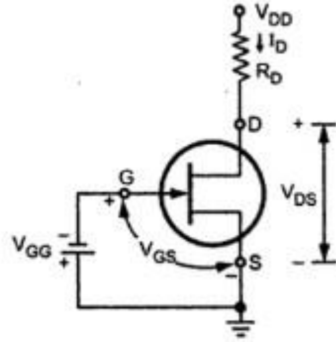


DC Analysis

For the dc analysis coupling capacitors are open circuits. The current through R_G is I_G which is zero. This permits R_G to replace by short circuit equivalent, simplifying the fixed bias circuit as shown in the Fig. 8.2.

Figure 8.2

Simplified fixed bias circuit



We know for dc analysis

$$I_G = 0 \text{ A}$$

and applying KVL to the input circuit we get,

$$V_{GS} + V_{GG} = 0$$

$$\therefore \; V_{GS} = -V_{GG} \qquad \dots (1)$$

Since V_{GG} is a fixed dc supply, the voltage V_{GS} is fixed in magnitude, and hence the name fixed bias circuit.

For fixed bias circuit the drain current I_D can be calculated using equation 8.3.

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_P}\right)^2$$

The drain to source voltage of output circuit can be determined by applying KVL.

$$+ V_{DS} + I_D R_D - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D \qquad \dots (2)$$

The **Q point** of the JFET amplifier with fixed bias circuit is given by :

$$\mathbf{I_{DQ}} = I_{DSS}\left[1-\frac{V_{GS}}{V_P}\right]^2$$

$$\mathbf{V_{DSQ}} = V_{DD} - I_{DQ} R_D$$

8.2.2 Voltage Divider Bias Circuit

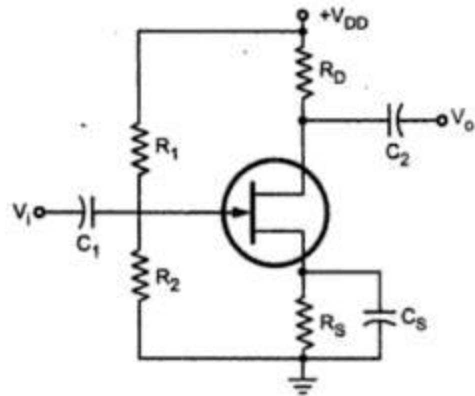
The Fig. 8.4 shows n-channel JFET with voltage divider bias. The voltage at the source of the JFET must be more positive than the voltage at the gate in order to keep the gate-source junction reverse-biased. The source voltage is,

$$V_S = I_D R_S$$

The gate voltage is set by resistors R_1 and R_2 as expressed by the following equation using the voltage divider formula :

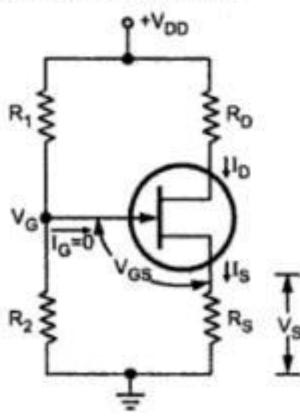
$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD} \qquad \because I_G = 0$$

Voltage divider bias for n-channel JFET



▶ **Figure 8.5**

Simplified voltage divider circuit for dc analysis



DC Analysis :

Applying KVL to the input circuit we get,

$$V_G - V_{GS} - V_S = 0$$

$$\therefore V_{GS} = V_G - V_S = V_G - I_S R_S$$

$$= V_G - I_D R_S \qquad \because I_D = I_S$$

$$\therefore V_{GS} = V_G - I_D R_S \qquad \dots (3)$$

Applying KVL to the output circuit we get,

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$\therefore V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$= V_{DD} - I_D (R_D + R_S) \qquad \dots (4)$$

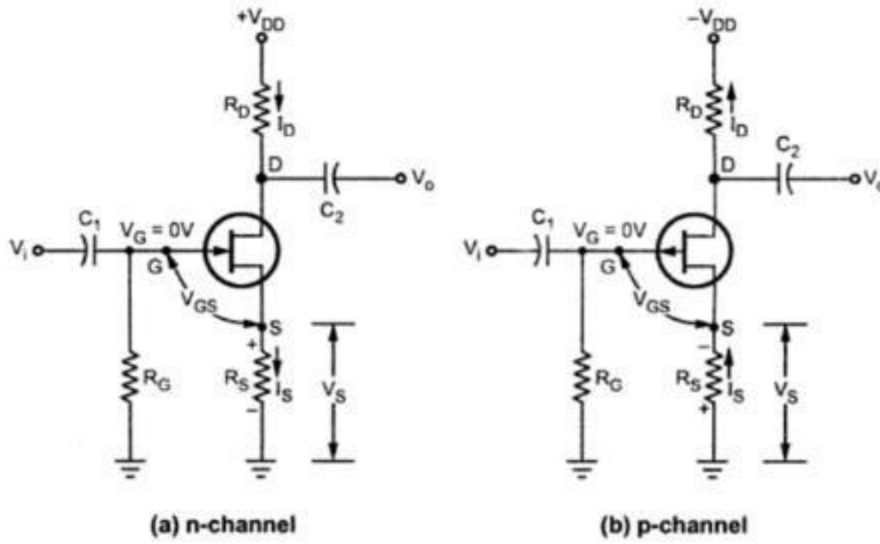
The Q point of a JFET amplifier using the voltage divider bias is given by :

$$\mathbf{I_{DQ}} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$\mathbf{V_{DSQ}} = V_{DD} - I_D (R_D + R_S)$$

5.9.1.3 Self Bias Circuit

Self bias is the most common type of JFET bias. Recall that a JFET must be operated such that the gate source junction is always reverse-biased. This condition requires a negative V_{GS} for an n-channel JFET and a positive V_{GS} for p-channel JFET. This can be achieved using the self bias arrangement shown in Fig. 5.50. The gate resistor, R_G, does not affect the bias because it has essentially no voltage drop across it; and therefore the gate remains at 0 V. R_G is necessary only to isolate an a.c. signal from ground in amplifier applications. The voltage drop across resistor, R_S makes gate source junction reverse biased.



For the n-channel FET in Fig. 5.50 (a), I_S produces a voltage drop across R_S and makes the source positive with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = I_S R_S = I_D R_S$. The gate to source voltage is,

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D R_S$$

For the p-channel FET in Fig. 5.50 (b), I_S produces a voltage drop across R_S and makes the source negative with respect to ground. Since $I_S = I_D$ and $V_G = 0$, then

$V_S = -I_S R_S = -I_D R_S$. The gate to source voltage is

$$V_{GS} = V_G - V_S = 0 - (-I_D R_S) = +I_D R_S$$

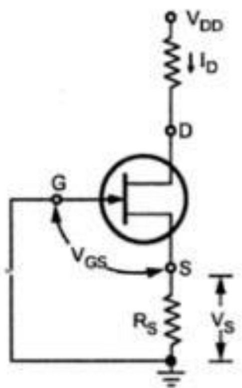


Fig. 5.51 Simplified self bias circuit for dc analysis

In the following D.C. analysis, the n-channel JFET shown in Fig. 5.50 (a) is used to for illustration . For D.C. analysis we can replace coupling capacitors by open circuits and we can also replace the resistor R_G by a short circuit equivalent, since $I_G = 0$. This is illustrated in Fig. 5.51.

We know, equation (3) gives relation between I_D and V_{GS}

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_p}\right)^2$$

Substituting value of V_{GS} in above equation we get,

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_p}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_p}\right)^2 \quad \dots (8)$$

Applying KVL to the output circuit we get,

$$V_S + V_{DS} + I_D R_D - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D (R_S + R_D)$$

$$V_{DS} = V_{DD} - I_D (R_S + R_D) \quad \dots (9)$$

6.With the help of a neat diagram explain the construction, operation and characteristics of N channel and P channel depletion type MOSFET. [Nov/Dec 2015][April 2015] [April/May 2014]

MOSFET (metal oxide semiconductor field effect transistor) is a second category of field effect transistor. It became a practical reality in the 1970s. The MOSFETs, compared to BJTs, can be made very small and hence can be used to design high density VLSI circuits.

The MOSFET differs from the JFET in that it has no p-n junction structure ; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input resistance of MOSFET is greater than JFET. Because of the insulated gate, MOSFETs are also called **IGFETs**. Two basic types of MOSFETs are : depletion (D) MOSFET and enhancement (E) MOSFET. The terms depletion and enhancement define their basic mode of operation.

3.17.1 Depletion MOSFET (D-MOSFET)

3.17.1.1 Construction of n-channel MOSFET

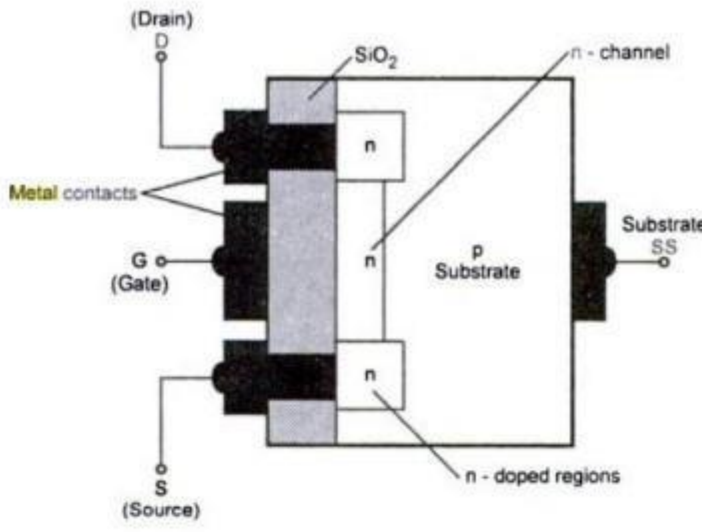
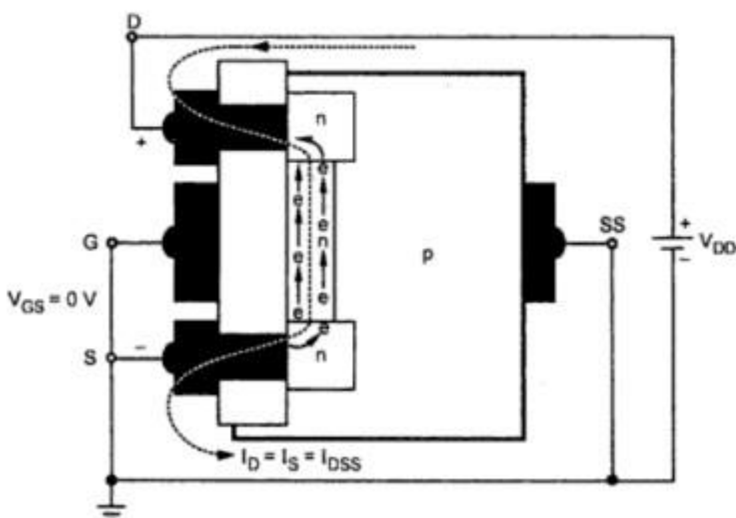


Fig. 3.63 n-channel depletion-type MOSFET

The Fig. 3.63 shows the basic construction of n channel depletion type MOSFET. Two highly doped n regions are diffused into a lightly doped p type substrate. These two highly doped n regions represent source and drain. In some cases substrate is internally connected to the source terminal.

The source and drain terminals are connected through metallic contacts to n-doped regions linked by an n-channel as shown in the Fig. 3.63. The gate is also connected to a metal contact surface but remains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus, there is no direct electrical connection between the gate terminal and the channel of a MOSFET, increasing the input impedance of the device.

3.17.1.2 Operation, Characteristics and Parameters of n-Channel MOSFET



On the application of drain to source voltage, V_{DS} and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS} = 0$ V, as shown in the Fig. 3.64.

Fig. 3.64 n-channel depletion-type MOSFET with V_{GS} = 0 V and an applied voltage V_{DD}

If we apply negative gate voltage, the negative charges on the gate repel conduction electrons from the channel, and attract holes from the p type substrate. This initiates recombination of repelled electrons and attracted holes as shown in the Fig. 3.65.

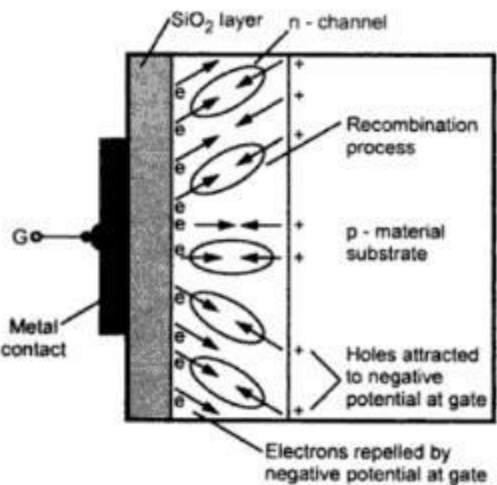


Fig. 3.65 Reduction in free electrons in the n-channel due to negative potential at the gate terminal

The level of recombination between electrons and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the number of free electrons in the n-channel for the conduction, reducing the drain current.

In other words we can say that, due to recombinations, n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. The level of drain current will reduce with increasing negative bias for V_{GS} as shown in the transfer characteristics of depletion type MOSFET (Fig. 3.66).

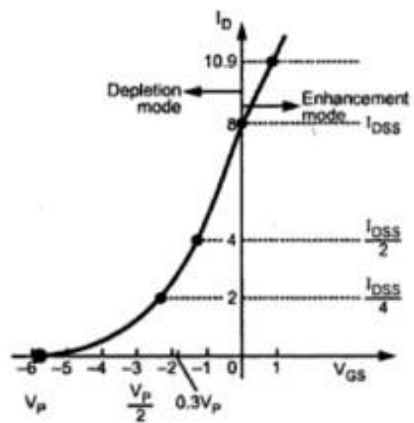


Fig. 3.66 Transfer characteristics for an n-channel depletion type MOSFET

For positive values of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases as shown in the Fig.3.67.

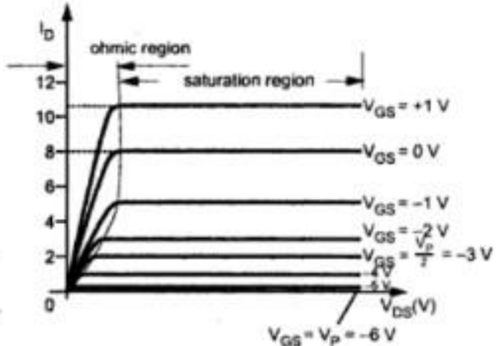
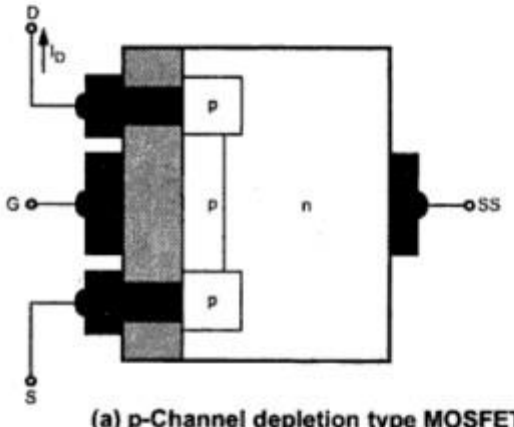


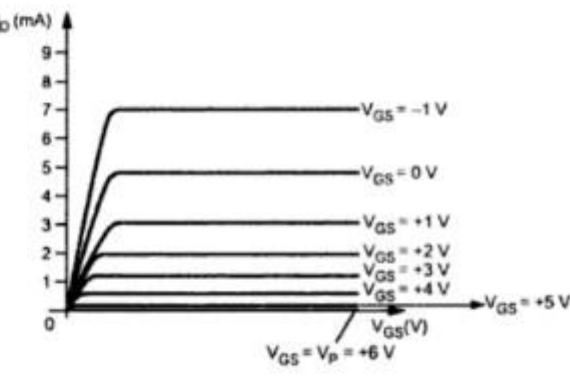
Fig. 3.67 Drain characteristics for an n-channel depletion type MOSFET

The application of a positive gate to source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with V_{GS} = 0 V. For this reason the region of positive gate voltages on the drain or transfer characteristics is referred to as enhancement region and the region between cut-off and the saturation levels of I_{DSS} referred to as depletion region. Fig. 3.67 shows drain characteristics for an n-channel depletion type MOSFET. It is similar to that of JFET. The only difference is that it has positive part of V_{GS}.

3.17.1.3 p-Channel Depletion Type MOSFET



(a) p-Channel depletion type MOSFET



(b) Drain characteristics of p-channel depletion type MOSFET

Fig. 3.68

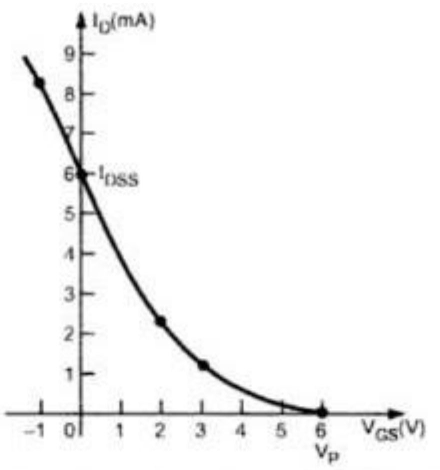


Fig. 3.69 Transfer characteristics of p-channel depletion type MOSFET

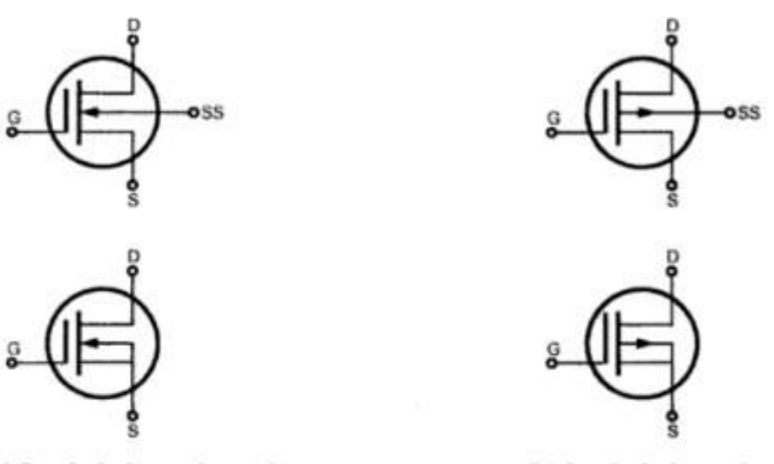
The construction of the p-channel depletion type MOSFET is exactly opposite of that of n-channel depletion type MOSFET. Here, the substrate is of n-type, and regions and channel are of p type as shown in the Fig. 3.68 (a).

As shown in the Fig. 3.68 (a) voltage polarities and current directions are reversed. The drain characteristics appear exactly as in Fig. 3.68 (b) but V_{DS} with negative values, I_D in the opposite direction and V_{GS} having opposite polarities as shown in the Fig. 3.68 (b).

Fig. 3.69 shows the transfer characte- ristics of p-channel depletion type MOSFET. In the p-channel depletion type MOSFET, the transfer characteristics is a mirror image about the I_D axis (Y axis) of the transfer characteristic of n-channel depletion type MOSFET, since the V_{GS} is positive in p-channel depletion region.

3.17.1.4 D-MOSFET Symbols

Fig. 3.70 shows graphic symbols for n and p-channel depletion type MOSFET. In the symbol insulation between gate and channel is represented by a space between the gate and other terminals of the symbol. The vertical line represents that the channel is connected between the drain and source and is "supported" by the substrate. Two symbols are given for each type of channel to reflect the fact that, in some cases it is internally shorted to source terminal.



(a) Symbols for n-channel depletion type MOSFETs

(b) Symbols for p-channel depletion type MOSFETs

Fig. 3.70

7. **With the help of a neat diagram explain the construction, operation and characteristics of N channel and P channel enhancement type MOSFET. [Nov/Dec 2015][April 2015] [April/May 2014]**

3.17.2 Enhancement MOSFET (E-MOSFET)

This type of MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the depletion MOSFET in that it has no physical channel.

3.17.2.1 Construction of n-Channel E-MOSFET

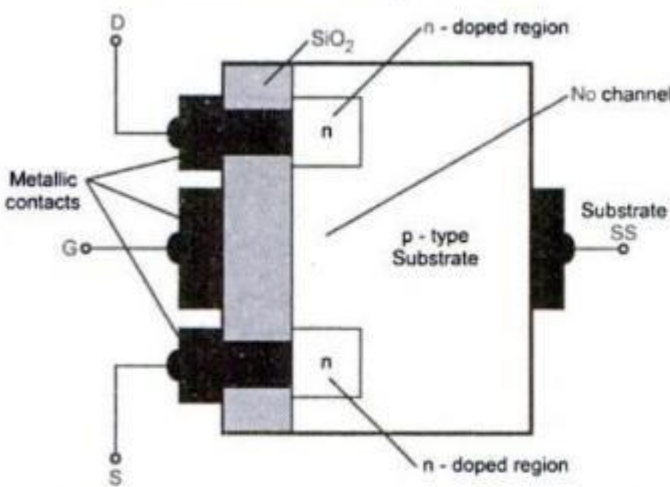


Fig. 3.71 n-Channel enhancement type MOSFET

The Fig. 3.71 shows the basic construction of n-channel enhancement type MOSFET.

Like, depletion type MOSFET, two highly doped n regions are diffused into a lightly doped p type substrate. The source and drain are taken out through metallic contacts to n-doped regions as shown in the Fig. 3.71. But the channel between two n-regions is absent in the enhancement type MOSFET. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.

3.17.2.2 Operation, Characteristics and Parameters of n-Channel E-MOSFET

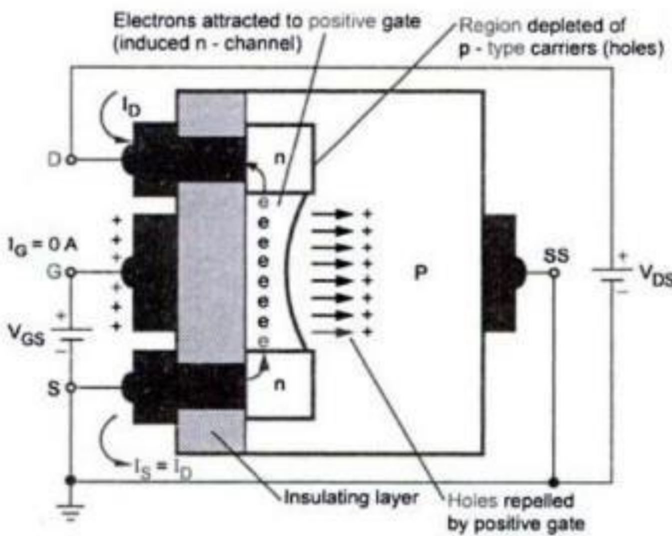


Fig. 3.72 Channel formation in the n-channel enhancement type MOSFET

On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows-quite different from the depletion type MOSFET and JFET. If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near the SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer, as shown in the Fig. 3.72. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.

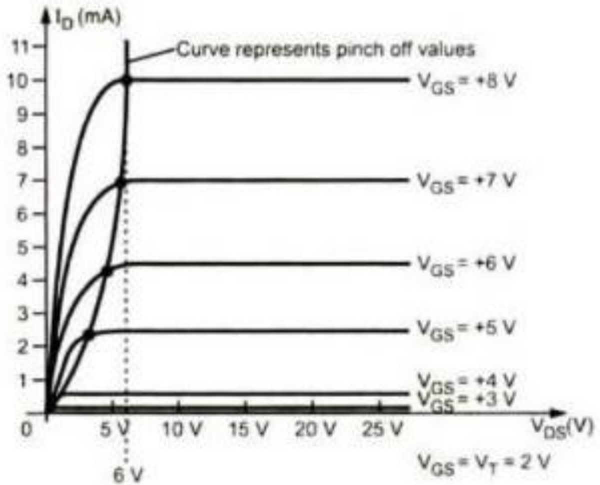


Fig. 3.73 Drain characteristics of an n-channel enhancement type MOSFET

Since the channel does not exist with V_{GS} = 0 V and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

Fig. 3.73 shows the drain characteristics of an n-channel enhancement type MOSFET. Looking at Fig. 3.73 we can say that as V_{GS} increases beyond the threshold level, the density of free carriers (electrons) in the induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET. Fig. 3.74 shows pinch off process for n-channel enhancement type MOSFET.

current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The levelling off of I_D is due to a pinch-off process, is as described earlier for the JFET. Fig. 3.74 shows pinch off process for n-channel enhancement type MOSFET.

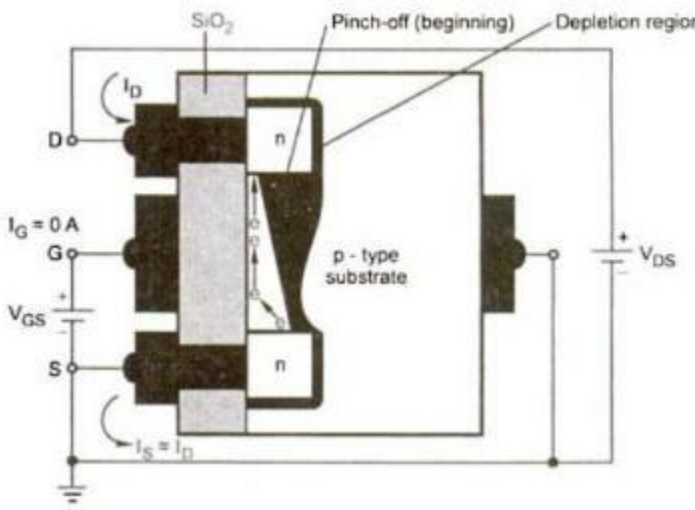


Fig. 3.74 Change in channel and depletion region with increasing level of V_{DS} for a fixed value of V_{GS}

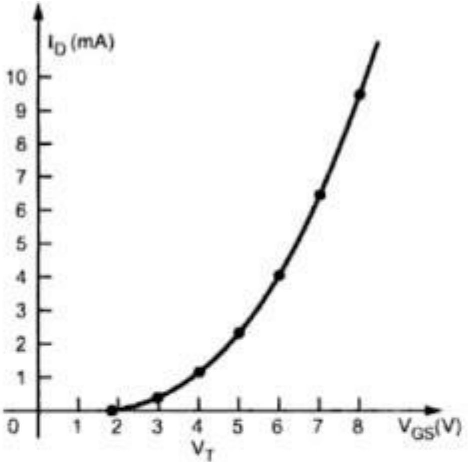


Fig. 3.75 Transfer characteristic for n-channel enhancement type MOSFET

Fig. 3.75 shows the transfer characteristic for n-channel enhancement type MOSFET. This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow until $V_{GS} = V_T$.

For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is nonlinear and it is given as

$$I_D = K(V_{GS} - V_T)^2 \qquad \dots (1)$$

The K term is a constant that is a function of the construction of the device. The value of K can be determined from equation,

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2} \qquad \dots (2)$$

3.17.2.3 p-Channel Enhancement Type MOSFET

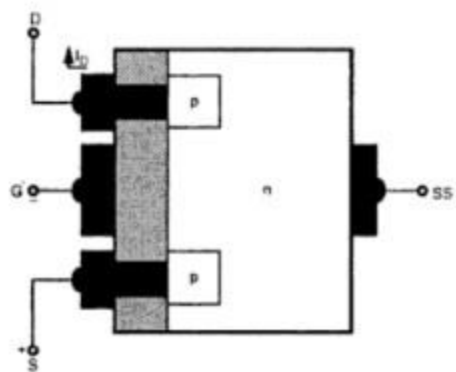


Fig. 3.76 Construction of p-channel enhancement type MOSFET

The construction of the p-channel enhancement type MOSFET is exactly opposite to that of n-channel enhancement type MOSFET. Here, the substrate is of n-type and regions are of p-type as shown in the Fig. 3.76.

As shown in the Fig. 3.77 voltage polarities and current directions are reversed. The drain characteristics appear exactly as in the Fig. 3.77 but with V_{DS} with negative values, I_D in opposite direction and V_{GS} having opposite polarities as shown in the Fig. 3.77.

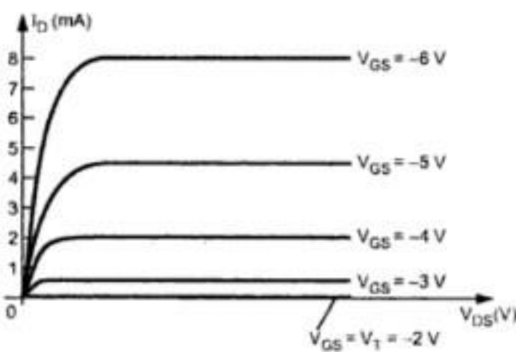


Fig. 3.77 Drain characteristics of p-channel enhancement MOSFET

Fig. 3.78 shows the transfer characteristics of p-channel enhancement type MOSFET. In the p-channel enhancement type MOSFET, the transfer characteristic is a mirror image about the I_D axis (y axis) of the transfer characteristics of n-channel depletion type MOSFET, since the V_{GS} is negative.

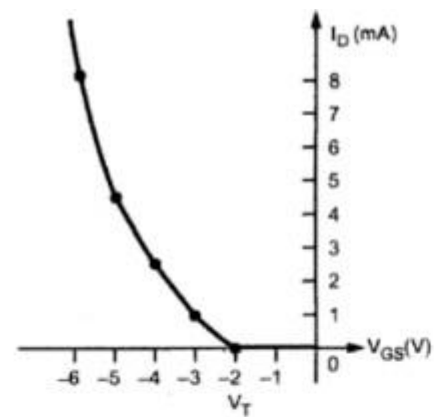


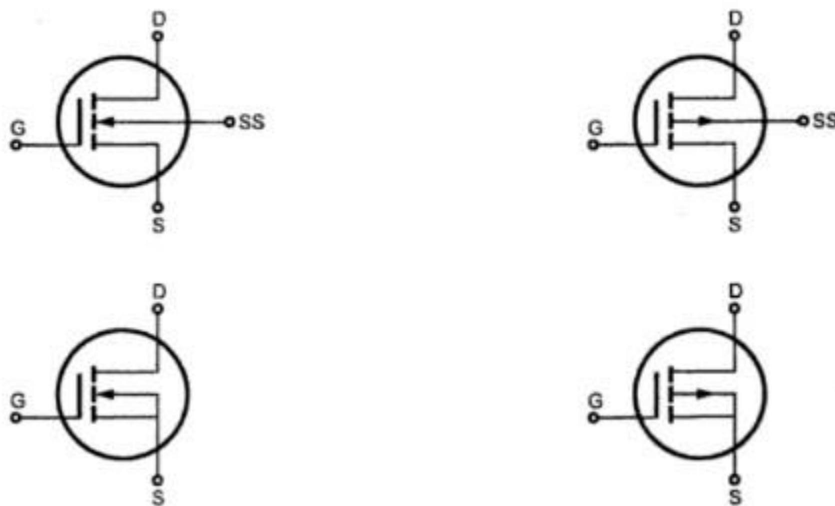
Fig. 3.78 Transfer characteristics of p-channel enhancement type MOSFET

E-MOSFET symbols

Fig. 3.79 shows graphic symbols for an n and p-channel enhancement type MOSFET. The dashed line between drain and source represents the fact that a channel does not exists between the two under no-bias conditions. It is the only difference between the symbols for the depletion type and enhancement type .

E-MOSFET symbols

Fig. 3.79 shows graphic symbols for an n and p-channel enhancement type MOSFET. The dashed line between drain and source represents the fact that a channel does not exists between the two under no-bias conditions. It is the only difference between the symbols for the depletion type and enhancement type .



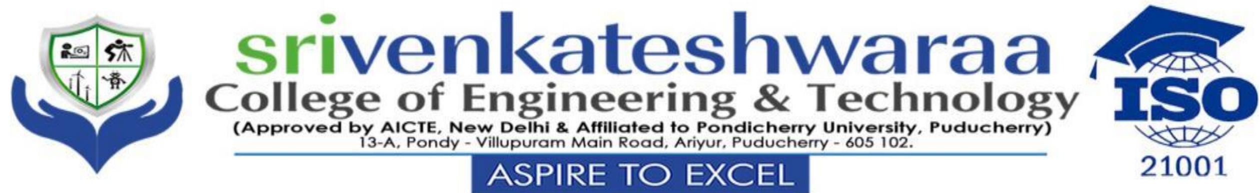
(a) Symbols for n-channel type MOSFETs enhancement

(b) Symbols for p-channel type MOSFETs enhancement

Fig. 3.79 Channel length modulation

3.18 Comparison of MOSFET with JFET

Sr. No.	Parameter	JFET	MOSFET
1	Types	a) n-channel b) p-channel	A) n-channel depletion type MOSFET B) p-channel depletion type MOSFET C) n-channel enhancement type MOSFET D) p-channel enhancement type MOSFET
2	Symbols	D, G, S n-channel D, G, S p-channel	D, G, S n-channel D, G, S p-channel Depletion type D, G, S n-channel D, G, S p-channel Enhancement type
3	Operation mode	Operated in depletion mode	Operated in depletion and enhancement mode
4	Input impedance	High (> 10 MΩ)	Very high (> 10,000 MΩ)
5	Gate	Gate is not insulated from channel	Gate is insulated from channel by a layer of SiO_2.
6	Channel	Channel exists permanently .	Channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET.



DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Subject Name: **ELECTRONIC DEVICES AND CIRCUITS**

Subject Code: **EE T34**

UNIT –IV POWER DEVICES

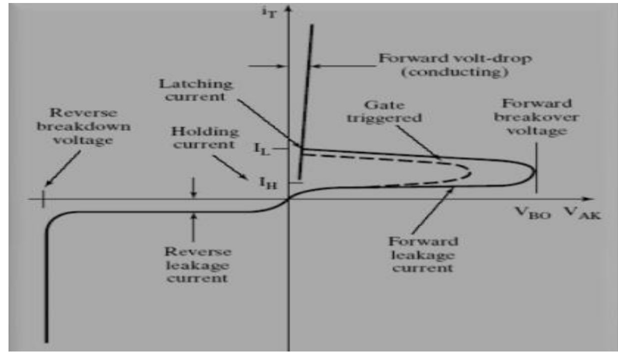
Introduction to power devices– SCR, SCS, GTO, Shockley diode-DIAC- TRIAC and UJT. RECTIFIERS AND POWER SUPPLIES: Half-wave and full-wave rectifiers–ripple reduction using filter circuits– Shunt and series voltage regulators– Regulated power supplies.

(2 marks)

1. **Define latching holding current in SCR. [Nov/Dec 2014]**
   - Latching current is the minimum anode current required to maintain the thyristor in the on State immediately after a thyristor has been turned on and gate signal has been removed.
   - Holding current is the minimum anode current to maintain the thyristor in the on state.
2. **What is DIAC? [Nov/Dec 2015]**

   A DIAC is a two-terminal four-layer semiconductor device (thyristor) that can conduct current in either direction.

3. **Draw the VI characteristics of a SCR and mark important points.[April 2014]**



4. **What are applications of UJT? [Nov 2013]**

   1. Phase control
   2. Saw – tooth generators
   3. Non sinusoidal oscillators
   4. Triggering device for SCR and TRIAC

5. **What does UJT stand for? Justify the name UJT**

   UJT stands for Unijunction Transistor. The UJT is a three terminal semiconductor device having two doped regions. It has one emitter terminal (E) and two base terminals (B1 and B2) It has only One junction, and the outlook of UJT resembles to a transistor and hence the name unijunction transistor. It is also called as double based diode.

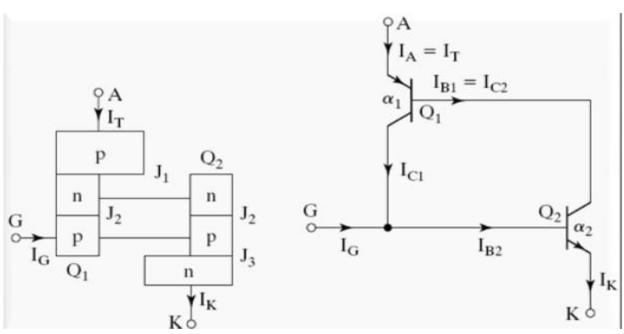
6. **What is intrinsic standoff ratio of a UJT? (Nov 2013)**

   The ratio of voltage between emitter and base 1 to V_{BB} is called as intrinsic stand of ratio $\eta = R_{B1} / (R_{B1}+R_{B2})$. The value lies between 0.51 to 0.82

7. **What is SCR?**

   A silicon-controlled rectifier (SCR) is a three terminal, three-junction semiconductor device that acts as a true electronic switch. It is a unidirectional device. It control the amount of power fed to the load.

8. **Draw the two transistor model of SCR**



9. Compare the transistor and thyristors

S.NO	TRANSISTOR	THYRISTOR
1.	Transistor is a three layer , two junction device	Thyristor is a four layer, three junction device
2.	Commutation circuitry which is costly and bulky, is not required	Commutation circuit is required
3.	To keep a transistor in the conducting state, a continuous base current is required.	Thyristors require a pulse to make it conducting and thereafter it remain conducting.

10. What is an IGBT? List its types.

Insulated gate bipolar transistor (IGBT) combines the advantages of BJT and MOSFET. Therefore it has low switching times as well as low power losses.

1. Punch through IGBT 2. Non punch IGBT.

11. What are the advantages of IGBTs?

i) They have high input gate impedance.
ii) They have low conduction loss.
iii) They have fast switching characteristics.
iv)They have very high operating frequency.

12. List the applications of IGBTs.

i) They are used in low noise, high performance power supplies.

ii) They are used in inverters.

iii) They are used in motor speed controls.

13. What is forward break over voltage?

It is the voltage above which the SCR enters the conduction region ('ON' state). The forward breakdown voltage is dependent on the gate bias.

14. What is holding current?

It is that value of current below which the SCR switches from the conduction state (ON state) to the forward blocking state.

15. What is latching current?

This is the minimum current flowing from anode to cathode when SCR goes from OFF to ON state and remains in ON state even after gate bias is removed. It is greater than, but very close to holding current.

16. What is reverse breakdown voltage?

It is the reverse voltage (Anode-negative and cathode-positive) above which the reverse breakdown occurs, breaking J_1 and J_3 junctions. When the SCR is reversed biased, the thickness of the J_2 depletion layer during the forward bias condition is greater than the total thickness of the two depletion layers at J_1 and J_3. Therefore, the forward breakover voltage V_{BO} is greater than the reverse breakover voltage V_{BR}.

(11 MARKS)

1. **Explain the construction and working of silicon controlled thyristor in detail**

Silicon controlled thyristor (scr):

The SCR is an unidirectional device and like diode, it allows to flow current in only one direction. But unlike diode, it has a built in feature to switch 'ON' and 'OFF'. The switching of SCR is controlled by the additional input called **gate** and biasing conditions. This switching property of SCR allows to control the 'ON' periods of the SCR thus controlling average power delivered to the load.

It can be used as a rectifier element like diode to convert a.c. signals to d.c. signals.

Construction:

The SCR is a four layer p-n-p-n device where p and n layers are alternately arranged. The outer layers are heavily doped. There are three p-n junctions called J_1, J_2 and J_3. The outer p layer is called **anode** while outer n layer is called **cathode.** Middle p layer is called **gate**. The three terminals are taken out respectively from these three layers, as shown in the Fig. 6.1.

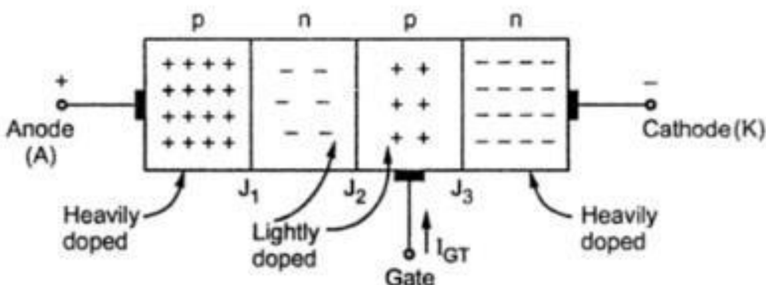


Fig. 6.1 Construction of SCR

Anode must be positive with respect to cathode to forward bias the SCR. But this is not sufficient criterion to turn SCR ON. To make it ON, a current is to be passed through the gate terminal denoted as I_{GT}. Thus it is a **current operated device.**

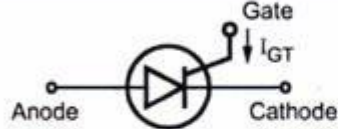


Fig. 6.4 (a) Symbol of SCR

The Fig. 6.4 (a) shows the symbol of SCR. The I_{GT} is the gate trigger current required to make the SCR ON. Basically it is a diode symbol, with a third terminal gate connected to it. Thus the basic material used for the SCR fabrication is silicon whose reverse current is very small compared to the other important semiconductor material like Germanium. The SCR conducts only in one direction and not only that the point at which it starts conduction can be controlled. Due to this, the device is called **silicon controlled rectifier** (SCR).

The operation of SCR is divided into two categories.

1. When gate is open :

Consider that the anode is positive with respect to cathode and gate is open. The junctions J_1 and J_3 are forward biased and junction J_2 is reverse biased. There is depletion region around J_2 and only leakage current flows which is negligibly small. Practically the SCR is said to be **OFF**. This is called **forward blocking state** of SCR and voltage applied to anode and cathode with anode positive is called **forward voltage**. This is shown in the Fig. 6.5 (a).

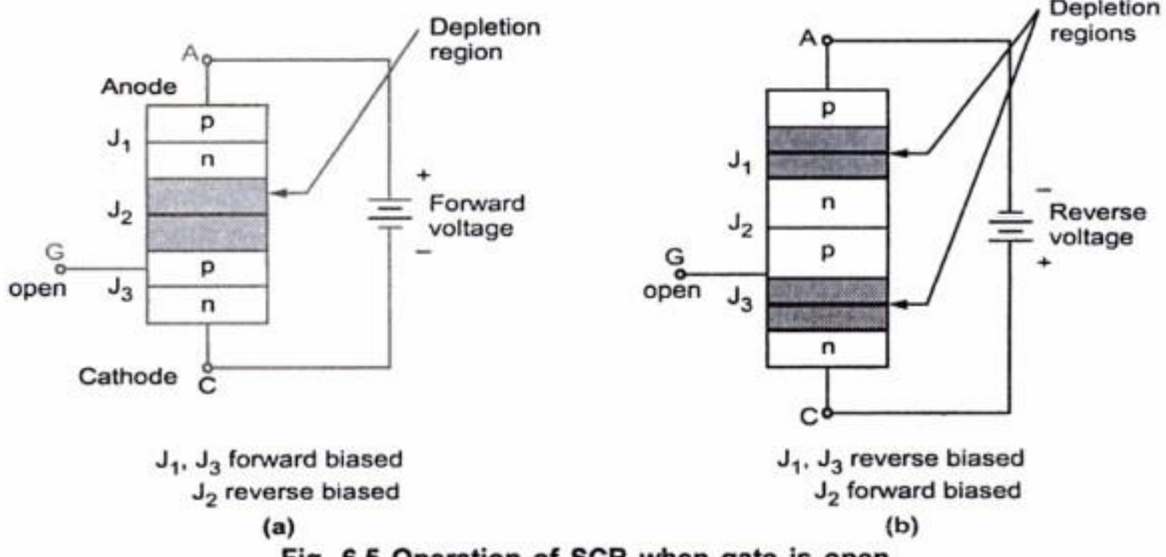


Fig. 6.5 Operation of SCR when gate is open

With gate open, if cathode is made positive with respect to anode, the junctions J_1, J_3 become reverse biased and J_2 forward biased. Still the current flowing is leakage current, which can be neglected as it is very small. The voltage applied to make cathode positive is called **reverse voltage** and SCR is said to be in **reverse blocking state.** This is shown in the Fig. 6.5 (b).

In forward blocking state, if the forward voltage is increased, the current remains almost zero upto certain limit. At a particular value, the reverse biased junction J_2 breaks down and SCR conducts heavily. This voltage is called **forward breakover voltage V_{BO}** of SCR. In such condition, SCR is said to be ON or triggered.

2. When gate is closed :

Consider that the voltage is applied between gate and cathode when the SCR is in forward blocking state. The gate is made positive with respect to the cathode. The electrons from n-type cathode which are majority in number, cross the junction J_3 to reach to positive of battery.

While holes from p-type move towards the negative of battery, this constitutes the gate current. This current increases the anode current as some of the electrons cross junction J_2. As anode current increases, more electrons cross the junction J_2 and the anode current further increases. Due to regenerative action, within short time, the junction J_2 breaks and SCR conducts heavily. The connections are shown in the Fig. 6.6. The resistance R is required to limit the current. Once the SCR conducts, the gate loses its control.

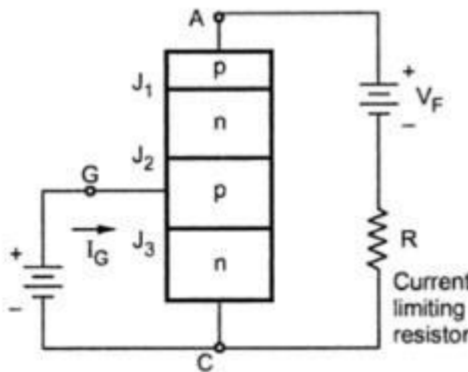


Fig. 6.6 Operation of SCR when gate is closed

Key Point: *Thus if a bias voltage is applied to gate, the value of forward voltage V_F, required to turn ON the SCR decreases. Hence the gate control is more convenient and useful method to turn ON the SCR.*

2. Describe in detail about the characteristics of SCR

The working of the SCR can be discussed into three modes : Reverse blocking mode, forward blocking mode and forward conduction mode. Fig. 6.7 shows the V-I characteristics of the SCR.

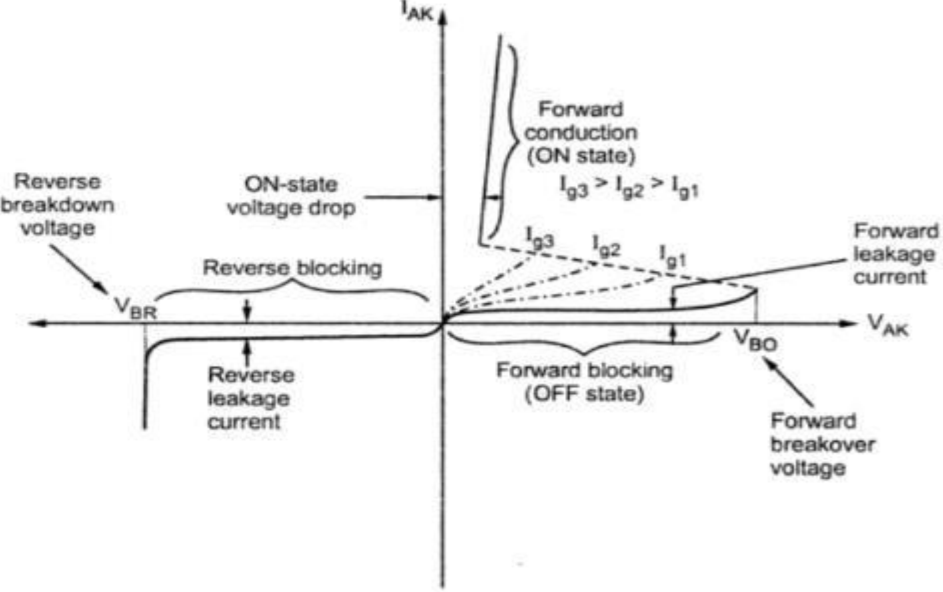


Fig. 6.7 Static V-I characteristics of a SCR

The characteristics shown in the Fig. 6.7 are called static characteristics. The anode to cathode current I_{AK} is plotted with respect to anode to cathode voltage V_{AK}. The voltage 'V_{BO}' is the forward break over voltage. 'V_{BR}' is the reverse break-down voltage. And I_{g1}, I_{g2}, I_{g3} are the gate currents applied to the SCR.

Reverse blocking mode:

Fig. 6.8 shows the situation when the thyristor will be in reverse blocking mode.

In the Fig. 6.8, observe that the anode (A) is made negative with respect to cathode (K). The gate is kept open. There are three PN junctions in the SCR : J_1, J_2 and J_3. Due to this reverse bias, junctions J_1 and J_3 are also reverse biased. And junction J_2 is forward biased. The SCR doesnot conduct due to this reverse bias. A very small current flows from cathode to anode. This current is called *reverse leakage current* of the SCR. This mode is called reverse blocking mode. Fig. 6.7 shows the characteristic of SCR in reverse blocking mode. Observe that reverse voltage increases but very small current flows. At reverse break down voltage (V_{BR}), the reverse current increases rapidly. At the time of reverse breakdown, the high voltage is present across the SCR and heavy current flows through it. Hence large power dissipation takes place in the thyristor. Due to this

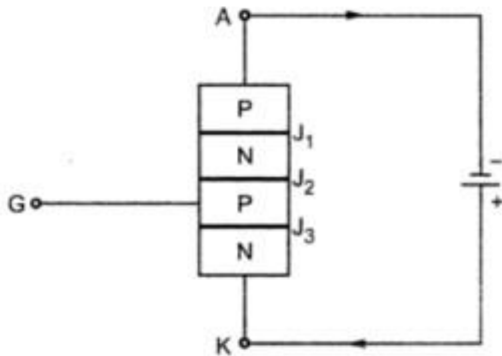


Fig. 6.8 A reverse biased SCR

dissipation, the junction temperature exceeds the permissible value and the SCR is damaged. Hence a reverse voltage across the SCR should never exceed V_{BR}.

During the reverse blocking mode, the positive gate signal should not be applied. If the positive signal is applied between gate and cathode, junction J_3 is forward biased. Hence current starts flowing through it. This current adds to reverse leakage current of the SCR. Hence dissipation is also increased.

6.4.2 Forward Blocking Mode

The SCR is said to be forward biased when anode is made positive with respect to cathode as shown in Fig. 6.9. Due to this forward bias the junction J_1 and J_3 is forward biased and J_2 is reverse biased. Hence the forward voltage is to be hold by junction J_2. A very small current flows from anode to cathode. This current is called forward leakage current. This current is of the order of few milliamperes. In the forward blocking mode, the thyristor is forward biased but it doesnot turn-on. In the forward blocking mode a very small forward leakage current flows. In the forward blocking mode the voltage (V_{AK}) can be increased till V_{BO}. This situation is shown in Fig. 6.7. When the forward voltage reaches V_{BO}, the SCR turns

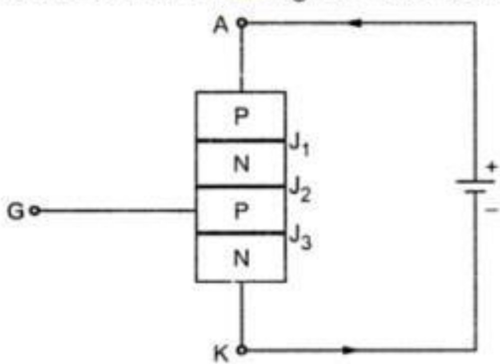


Fig. 6.9 SCR in forward biased condition

on. The SCR goes from forward blocking mode to forward conduction mode. Normally gate drive is applied for this purpose. The highest voltage to be sustained in forward blocking mode is forward break-over voltage, V_{BO}.

When the voltage increases above V_{BO}, the SCR goes into forward conduction mode (i.e. turns-on) even if gate drive is not applied. Thus SCR is not damaged if voltage $V_{AK} > V_{BO}$, rather it is turned-on.

The forward breakover voltage is obtained due to blocking capability of junction J_2. The reverse breakover voltage is obtained due to blocking capabilities of junctions J_1 and J_3. The blocking capability of $(J_1 + J_3)$ combined is higher than that of J_2. Therefore reverse blocking voltage is higher than forward blocking voltage of SCR.

6.4.3 Forward Conduction Mode

When the SCR is forward biased, then it can go into forward conduction by following techniques :

i) When $V_{AK} > V_{BO}$

ii) When gate drive is applied

iii) When $\frac{dv}{dt}$ exceeds permissible value

iv) When gate cathode junction is exposed to light

It shows a forward blocking region, when $I_G = 0$. It also shows that when forward voltage increases upto V_{BO}, the SCR turns ON and high current results. The drop across SCR reduces suddenly which is now the ohmic drop in the four layers. The current must be limited only by the external resistance in series with the device.

It also shows that, if gate bias is used then as gate current increases, less voltage is required to turn ON the SCR.

If the forward current falls below the level of the **holding current** I_H, then depletion region begins to develop around J_2 and device goes into the forward blocking region.

When SCR is turned ON from OFF state, the resulting forward current is called **latching current** I_L. The latching current is slightly higher than the holding current.

3. Explain the two transistor analogy of an SCR +[Nov/Dec 2014]

The easiest way to understand how SCR works is to visualize it separately into two halves, as shown in the Fig. 6.8. The left half is a pnp transistor and right half is npn transistor. This is also called **two transistor model** of SCR.

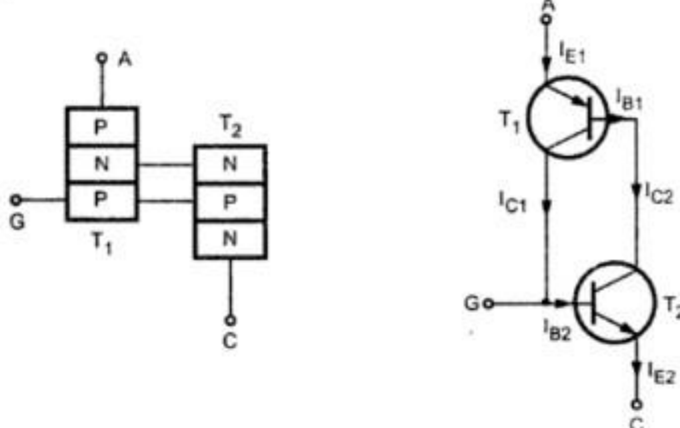


Fig. 6.8 Two transistor model of SCR

The collector current of T_1 becomes base current of T_2 and collector current of T_2 becomes base current of T_1. Consider a positive voltage on the anode with respect to the cathode and gate current is zero. As gate current is zero, base current of T_2, I_{B2} is zero and I_{C2} is approximately I_{C0}. The base current of T_1, $I_{B1} = I_{C2} = I_{C0}$, is too small to turn T_1 ON. Both transistors are therefore in the "OFF" state, resulting in a high impedance between the collector and emitter of each transistor. The anode current is then just the sum of the leakage currents of the two transistors, $I_{C01} + I_{C02}$.

Let us see what happens when we apply positive voltage from gate to cathode. Upon applying positive gate voltage holes are injected into the base of T_2. This forward biases the base emitter junction of T_2, increasing I_{C2}. This collector current is the base current for T_1, therefore increase in I_{C2} (I_{B1}) will increase collector and emitter

currents of T_1, resulting increase in base current of T_2. The increase in base,

T_2 will result in a further increase in I_{C2}. The net result is a regenerative increase in the collector current of each transistor. This regenerative process is continuous until both transistors are driven into saturation making all junctions forward biased. This results in large anode current (IA) which is limited only by the external circuit resistance and voltage.

Key Point: *Once the SCR turns ON, due to the regenerative action, the gate voltage can be removed and the SCR still remains ON. Therefore, gate signal is required only for turning on the SCR.*

Mathematical analysis :

Let I_{C1} and I_{C2} are collector currents, I_{E1} and I_{E2} are emitter currents while I_{B1} and I_{B2} are base currents of transistors T_1 and T_2. Let both the transistors are operating in active region. From transistor analysis we can write,

$$I_{C1} = \alpha_1 I_{E1} + I_{C01} \text{ and } I_{C2} = \alpha_2 I_{E2} + I_{C02}$$

where I_{C0} = Reverse current or leakage current

and $\alpha = \dfrac{\beta}{1+\beta}$

Now $I_{E2} = I_{C2} + I_{B2}$ ... (1)

I_A = Anode current = I_{E1}

I_K = Cathode current = I_{E2}

I_G = Gate current

Now $I_K = I_A + I_G$ ... (2)

$$\therefore\ I_{E2} = I_A + I_G = I_{C2} + I_{B2} \quad \text{... (3)}$$

But $$I_{B2} = I_{C1} + I_G \quad \text{... (4)}$$

$$\therefore\ I_A + I_G = I_{C2} + I_{C1} + I_G \quad \text{... (5)}$$

Substituting I_{C1} and I_{C2},

$$\therefore\ I_A = \alpha_1 I_{E1} + I_{C01} + \alpha_2 I_{E2} + I_{C02} \quad \text{... (6)}$$

$$\therefore\ I_A = \alpha_2 (I_A + I_G) + \alpha_1 I_A + I_{C01} + I_{C02} \quad \text{... Using (3)}$$

$$\therefore\ I_A - \alpha_2 I_A - \alpha_1 I_A = \alpha_2 I_G + I_{C01} + I_{C02}$$

$$\therefore\ \boxed{I_A = \frac{\alpha_2 I_G + I_{C01} + I_{C02}}{1 - (\alpha_1 + \alpha_2)}} \quad \text{... (7)}$$

In blocking state α_1 and α_2 are small. Thus I_A is small. As $\alpha_1 + \alpha_2$ approaches unity, the SCR is ready to enter into conduction. Then due to positive gate current, the regenerative action takes place and SCR conducts.

4. Explain the methods to turn ON and OFF SCR.

6.2.6 Methods of Turning ON SCR

There are five basic methods of triggering of SCR.

1. Thermal Triggering : We know that the width of depletion layer of a semiconductor decreases as temperature increases. Thus in a SCR if applied voltage is very near the break down voltage, the increase in temperature can trigger the SCR.

2. Radiation Triggering : The SCR can be triggered by bombarding photons which results electron-hole pairs. Such triggering is called radiation triggering and such SCR are called LASCR (Light-Activated SCRs).

3. Voltage Triggering : An increase in forward biased voltage causes, the electrons and holes to concentrate at reverse biased junction. This increases the blocking current and the SCR is triggered.

4. dV/dt Triggering : If the rate of rise of voltage exceeds the critical rate of rise of voltage, SCR is triggered.

5. Gate Triggering : This is the most easy and useful method of turning ON SCR. While designing the gate control circuit the following points must be considered.

i) When the SCR is forward biased, appropriate gate-to-cathode voltage must be applied to turn ON SCR.

ii) To reduce losses and higher junction temperatures, gate signal should be removed after the SCR is turned ON.

iii) No gate signal should be applied when the SCR is reverse biased.

iv) To improve the characteristics of the SCR, negative voltage should be applied between gate and cathode when the SCR is in the OFF state.

There are three ways to turn SCR ON by gate control which are,

a) **By d.c. gate signal :** In this method, a d.c. voltage of proper polarity and magnitude is applied between gate and cathode.

b) **By a.c. gate signal :** In this method, a.c. voltage is applied between gate and cathode. It is shifted a.c. voltage which is derived from the mains supply.

c) **By pulsed gate signal :** In this method, a pulsed waveform is applied to gate. The pulse occurs periodically at the gate. Due to pulse signal, the gate current is not continuous hence losses are less and gate isolation is achieved.

6.2.7 Turn OFF Mechanism

The SCR can be brought back to the forward blocking state from the conduction state only by reducing the forward current to a level below that of the holding current. In AC circuits where the current goes through a natural zero value, the SCR will be automatically turned off.

5. Explain principle of working of GTO. [Nov/Dec 2015]

Construction:

At the beginning of the chapter we discussed structure and working of SCR. The SCR is most commonly used member of thyristor family. But SCR needs external circuits for turn-off. Now we present another thyristor, called GTO. The GTO can be turned-off by gate drive. Thus gate has full control over the operation of GTO. Fig. 6.73 shows the structure of GTO.

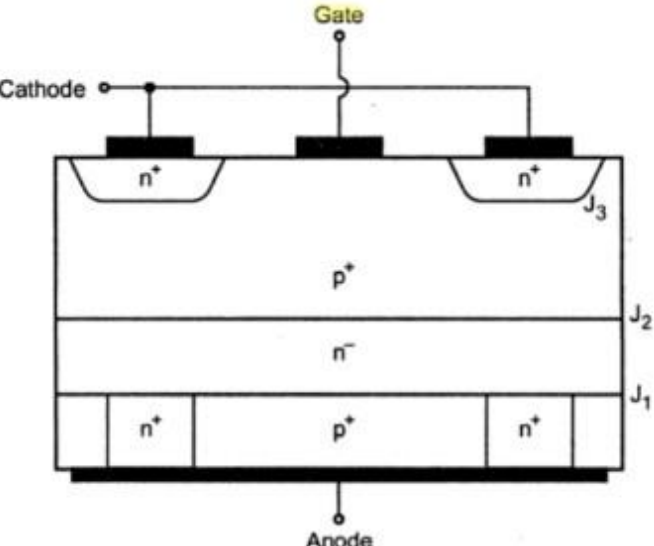


Fig. 6.73 Structure of GTO

Observe that the structure of GTO is almost similar to SCR. But there are significant differences that make GTO different than SCR. These differences are :

i. Gate and cathodes are highly interdigited with various geometric forms. This maximizes periphery of the cathode and minimize gate-cathode distance.

ii. There are n^+ regions at regular intervals in the p^+ anode layer. This n^+ layer makes direct contact with n^- layer. This is called anode short. This speeds up the turn-off mechanism of GTO.

iii. The operation of GTO can be explained with the help of two transistor analogy. The gain of pnp transistor is reduced. This reduces the regenerative action. Hence turn-off of GTO can be achieved by negative current from gate.

Fig. 6.74 shows the symbol of GTO.

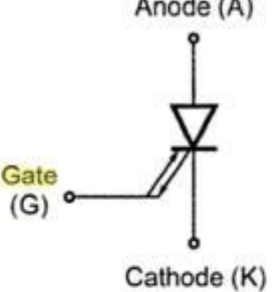


Fig. 6.74 Symbol of GTO

Observe that there is double arrow on the gate. This indicates that bidirectional current flows through the gate. The rest of the symbol is similar to SCR.

Characteristics of GTO:

Fig. 6.75 shows the V-I characteristics of GTO.

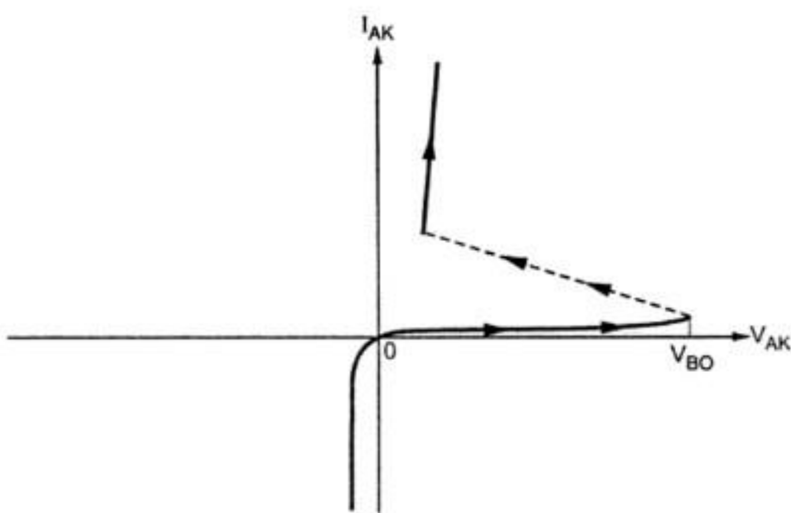


Fig. 6.75 V-I characteristics of GTO

In this figure observe that the V-I characteristics of GTO in forward direction are similar to that of SCR. But in reverse direction GTO has virtually no blocking capability. Observe that GTO starts conducting in reverse direction after very small reverse (20 to 30 V) voltage. This is because of the anode short structure.

In Fig. 6.73 observe that junction J_3 blocks reverse voltages. But J_3 has very small reverse breakdown voltage. Thus GTO has asymmetric voltage blocking capability.

6.21.3 Advantages, Limitations and Applications of GTO

6.21.4 Advantages

i. Higher voltage blocking capability.

ii. Gate has full control over the operation of GTO.

iii. Low on-state loss.

iv. High ratio of peak surge current to average current.

v. High on-state gain.

6.21.5 Limitations

i. GTOs require large negative gate currents for turn-off. Hence they are suitable for low power applications.

ii. Very small reverse voltage blocking capability.

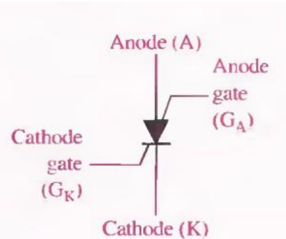
iii. Switching frequencies are very small.

6.21.6 Applications

i. GTOs are suitable mainly for low power applications.

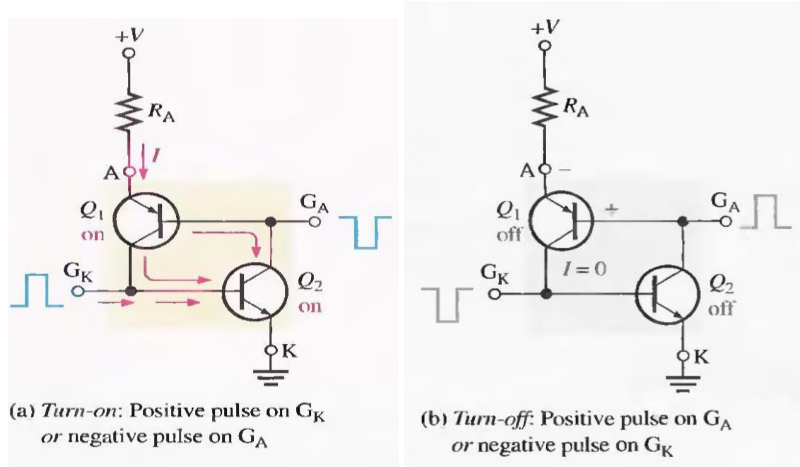
ii. Induction heating and motor drives.

6. Expalin in detail about construction,working and characterisitics of SCS .



- An SCS (silicon-controlled switch) is a four-terminal thyristor that has two gate terminals that are used to trigger the device ON and OFF.
- The symbol and terminal identification for an SCS are shown in Figure.
- A positive pulse on the cathode gate drives Q_2 into conduction and thus provides a path for Q_1 base Current.
- When Q_1 turns on, its collector Current provides base current for Q_2 thus sustaining the ON state of the device. This regenerative action is the same as in the turn-on process of the SCR and the 4-1ayer diode.
- The SCS can also be turned on with a negative pulse on the anode gate, as indicated in Figure 4(b). This drives Q_1 into conduction which, in turn, provides base current for $Q_{2.}$ Once Q_2 is on, it provides a path for Q_2, base current, thus sustaining the ON state.
- To turn the SCS off, a positive pulse is applied to the anode gate.
- This reverse-biases the base-emitter junction of Q_1 and turns it off, because of this Q_2 also turn off and the SCS ceases conduction, is shown in figure 4(c).

➢ The device can also be turned off with a negative pulse on the cathode gate, as indicated in 4(c). The SCS typically has a faster turn-off time than the SCR.



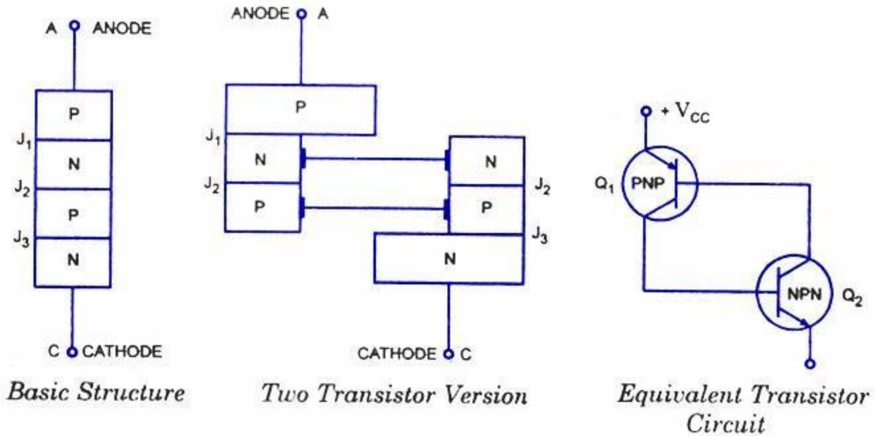
(a) *Turn-on*: Positive pulse on G_K *or* negative pulse on G_A

(b) *Turn-off*: Positive pulse on G_A *or* negative pulse on G_K

Applications

The SCS and SCR are used in similar applications. The SCS has the advantage of faster turn-off with pulses on either gate terminal; however, it is more limited in term of maximum current and voltage ratings. Also, the SCS is sometimes used in digital applications such as counters, registers, and timing circuits.

7. Explain the construction, working of Shockley diode in detail.



Basic Structure *Two Transistor Version* *Equivalent Transistor Circuit*

The four-layer diode, also called the Shockley diode after its inventor William Shockley, is essentially a low-current SCR without a gate. It is classified as a diode because it has only two external terminals through anode and cathode. Because of its four doped regions it is often called a P-N-P-N diode.

Construction:

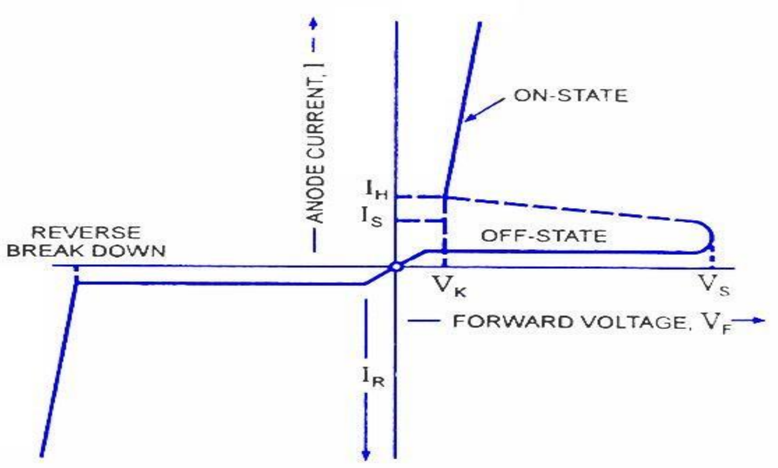
➢ The basic structure, two transistor version, equivalent transistor circuit and schematic symbol of a Shockley diode are shown in figure.

- The easiest way to understand how it operates is to visualize it to be formed of two transistors Q1 and Q2 placed back to back, as shown in figure.b.
- Figure shows the diode split-up into two parts, displaced mechanically but connected electrically.
- The left half is a P-N-P transistor while the right half is an N-PN- transistor. It may be seen that N-type base region of P-N-P transistor forms the collector of N-P-N transistor while P-type base of N-P-N transistor forms the collector of P-N-P transistor.
- Thus the four-layer diode is equivalent to the latch shown in figure.

Working:

- Because there are no trigger inputs, the only way to switch the device on is to increase the anode-to-cathode voltage V_{AK} to the forward switching voltage, and the only way to open it is by low current drop out.
- With a four layer diode it is not necessary to reduce the current all the way to zero to open the latch. The internal transistors of the device will come out of saturation when the current is reduced to a low value, called the holding current.
- The forward switching voltage V_s is equivalent of the SCR forward breakover voltage and the minimum current at which device will switch on is the switching current I_S.

Break over Characteristic of Shockley Diode:



Breakover Characteristic of Shockley Diode

Voltage-current characteristic of a Shockley diode is shown in figure. The device has two operating states: conducting and non-conducting.

- In non-conducting state, it operates on lower line with negligible current and a voltage less than switching voltage or break over voltage.
- When the voltage tries to exceed the break over voltage, the device breaks down and switches along the dotted line to the conducting or on-state.

- The dotted line indicates an unstable or a temporary condition. The device can have current and voltage values on this dotted line only briefly as it switches between the two stable operating states. In conducting state or in on-state, the device operates on the upper line.
- As long as the current through the device is greater than the holding current I_H, then the voltage across it is slightly greater than knee voltage, V_K.
- When the current falls below the level of the holding current I_H, the device switches back along the dotted line to the non-conducting or off-state.

Application of Shockley Diode:

- One common application of the Shockley diode is as a trigger switch for an SCR.
- When the circuit is energized, the capacitor will start getting charged and eventually, the voltage across the capacitor will be sufficiently high to first turn-on Shockley diode and then the SCR
- Another application of this diode is as a relaxation oscillator.

8. Explain the construction, working and characteristics of UJT in detail.

A unijunction transistor (UJT) is a device which does not belong to thyristor family but is used to turn ON SCRs.

Construction:

It is a three terminal device, having two layers. It consists of a slab of lightly doped n type silicon material. The two base contacts are attached to both the ends of this n type surface. These are denoted as B_1 and B_2 respectively. A p type material is used to form a p-n junction at the boundary of the aluminium rod and n type silicon slab. The third terminal called emitter (E) is taken out from this p-type material. The n-type is lightly doped while p type is heavily doped. The basic construction is shown in the Fig. 6.30.

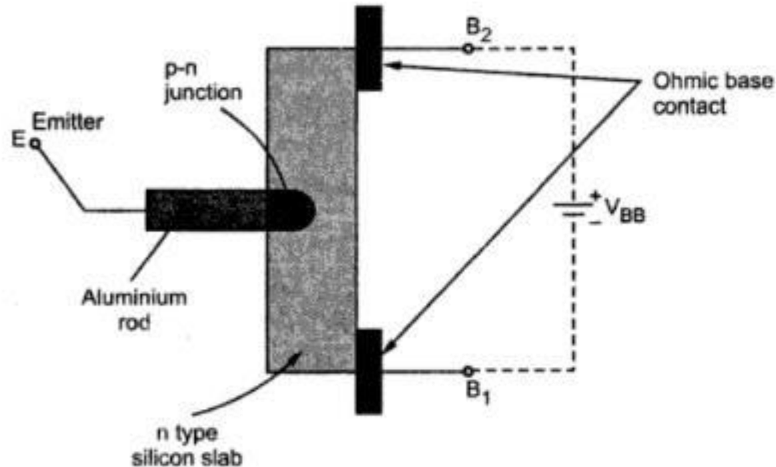


Fig. 6.30 Construction of UJT

As n type is lightly doped, it provides high resistivity and p type as heavily doped, provides low resistivity.

The symbolic representation of UJT is shown in the Fig. 6.31. The emmiter is shown by an arrow which is at an angle to the vertical line representating n type material. This arrow indicates the direction of flow of conventional current when the UJT is forward biased.

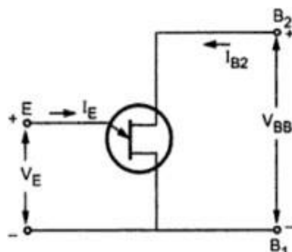
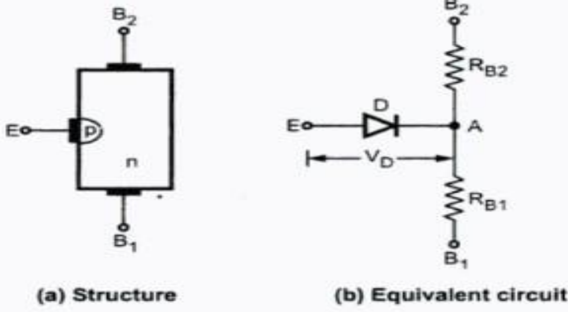


Fig. 6.31 Symbol of UJT

EQUIVALENT CIRCUIT OF UJT

The Fig. 6.32 (a) shows the basic structure of UJT while the Fig. 6.32 (b) shows the equivalent circuit of UJT.



(a) Structure **(b) Equivalent circuit**

Fig. 6.32

The internal resistances of the two bases are represented as R_{B1} and R_{B2}. In the actual construction, the terminal E is closer to B_2 as compared to B_1. Hence resistance R_{B1} is more than the resistance R_{B2}. The p-n junction is represented by a normal diode with V_D as the drop across it.

When the emitter diode is not conducting then the resistance between the two bases B_1 and B_2 is called **interbase resistance** denoted as R_{BB}.

$$\therefore \quad R_{BB} = R_{B1} + R_{B2}$$

Its value ranges between 4 kΩ ~~and~~ 12 kΩ.

6.5.3 Intrinsic Stand Off Ratio (η)

Consider UJT as shown in the Fig. 6.33 to which supply V_{BB} is connected. With $I_E = 0$ i.e. emitter diode is not conducting,

$$R_{BB} = R_{B1} + R_{B2}$$

Then the voltage drop across R_{B1} can be obtained by using potential divider rule.

$$V_{RB1} = \frac{R_{B1}\, V_{BB}}{R_{B1} + R_{B2}} = \eta\, V_{BB} \quad \text{... when } I_E = 0$$

Then $$\eta = \text{Intrinsic stand off ratio} = \left.\frac{R_{B1}}{R_{B1} + R_{B2}}\right|_{I_E=0}$$

$$\eta = \left.\frac{R_{B1}}{R_{BB}}\right|_{I_E=0}$$

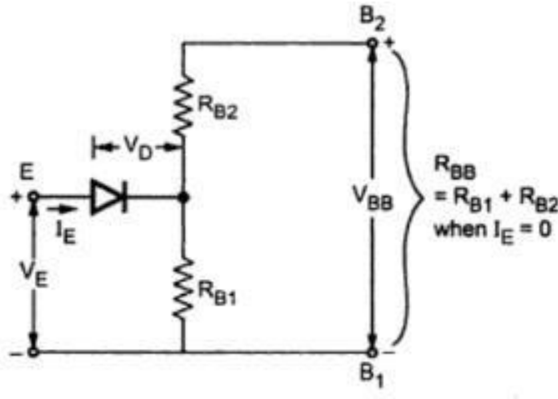


Fig 6.33

The typical range of η is from 0.5 to 0.8. The voltage V_{RB1} is called **intrinsic stand off voltage** because it keeps the emitter diode reversed biased for all the emitter voltages less than V_{RB1}.

PRINCIPLE OF OPERATION:

While operating an UJT, the supply V_{BB} is applied between B_2 and B_1 while the variable emitter voltage V_E is applied across the emitter terminals. This arrangement is shown in the Fig. 6.34.

Let us see the effect of change in V_E. The potential of A is decided by η and is equal to $\eta\, V_{BB}$.

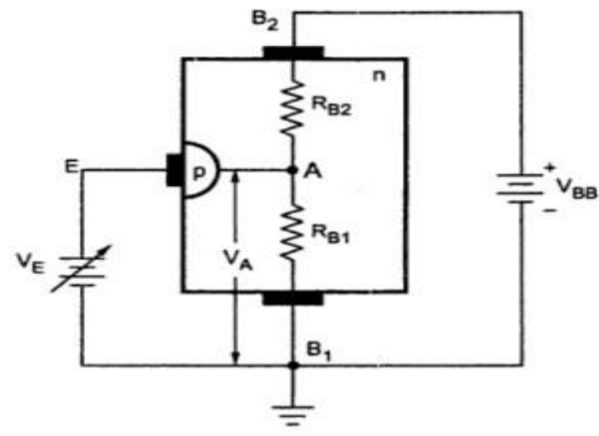


Fig. 6.34

Case 1 : $V_E < V_A$

As long as V_E is less than V_A, the p-n junction is reverse biased. Hence emitter current I_E will not flow. Thus UJT is said to be OFF.

Case 2 : $V_E > V_P$

The diode drop V_D is generally between 0.3 to 0.7 V. Hence we can write,

$$V_P = V_A + V_D = \eta\, V_{BB} + V_D$$

When V_E becomes equal to or greater than V_P the p-n junction becomes forward biased and current I_E flows. The UJT is said to be ON.

CHARACTERISITCS OF UJT

The graph of emitter current against emitter voltage plotted for a particular value of V_{BB} is called the characteristics of UJT. For a particular fixed value of V_{BB} such characteristics is shown in the Fig. 4.5.

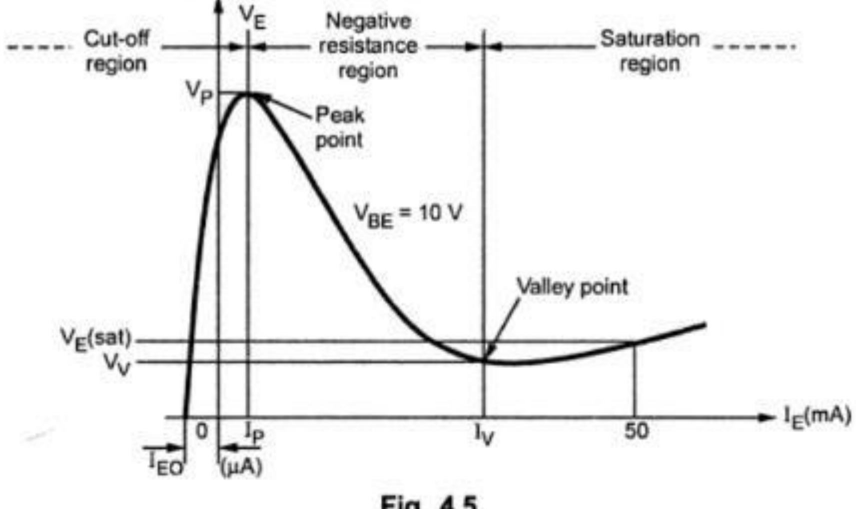


Fig. 4.5

The characteristics can be divided into three main regions which are,

1. **Cut-off region :** The emitter voltage V_E is less than V_P and the p-n junction is reverse biased. A small amount of reverse saturation current I_{E0} flows through the device, which is negligibly small of the order of µA. This condition remains till the peak point.

2. **Negative resistance region :** When the emitter voltage V_E becomes equal to V_P the p-n junction becomes forward biased and I_E starts flowing. The voltage across the device decreases in this region, though the current through the device increases. Hence the region is called negative resistance region. This decreases the resistance R_{B1}. This region is stable and used in many applications. This region continues till valley point.

3. **Saturation region :** Increase in I_E further valley point current I_V drives the device in the saturation region. The voltage corresponding to valley point is called **valley point voltage** denoted as V_V. In this region, further decrease in voltage does not take place. The characteristic is similar to that of a semiconductor diode, in this region.

The active region i.e. negative resistance region, the holes which are large in number on p-side, get injected into n-side. This causes increase in free electrons in the n-type slab. This increases the conductivity i.e. decreases the resistivity. Hence the resistance R_{B1} decreases in this region.

As the V_{BB} increases, the potential V_P corresponding to peak point will increase.

4.1.6 Applications

The UJT is mainly used in the triggering of other devices such as SCR. It is also used in the sawtooth wave generators and some timing circuits. The most popular application of UJT is as a relaxation oscillator to obtain short pulses for triggering of SCRs.

9. Explain the working of UJT as a relaxation oscillator with necessary waveform and equations. [Nov/Dec 2014]

4.1.7 UJT Relaxation Oscillator

The pulse signal required to drive the digital circuits can be obtained from a single stage oscillator circuits using a particular device like unijunction transistor. Such a oscillator which uses UJT is called UJT relaxation oscillator. The basic circuit of UJT relaxation oscillator is shown in the Fig. 4.6.

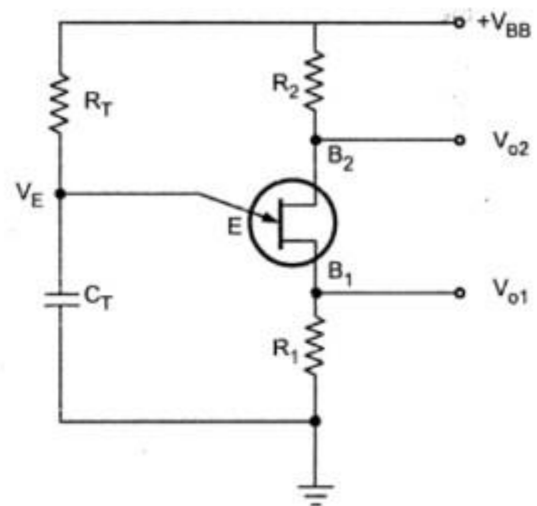


Fig. 4.6 UJT relaxation oscillator

The R_1 and R_2 are biasing resistances which are selected such that they are lower than interbase resistances R_{B1} and R_{B2}. The resistance R_T and the capacitance C_T decide the oscillating rate. The value of R_T is so selected that the operating point of UJT remains in the negative resistance region. The UJT characteristics and the negative resistance region of the characteristics are shown in the Fig. 4.7. The characteristics of UJT shows the variation between V_E and I_E, where V_E is emitter voltage and I_E is emitter current.

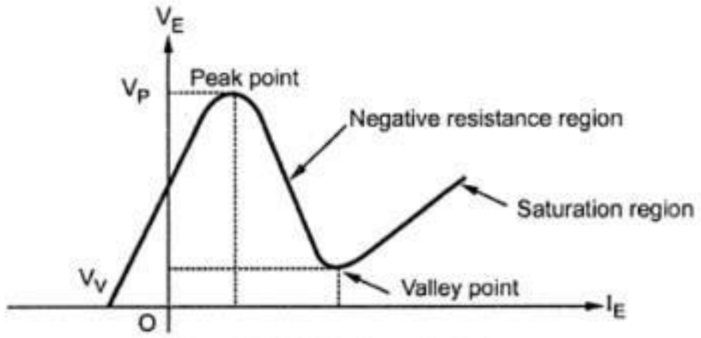


Fig. 4.7 UJT characteristics

Operation

Capacitor C_T gets charged through the resistance R_T towards supply voltage V_{BB}. As long as the capacitor voltage is less than peak voltage V_P, the emitter appears as an open circuit.

$$V_P = \eta V_{BB} + V_D \qquad \text{... (1)}$$

where η = Stand off ratio of UJT

V_D = Cut-in voltage of diode

When the capacitor voltage V_C exceeds the voltage V_P, the UJT fires. The capacitor starts discharging through $R_1 + R_{B1}$ where R_{B1} internal base resistance. As R_{B1} is assumed negligible and hence capacitor discharges through R_1.

Due to the design of R_1, this discharge is very fast, and it produces a pulse across R_1. When the capacitor voltage falls below V_V i.e. $V_C = V_E = V_V$, the UJT gets turned OFF. The capacitor starts charging again.

The discharge time of the pulse is controlled by the time constant $C_T R_1$ while the charging time constant by $R_T C_T$. The waveforms are shown in the Fig. 4.8.

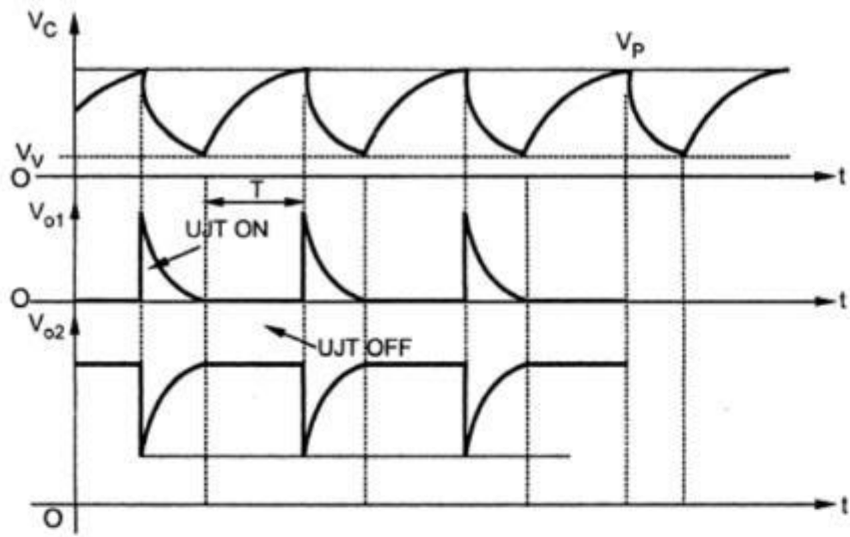


Fig. 4.8 Waveforms of UJT relaxation oscillator

There is voltage drop across R_2 and voltage rise across R_1, when UJT fires.

The charging equation of the capacitor is given by,

$$V_{C(t)} = V_V + V_{BB}\left[1 - e^{-t/R_T C_T}\right] \quad \text{... (2)}$$

But $\quad V_{C(t)} = V_P, \text{ at } t = T$

$$V_P = V_V + V_{BB}\left[1 - e^{-1/R_T C_T}\right] \quad \text{... (3)}$$

Using the equation (1),

$$\therefore \quad \eta V_{BB} + V_D = V_V + V_{BB}\left[1 - e^{-T/R_T C_T}\right] \quad \text{... (4)}$$

Neglecting V_D and V_V to get approximate relation for T.

$$\therefore \quad \eta = 1 - e^{-T/R_T C_T}$$

$$\therefore \quad T = R_T C_T \, ln\left[\frac{1}{1-\eta}\right] \quad \text{... (5)}$$

$$\therefore \quad \boxed{f_0 = \frac{1}{T} = \frac{1}{R_T C_T \, ln\left[\frac{1}{1-\eta}\right]}} \quad \text{... (6)}$$

Where $\quad f_0$ = Oscillating frequency

Condition to turn ON and OFF

To ensure turn ON of UJT, I_E should not be less than I_P at the peak point. To achieve this,

$$V_{BB} - V_P > I_P R_T$$

$$\therefore \quad R_T < \frac{V_{BB} - V_P}{I_P} \quad \text{... Turn ON condition}$$

To turn OFF the device, I_E at the valley point must be less than I_V specified. Thus voltage across R_T must be less than $I_V R_T$.

$$\therefore \quad V_{BB} - V_V < I_V R_T$$

$$\therefore \quad R_T > \frac{V_{BB} - V_P}{I_P} \quad \text{... Turn OFF condition}$$

Hence the range of R_T for the proper turn ON and OFF is,

$$\frac{V_{BB} - V_P}{I_P} > R_T > \frac{V_{BB} - V_V}{I_V}$$

10. Explain the construction and working of DIAC in detail

The diac is a two terminal, four layer device. It conducts in either directions hence it is also called bilateral trigger diode. It has a pair of four layer diodes a shown in the Fig. 4.28 (a). The two different symbols used for the diac are shown in the Fig. 4.28 (b).

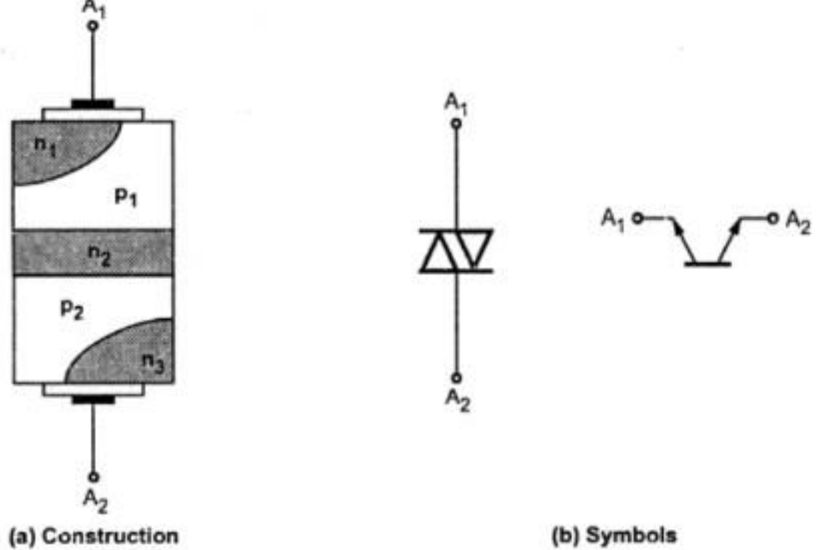


Fig. 4.28 Diac

The terminals of the diac are not named as it can be used in any direction. It is low power triggering device. There is no control terminal on the diac.

Basic operation

The diac can be treated as parallel inverse combination of the semiconductor layers that permits triggering in either direction. The Fig. 4.29 (a) shows the diac equivalent circuit as two parallel Shockley diodes, connected in opposite directions. The Shockley diode is basically a four layer pnpn diode, with only two external terminals. The characteristics of Shockley diode are similar to SCR with $I_G = 0$. It acts as a switch which is on in one direction and off in the other. Both the Shockley diodes act as a switch as shown in the Fig. 4.29 (b). The V is the applied voltage across A_1 and A_2.

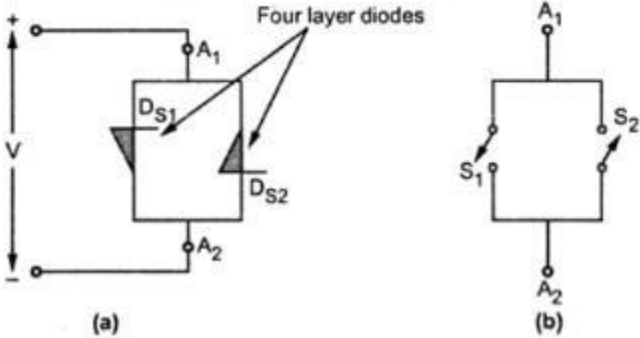


Fig. 4.29 Diac operation

When the polarity of applied voltage is as shown in the Fig. 4.29 (a) then Shockley diode D_{S1} becomes ON when V is more than $V_{BR(F)}$ of D_{S1}. Thus current flows from A_1 to A_2 as D_{S1} acts as closed switch S_1. If the polarities of applied voltage V are reversed then for applied voltage more than $V_{BR(F)}$ of D_{S2}, the D_{S2} conducts and its acts like a closed switch S_2. The current flows from A_2 to A_1. Thus device can conduct in both the directions, depending on the polarities of the applied voltage across it.

4.5.1.2 Four Transistors Analogy

The diac operation can be explained using four transistors analogy. Each pair of transistors form a Shockley diode. The four transistors analogy and the biasing conditions shown in the Fig. 4.30 (a) and (b) also can be used to explain the basic operation of diac.

Four transistor analogy

The diac operation can be explained using four transistors analogy. Each pair of transistors form a Shockley diode. The four transistors analogy and the biasing conditions shown in the Fig. 4.30 (a) and (b) also can be used to explain the basic operation of diac.

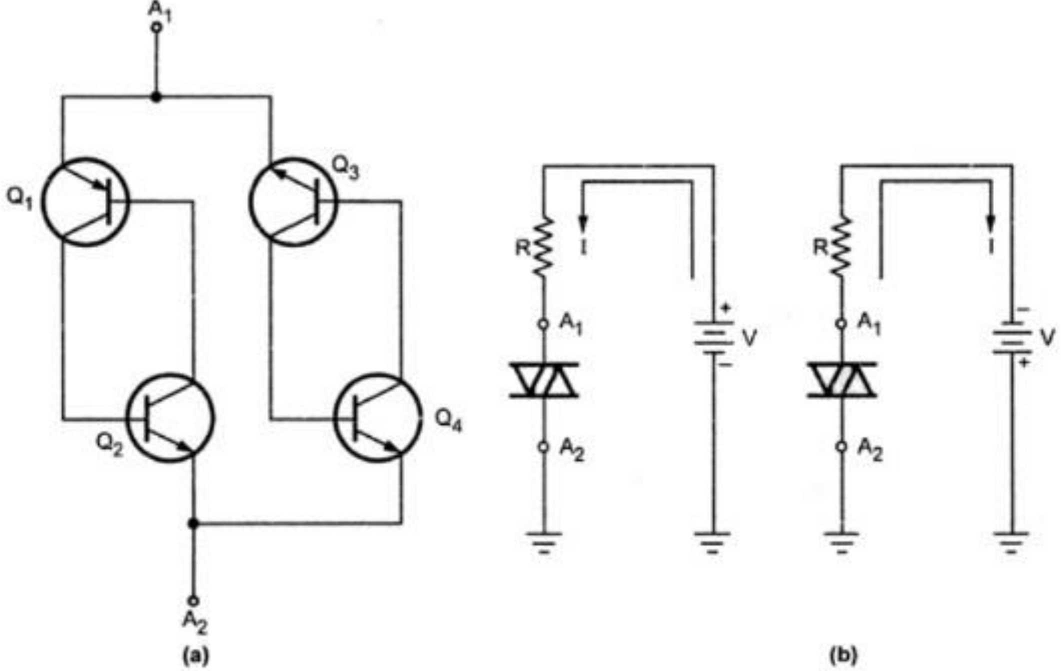


Fig. 4.30 Four transistors analogy

The transistors Q_1, Q_2 form a Shockley diode D_{S1} while the transistors Q_3, Q_4 form a Shockley diode D_{S2}. The basic operation remains same as explained earlier.

4.5.2 Characteristics

The diac characteristics are exactly similar to the Shockley diode. But for one Shockley diode, they are in 1st quadrant while for other they are in 3rd quadrant due to opposite polarities of voltage and current. The diac characteristics are shown in the Fig. 4.31.

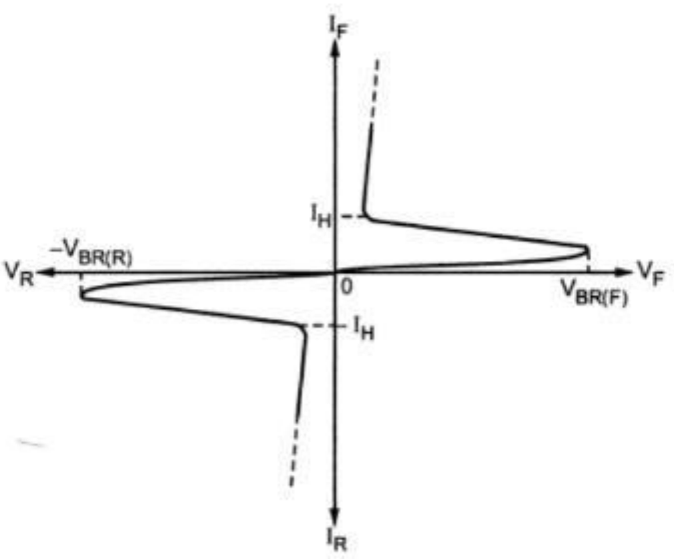


Fig. 4.31 Diac characteristics

4.5.3 Applications

The diac is not a control device, it is used as a triggering device. It is used in,

1. Triggering of triac
2. Motor speed control
3. Temperature control
4. Light dimming circuits.

11. Explain the construction and working of DIAC in detail

4.6 Triac

The triac is another important member of the thyristor family. It is basically two parallel SCRs turned in opposite directions, with a common gate terminal.

Key Point : *It is a bidirectional device and can conduct in both the directions.*

The Fig. 4.34 (a) shows the basic construction of a triac. The Fig. 4.34 (b) shows the symbol of a triac. The Fig. 4.34 (c) shows an equivalent circuit of a triac which is antiparallel connection of the two SCRs.

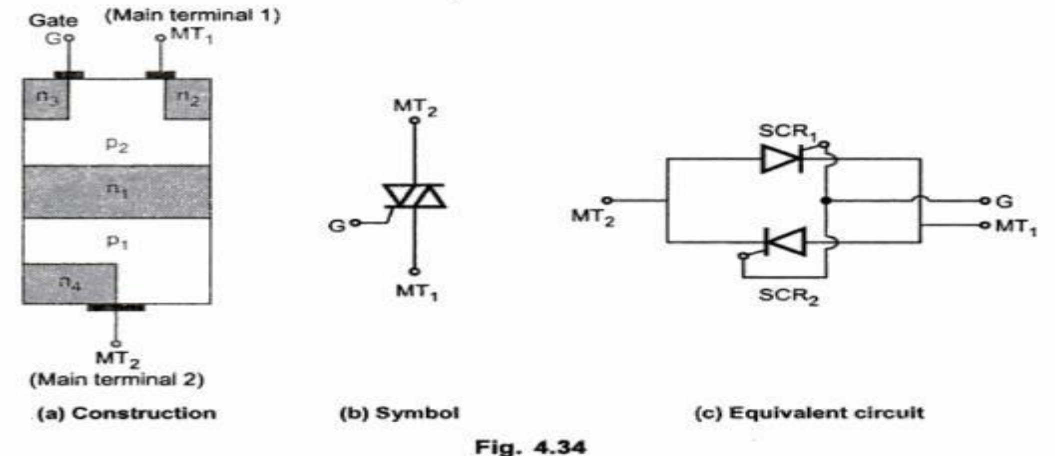


Fig. 4.34

As triac conducts both ways, anode-cathode terminology is not used. The two main electrodes are called **main terminals** MT_1 and MT_2 while common control terminal is called **gate** G. The gate terminal is near MT_1. The triac can be turned ON by applying either a positive or negative voltage to the gate G with respect to the main terminal MT_1.

Working of TRIAC

With gate open, either MT_1 is positive with respect to MT_2 or MT_2 is positive with respect to MT_1.

Forward blocking region : When gate is open and MT_2 is positive with respect to MT_1 but the voltage is less than forward breakover voltage then triac does not conduct. This region is called **forward blocking region.** If this voltage is increased beyond breakover voltage, the triac conducts in the forward direction similar to SCR.

Reverse blocking region : When gate is open and MT_2 is negative with respect to MT_1 but the voltage is less than breakover voltage then triac does not conduct. This region is called **reverse blocking region.** But note that if this voltage is increased beyond the breakover voltage, triac conducts in reverse direction while SCR does not conduct in reverse direction at all.

In forward or reverse blocking, now if gate is made positive or negative with respect to MT_1 then also the triac conducts. This is the gate control of triac and easy way of switching triac ON.

The connections for forward and reverse blocking are shown in the Fig. 4.35 (a) and (b).

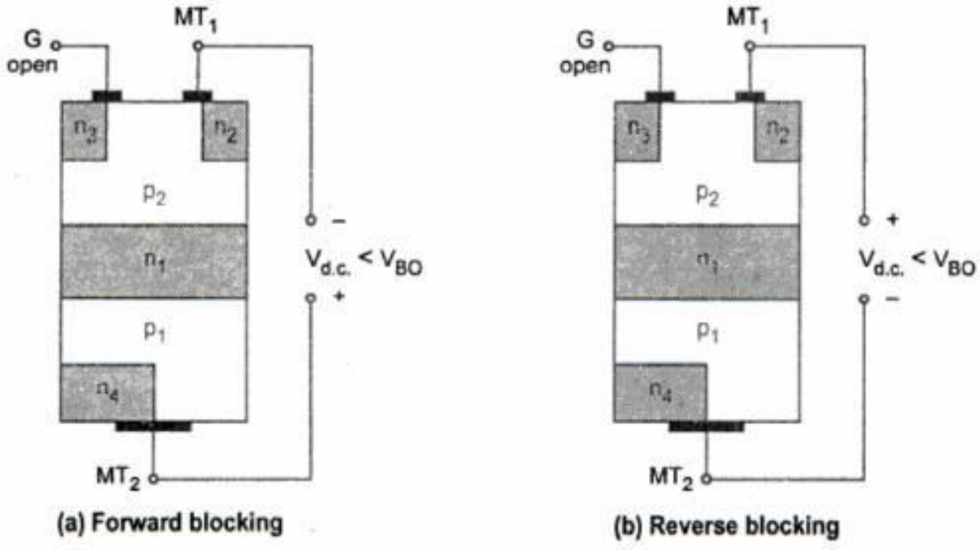
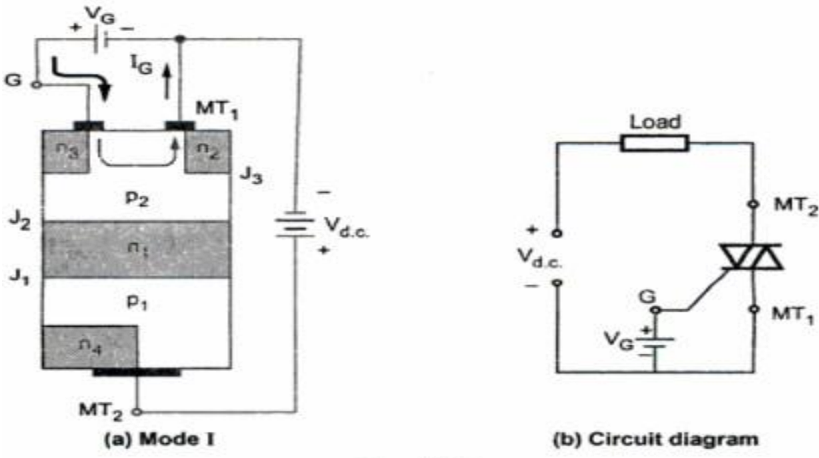


Fig. 4.35

Key Point *: When* MT_2 *is positive and* MT_1 *is negative, triac is forward biased while when* MT_1 *is positive and* MT_2 *is negative, triac is reverse biased.*

Operating modes of triac : In each biased state, gate can be positive or negative. This gives four different operating modes of triac.

1. Mode I : In this mode, triac is forward biased and gate is made positive with respect to MT_1. This is shown in the Fig. 4.36 (a). The terminal MT_2 is positive with respect to MT_1 as triac is forward biased.



(a) Mode I (b) Circuit diagram

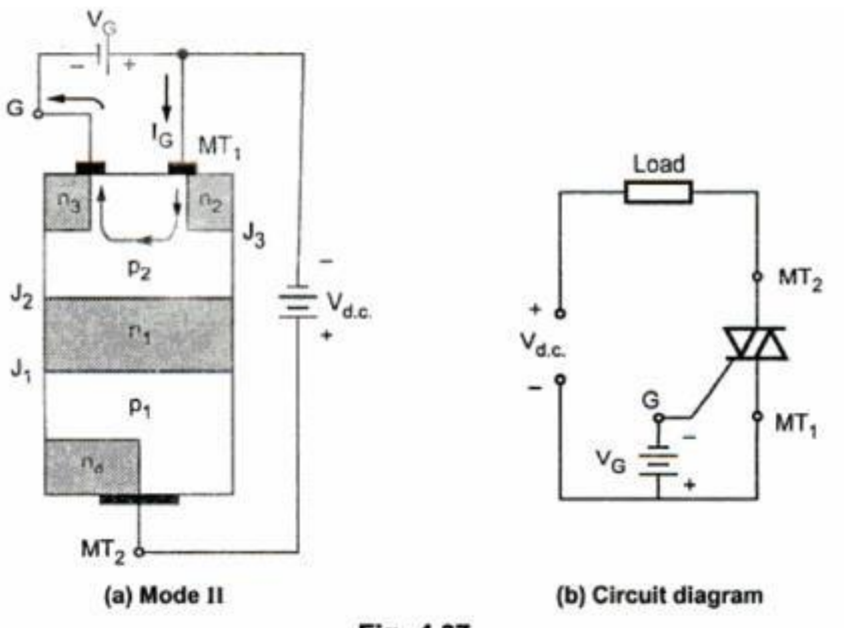
Fig. 4.36

This arrangement forward biases $p_2 - n_2$ junction and the breakdown occurs as a normal SCR.

The gate current is positive and the triac is said to be operating in the first quadrant of its V-I characteristics. Hence this mode is also called I^+ mode of operation.

2. Mode II : In this mode, triac is forward biased and gate is made negative with respect to MT_1. This is shown in the Fig. 4.37 (a).

The negative gate in this arrangement forward biases $p_2 - n_3$ junction. This injects carriers in p_2 to turn SCR ON.



(a) Mode II (b) Circuit diagram

Fig. 4.37

Thus $p_1 n_1 p_2 n_3$ acts as pilot SCR and later on the final conduction takes place as $p_1 n_1 p_2 n_2$, which is main SCR. The sensitivity to gate current is less in this mode. The gate current is negative but triac still operates in first quadrant of its V-I characteristics. Due to negative gate, this mode is also called I^- mode of operation.

3. Mode III : In this mode, triac is reverse biased i.e. MT_1 is positive with respect to MT_2 and the gate is made positive as shown in the Fig. 4.38. (See Fig. 4.38 on next page.)

The gate current flows from p_2 to n_2 while due to reverse biasing of SCR, $p_2n_1p_1n_4$ forms a main SCR. The gate current initiates the conduction and due to regenerative action, the triac is turned ON.

In this mode, direction of main SCR i.e. triac current reverses compared to mode I and II and polarities of voltage between MT_1 and MT_2 are also reversed compared to mode I and II hence triac operates in third quandrant of its V-I characteristics. But due to positive gate, it is called III^+ mode.

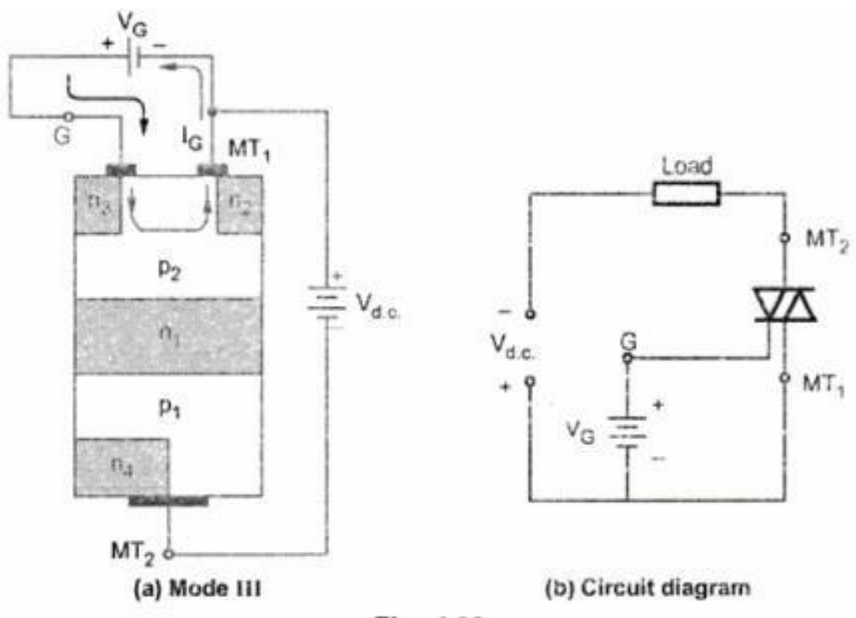


Fig. 4.38

4. Mode IV : In this mode, triac is reverse biased but gate is made negative as shown in the Fig. 4.39 (a) and (b).

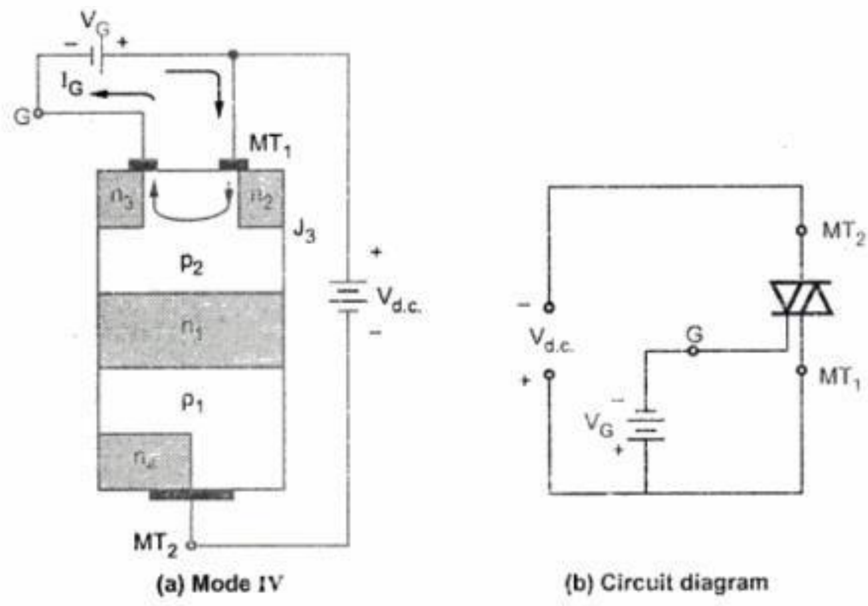


Fig. 4.39

In this mode, gate current is negative and p_2n_3 junction is forward biased. This injects the carriers to initiate the conduction of main SCR formed as $p_2n_1p_1n_4$. Due to regenerative action, the triac starts conducting.

Compared to III^+ mode, in this mode only gate current direction is reversed. Hence this mode is called III^- mode. The triac operation is in the third quadrant of its V-I characteristics. In this mode triac is more sensitive than III^+ mode.

VI Charactersitics of TRIAC

The triac has its characteristics in first quadrant and third quadrant. The characteristics are exactly similar to that of SCR, but in both the quadrants I and III and not like SCR only in first quadrant. The mode I and II operations exist in first quadrant while mode III and IV operations exist in the third quadrant. The entire V-I characteristics of triac are shown in the Fig. 4.40.

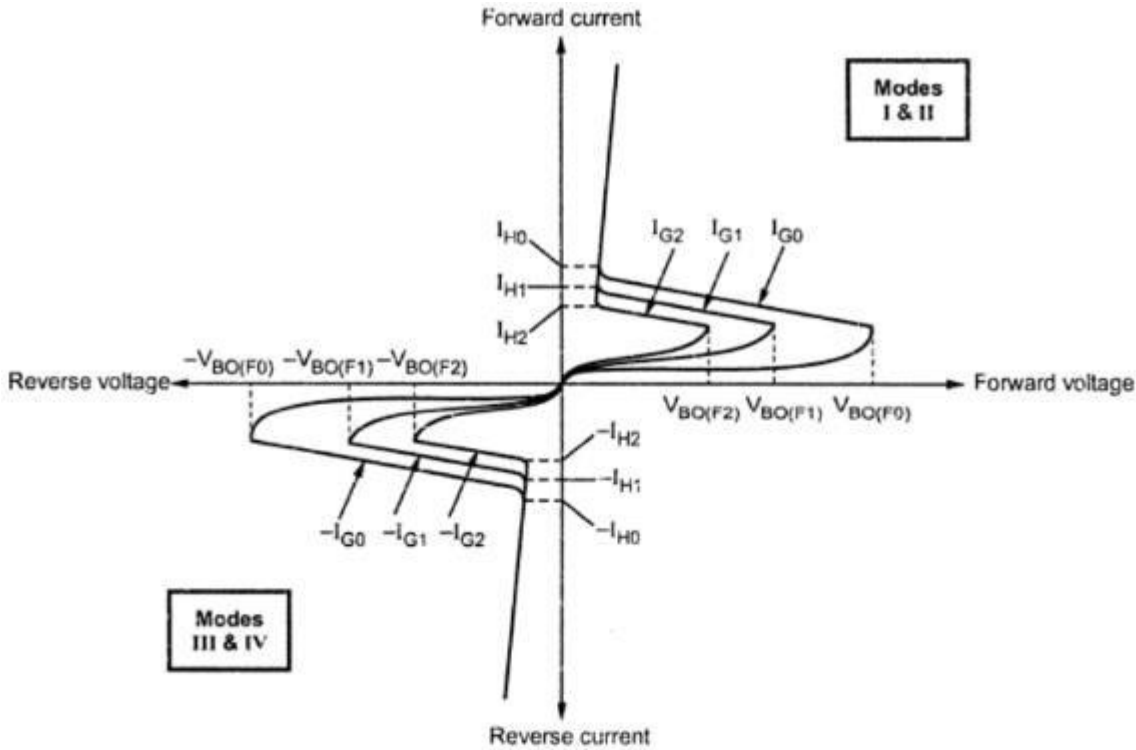


Fig. 4.40 V-I Characteristics of triac

4.6.5 Merits of Triac

1. It conducts in both the directions.
2. Triac turns off when voltage is reversed.
3. Single gate controls the conduction in both the directions.
4. Triacs with high voltage and current ratings are available.

4.6.6 Demerits of Triac

1. Not suitable for d.c. power applications.
2. Gate has no control over the conduction when triac is on.
3. Triacs have very small switching frequencies.

12. Draw the circuit diagram of half wave rectifier and full wave rectifier and explain its operation with necessary waveform. Also derive the expression for rectification efficiency and TUF.

Rectifiers

A rectifier is a device which converts a.c. voltage to pulsating d.c. voltage, using one or more p-n junction diode.

Using one or more diodes following rectifier circuits can be designed.

1. Half wave rectifier
2. Full wave rectifier
3. Bridge rectifier

Let us discuss the various rectifier circuits in detail.

3.3 Half Wave Rectifier

In half wave rectifier, rectifying element conducts only during positive half cycle of input a.c. supply. The negative half cycles of a.c. supply are eliminated from the output.

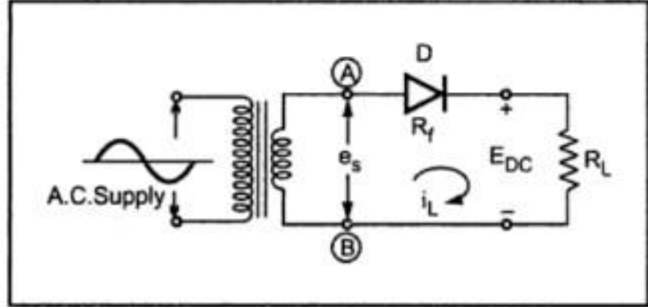


Fig. 3.2 Halfwave rectifier

This rectifier circuit consists of resistive load, rectifying element, i.e. p-n junction diode, and the source of a.c. voltage, all connected in series. The circuit diagram is shown in Fig. 3.2. Usually, the rectifier circuits are operated from ac mains supply. To obtain the desired d.c.voltage across the load, the a.c. voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turns ratio.

The input voltage to the half-wave rectifier circuit shown in Fig. 3.2 is a sinusoidal a.c. voltage, having a frequency which is the supply frequency, 50 Hz.

The transformer decides the peak value of the secondary voltage. If the N_1 are primary number of turns and N_2 are secondary number of turns and E_{pm} is the peak value of the primary voltage then,

$$\frac{N_2}{N_1} = \frac{E_{sm}}{E_{pm}}$$

where E_{sm} is the peak value of the secondary a.c. voltage.

As the nature of E_{sm} is sinusoidal the instantaneous value will be,

$$e_s = E_{sm} \sin \omega t$$
$$\omega = 2\pi f$$
$$f = \text{supply frequency}$$

Let R_f represents the forward resistance of the diode. Assume that, under reverse biased condition, the diode acts almost as open circuit, conducting no current.

3.3.1 Operation of the Circuit

During the positive half cycle of secondary a.c voltage, terminal (A) becomes positive with respect to terminal (B). The diode is forward biased and the current flows in the circuit in the clockwise direction, as shown in Fig. 3.2. The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L hence denoted as i_L, the load current.

During negative half cycle when terminal (A) is negative with respect to terminal (B), diode becomes reverse biased. Hence no current flows in the circuit. Thus the circuit current, which is also the load current, is in the form of half sinusoidal pulses.

The load voltage, being the product of load current and load resistance, will also be in the form of half sinusoidal pulses. The different waveforms are illustrated in Fig. 3.3.

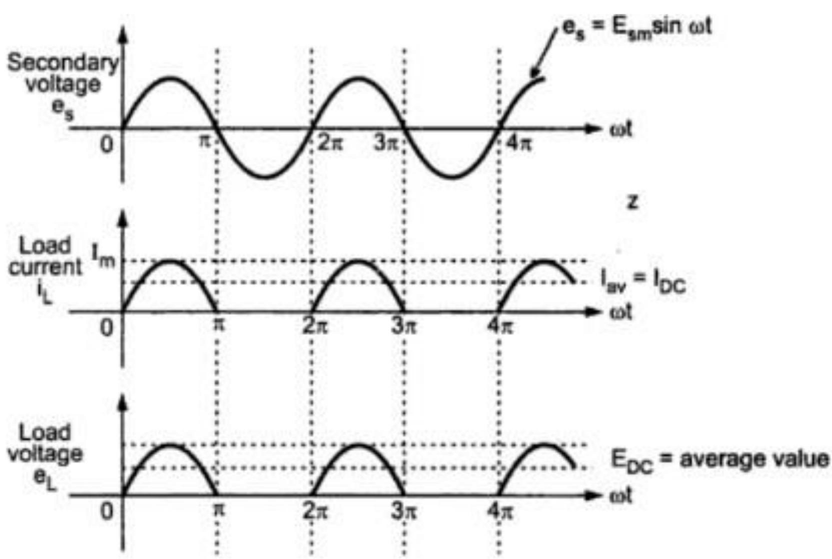


Fig. 3.3 Load current and load voltage waveforms for halfwave rectifier

The d.c. output waveform is expected to be a straight line but the half wave rectifier **gives** output in the form of positive sinusoidal pulses. Hence the output is called **pulsating d.c.** It is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of output voltage.

3.3.2 Average DC Load Current (I_{DC})

The average or dc value of alternating current is obtained by integration.

For finding out the average value of an alternating waveform, we have to determine the area under the curve over one complete cycle i.e. from 0 to 2π and then dividing it by the base i.e. 2π.

Mathematically, current waveform can be described as,

$$i_L = I_m \sin \omega t \qquad \text{for } 0 \le \omega t \le \pi$$

$$i_L = 0 \qquad \text{for } \pi \le \omega t \le 2\pi$$

where I_m = peak value of load current

$$\therefore \quad I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t) = \frac{1}{2\pi}\int_0^{2\pi} I_m \sin(\omega t)\, d(\omega t)$$

As no current flows during negative half cycle of ac input voltage, i.e. between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore \qquad I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin(\omega t)\, d(\omega t)$$

$$= \frac{I_m}{2\pi}\left[-\cos(\omega t)\right]_0^{\pi} = -\frac{I_m}{2\pi}\left[\cos(\pi) - \cos(0)\right]$$

$$= -\frac{I_m}{2\pi}[-1-1] = \frac{I_m}{\pi}$$

$$\therefore \qquad I_{DC} = \frac{I_m}{\pi} = \text{average value}$$

Applying Kirchhoff's voltage law we can write,

$$I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

where R_s = resistance of secondary winding of transformer. If R_s is not given it should be neglected while calculating I_m.

3.3.3 Average DC Load Voltage (E_{DC})

It is the product of average D.C. load current and the load resistance R_L.

$$E_{DC} = I_{DC} R_L$$

Substituting value of I_{DC},

$$E_{DC} = \frac{I_m}{\pi} R_L = \frac{E_{sm}}{(R_f + R_L + R_s)\,\pi} R_L$$

The winding resistance R_s and forward diode resistance R_f are practically very small compared to R_L.

$$\therefore \qquad E_{DC} = \frac{E_{sm}}{\pi\left[\dfrac{R_f + R_s}{R_L} + 1\right]}$$

But as R_f and R_s are small compared to R_L, $(R_f + R_s)/R_L$ is negligibly small compared to 1. So neglecting it we get,

$$\therefore \qquad E_{DC} \approx \frac{E_{sm}}{\pi}$$

3.3.4 R.M.S. Value of Load Current (I_{RMS})

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S. value of load current can be obtained as,

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{\pi}(I_m \sin\omega t)^2 \, d(\omega t)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(I_m{}^2 \sin^2 \omega t \, d(\omega t)\right)}$$

$$= I_m\sqrt{\frac{1}{2\pi}\int_0^{\pi}\frac{[1-\cos(2\omega t)]d(\omega t)}{2}}$$

$$= I_m\sqrt{\frac{1}{2\pi}\left\{\frac{\omega t}{2}-\frac{\sin(2\omega t)}{4}\right\}_0^{\pi}}$$

$$= I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2}\right)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$= \frac{I_m}{2}$$

$$\therefore \quad I_{RMS} = \frac{I_m}{2}$$

Note : Students must remember that this R.M.S. value is for **half wave** rectified waveform hence it is $I_m/2$. For full sine wave it is $I_m/\sqrt{2}$.

3.3.5 D.C. Power Output (P_{DC})

The d.c. power output can be obtained as,

$$P_{DC} = E_{DC} I_{DC} = I_{DC}^2 R_L$$

$$\text{D.C. Power output} = I_{DC}^2 R_L = \left[\frac{I_m}{\pi}\right]^2 R_L = \frac{I_m{}^2}{\pi^2} R_L$$

$$\therefore \quad P_{DC} = \frac{I_m{}^2}{\pi^2} R_L$$

$$\text{where} \quad I_m = \frac{E_{sm}}{R_f + R_L + R_s}$$

$$\therefore \quad P_{DC} = \frac{E_{sm}{}^2 R_L}{\pi^2 [R_f + R_L + R_s]^2}$$

3.3.6 A.C. Power Input (P_{AC})

The power input taken from the secondary of transformer is the power supplied to three resistances namely load resistance R_L , the diode resistance R_f and winding resistance R_s. The a.c. power is given by,

$$P_{AC} = I_{RMS}^2[R_L + R_f + R_s]$$

but $$I_{RMS} = \frac{I_m}{2} \quad \text{for half wave,}$$

$$\therefore \quad P_{AC} = \frac{I_m^2}{4}[R_L + R_f + R_s]$$

3.3.7 Rectifier Efficiency (η)

The rectifier efficiency is defined as the ratio of output d.c. power to input a.c. power.

$$\therefore \quad \eta = \frac{\text{D.C. output power}}{\text{A.C. input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\therefore \quad \eta = \frac{\frac{I_m^2}{\pi^2} R_L}{\frac{I_m^2}{4}[R_f + R_L + R_s]} = \frac{(4/\pi^2)R_L}{(R_f + R_L + R_s)}$$

$$\therefore \quad \eta = \frac{0.406}{1 + \left(\frac{R_f + R_s}{R_L}\right)}$$

If $(R_f + R_s) << R_L$ as mentioned earlier, we get the maximum theoretical efficiency of half wave rectifier as,

$$\%\eta_{max} = 0.406 \times 100 = 40.6\ \%$$

Thus in half wave rectifier, maximum 40.6% a.c. power gets converted to d.c. power in the load. If the efficiency of rectifier is 40% then what happens to the remaining 60% power. It is present interms of ripples in the output which is fluctuating component present in the output. Thus more the rectifier efficiency, less are the ripple contents in the output.

3.3.8 Ripple Factor (γ)

It is seen that the output of half wave rectifier is not pure d.c. but a pulsating d.c. The output contain pulsating components called **ripples**. Ideally there should not be any ripples in the rectifier output. The measure of such ripples present in the output is with the help of a factor called **ripple factor** denoted by γ. It tells how smooth is the output. Smaller the ripple factor closer is the output to a pure d.c. The ripple factor expresses how much successful the circuit is in obtaining pure d.c. from a.c. input.

Mathematically ripple factor is defined as the ratio of R.M.S. value of the a.c. component to the average or d.c.component.

$$\text{Ripple factor} \quad \gamma = \frac{\text{R.M.S. value of a.c. component}}{\text{Average or d.c. component}}$$

Now the output current is composed of a.c. component as well as d.c. component.

Let I_{ac} = r.m.s. value of a. c. component present in output

I_{DC} = d.c. component present in output

I_{RMS} = R.M.S. value of total output current

$$\therefore \quad I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$\therefore \quad I_{ac} = \sqrt{I_{RMS}^2 - I_{DC}^2}$$

Now Ripple factor $= \dfrac{I_{ac}}{I_{DC}}$ as per definition

$$\therefore \quad \gamma = \frac{\sqrt{I_{RMS}^2 - I_{DC}^2}}{I_{DC}}$$

$$\therefore \quad \gamma = \sqrt{\left(\frac{I_{RMS}}{I_{DC}}\right)^2 - 1}$$

This is the general expression for ripple factor and can be used for any rectifier circuit.

Now for a half wave circuit,

$$I_{RMS} = \frac{I_m}{2} \quad \text{while} \quad I_{DC} = \frac{I_m}{\pi}$$

$$\therefore \quad \gamma = \sqrt{\left[\frac{\left(\frac{I_m}{2}\right)}{\left(\frac{I_m}{\pi}\right)}\right]^2 - 1} = \sqrt{\frac{\pi^2}{4} - 1} = \sqrt{1.4674}$$

$$\therefore \quad \gamma = 1.211$$

This indicates that the ripple contents in the output are 1.211 times the d.c. component i.e. 121.1 % of d.c. component. The ripple factor for half wave is very high which indicates that the half wave circuit is a poor converter of a.c. to d.c. The ripple factor is minimised using filter circuits along with rectifiers.

3.3.11 Transformer Utilization Factor (T.U.F.)

The factor which indicates how much is the utilization of the transformer in the circuit is called Transformer Utilization Factor (T.U.F.)

The T.U.F. is defined as the ratio of d.c. power delivered to the load to the a.c power rating of the transformer. While calculating the a.c. power rating, it is necessary to consider r.m.s. value of a.c. voltage and current.

The T.U.F. for half wave rectifier can be obtained as,

$$\text{A.C. power rating of transformer} = E_{RMS}\, I_{RMS}$$

$$= \frac{E_{sm}}{\sqrt{2}} \cdot \frac{I_m}{2} = \frac{E_{sm}\, I_m}{2\sqrt{2}}$$

Remember that the secondary voltage is purely sinusoidal hence its r.m.s. value is $1/\sqrt{2}$ times maximum while the current is half sinusoidal hence its r.m.s. value is $1/2$ of the maximum, as derived earlier.

$$\text{D.C. power delivered to the load} = I_{DC}^2\, R_L$$

$$= \left(\frac{I_m}{\pi}\right)^2 R_L$$

$$\therefore \quad \text{T.U.F.} = \frac{\text{D.C. Power delivered to the load}}{\text{A.C. Power rating of the transformer}}$$

$$= \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{E_{sm} I_m}{2\sqrt{2}}\right)}$$

Neglecting the drop across R_f and R_s we can write,

$$E_{sm} = I_m R_L$$

$$\therefore \quad \text{T.U.F} = \frac{I_m{}^2}{\pi^2} \cdot \frac{R_L . 2\sqrt{2}}{I_m{}^2 R_L}$$

$$= \frac{2\sqrt{2}}{\pi^2}$$

$$= 0.287$$

The value of T.U.F. is low which shows that in half wave circuit, the transformer is not fully utilized.

3.3.12 Disadvantages of Half Wave Rectifier Circuit

1. The ripple factor of half wave rectifier circuit is 1.21, which is quite high. The output contains lot of varying components.
2. The maximum theoretical rectification efficiency is found to be 40%. The practical value will be less than this. This indicates that half wave rectifier circuit is quite inefficient.
3. The circuit has low transformer utilization factor, showing that the transformer is not fully utilized.
4. The dc current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of the transformer. To minimize the saturation, transformer size have to be increased accordingly. This increases the cost.

Because of all these disadvantages, the half-wave rectifier circuit is normally not used as a power rectifier circuit.

3.4 Full Wave Rectifier

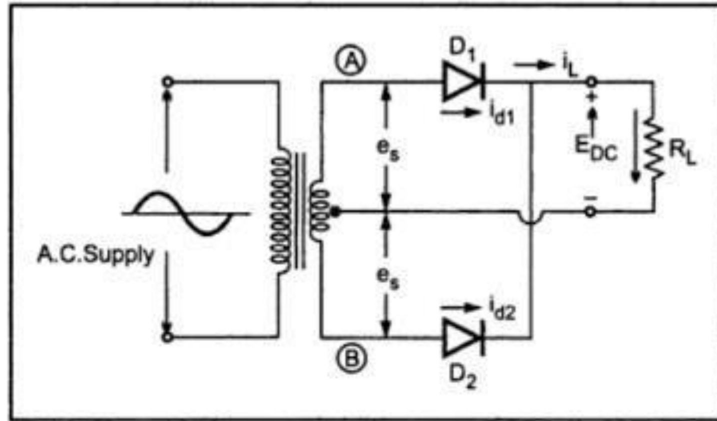


Fig. 3.6 Full wave rectifier

The full wave rectifier conducts during both positive and negative half cycles of input a.c. supply. In order to rectify both the half cycles of a.c. input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a center tap transformer. The a.c. voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is shown in the Fig.3.6.

For the proper operation of the circuit, a center-tap on the secondary winding of the transformer is essential.

3.4.1 Operation of the Circuit

Consider the positive half cycle of ac input voltage in which terminal (A) is positive and terminal (B) negative. The diode D_1 will be forward biased and hence will conduct; while diode D_2 will be reverse biased and will act as open circuit and will not conduct. This is illustrated in Fig.3.7.

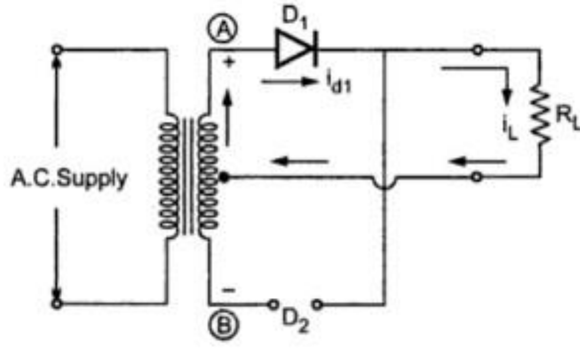


Fig. 3.7 Current flow during positive half cycle

The diode D_1 supplies the load current, i.e. $i_L = i_{d1}$ .This current is flowing through upper half of secondary winding while the lower half of secondary winding of the transformer carries no current since diode D_2 is reverse biased and acts as open circuit.

In the next half cycle of ac voltage, polarity reverses and terminal (A) becomes negative and (B) positive. The diode D_2 conducts, being forward biased, while D_1 does not, being reverse biased. This is shown in Fig. 3.8.

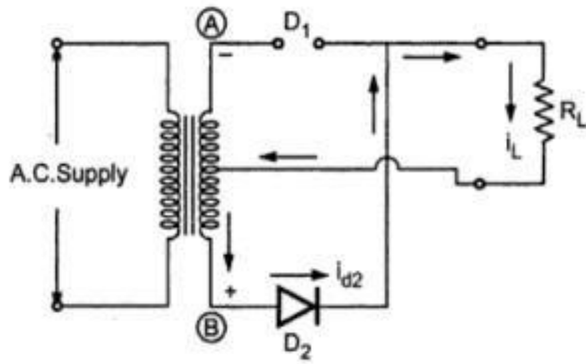


Fig. 3.8 Current flow during negative half cycle

The diode D_2 supplies the load current, i.e. $i_L = i_{d2}$. Now the lower half of the secondary winding carries the current but the upper half does not.

It is noted that the **load current flows in both half cycles of ac voltage and in the same direction through the load resistance**. Hence we get rectified output across the load. The load current is sum of individual diode currents flowing in corresponding half cycles. It is also noted that the two diodes do not conduct simultaneously but in alternate half cycles.The individual diode currents and the load current are shown in Fig. 3.9

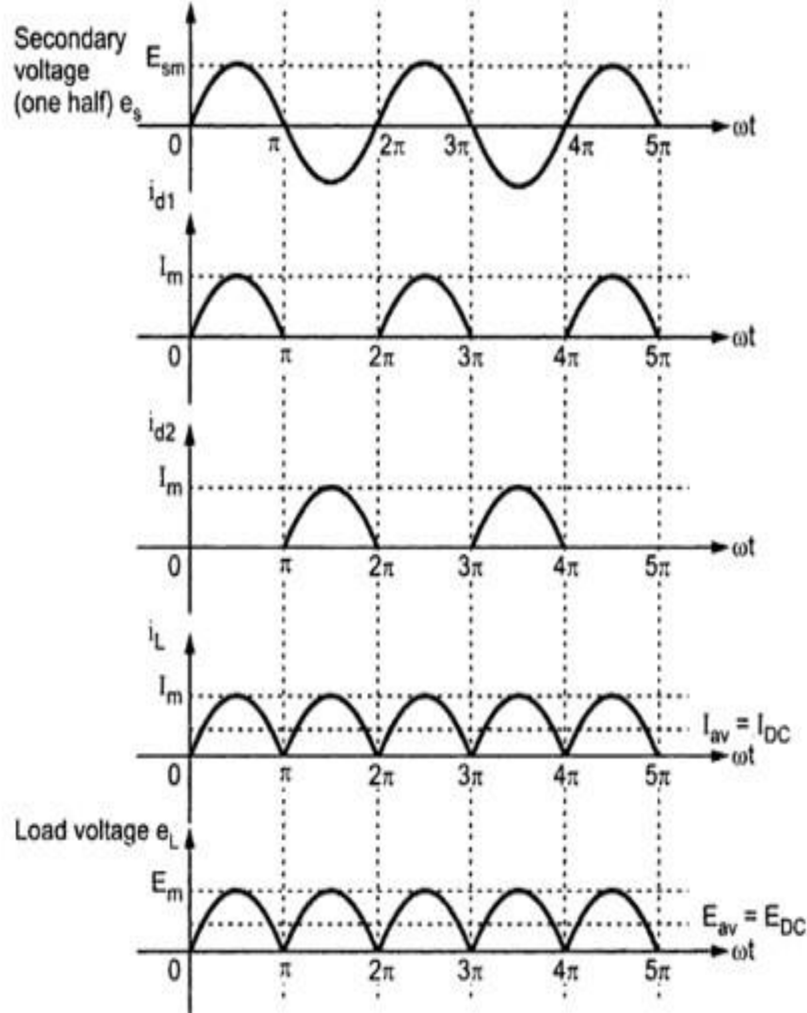


Fig. 3.9 Load current and voltage waveforms full wave rectifier

Thus the full wave rectifier circuit essentially consists of two half-wave rectifier circuits working independently (working in alternate half cycles of a c) of each other but feeding a common load. The output load current is still pulsating d.c. and not pure d.c.

3.4.2 Maximum Load Current

Let R_f = forward resistance of diodes

R_s = winding resistance of each half of secondary

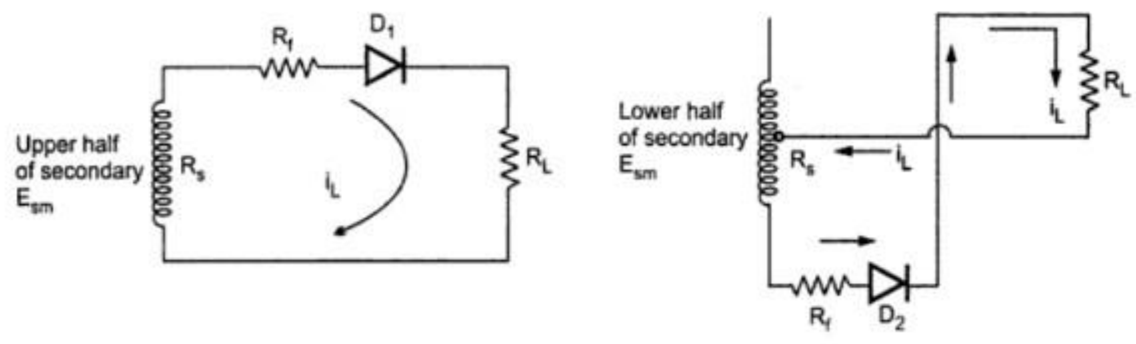
R_L = load resistance

e_s = instantaneous a.c. voltage across each half of secondary

$\therefore$ $e_s = E_{sm} \sin \omega t$

$\omega = 2\pi f$

E_{sm} = maximum value of a.c. input voltage across each half of secondary winding



(a) Fig. 3.10 (b)

$$\therefore \quad I_m = \frac{E_{sm}}{R_s + R_f + R_L}$$

where I_m = maximum value of load current i_L

3.4.3 Average DC Load Current (I_{DC})

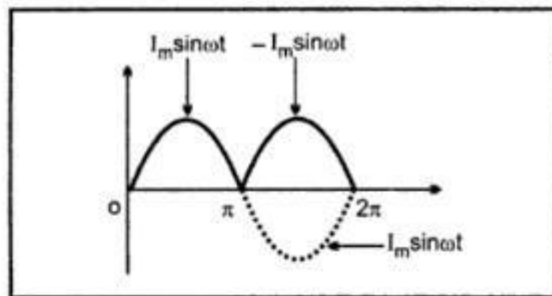


Fig. 3.11

Consider one cycle of load current i_L from 0 to 2π to obtain the average value which is d.c. value of load current.

$$i_L = I_m \sin \omega t \quad 0 \le \omega t \le \pi$$

But for π to 2π, the current i_L is again positive while sin ωt term is negative during π to 2π. Hence in the region π to 2π the positive i_L can be represented as negative of $I_m \sin(\omega t)$.

$$\therefore \quad i_L = -I_m \sin \omega t \qquad \pi \le \omega t \le 2\pi$$

$$\therefore \quad I_{av} = I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi}\left[\int_0^{\pi} I_m \sin\omega t \, d(\omega t) + \int_{\pi}^{2\pi} -I_m \sin\omega t \, d(\omega t)\right]$$

$$= \frac{I_m}{2\pi}\left[\int_0^{\pi} \sin\omega t \, d(\omega t) - \int_{\pi}^{2\pi} \sin\omega t \, d(\omega t)\right]$$

$$= \frac{I_m}{2\pi}\left[(-\cos\omega t)_0^{\pi} - (-\cos\omega t)_{\pi}^{2\pi}\right]$$

$$= \frac{I_m}{2\pi}\left[-\cos\pi + \cos 0 + \cos 2\pi - \cos\pi\right]$$

but $\cos\pi = -1$

$$= \frac{I_m}{2\pi}\left[-(-1) + 1 + 1 - (-1)\right] = \frac{4I_m}{2\pi}$$

$$\therefore \quad I_{DC} = \frac{2I_m}{\pi} \quad \text{for full wave rectifier}$$

For half wave it is I_m/π and full wave rectifier is the combination of two half wave circuits acting alternately in two half cycles of input. Hence obviously the d.c. value for full wave circuit is $2\,I_m/\pi$

3.4.4 Average DC Load Voltage (E_{DC})

The d.c. load voltage is,

$$E_{DC} = I_{DC} R_L = \frac{2I_m R_L}{\pi}$$

Substituting value of I_m,

$$E_{DC} = \frac{2\,E_{sm}\,R_L}{\pi\left[R_f + R_s + R_L\right]}$$

$$= \frac{2\,E_{sm}}{\pi\left[1 + \frac{R_f + R_s}{R_L}\right]}$$

But as R_f and $R_s << R_L$ hence $\frac{R_f + R_s}{R_L} << 1$

$$\therefore \qquad E_{DC} = \frac{2E_{sm}}{\pi}$$

3.4.5 RMS Load Current (I_{RMS})

The R.M.S. value of current, I_{RMS}, is obtained as follows :

$$I_{RMS} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 d(\omega t)}$$

Since two half wave rectifier are similar in operation we can write,

$$I_{RMS} = \sqrt{\frac{2}{2\pi}\int_0^{\pi} [I_m \sin\omega t]^2 d(\omega t)}$$

$$= I_m\sqrt{\frac{1}{\pi}\int_0^{\pi}\left[\frac{1-\cos 2\omega t}{2}\right]d(\omega t)} \text{ as } \sin^2\omega t$$

$$= \frac{1-\cos 2\omega t}{2}$$

$$\therefore \qquad I_{RMS} = I_m\sqrt{\frac{1}{2\pi}\left[[\omega t]_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

$$= I_m\sqrt{\frac{1}{2\pi}[\pi - 0]}$$

$$= I_m\sqrt{\frac{1}{2\pi}(\pi)} \qquad \text{as } \sin(2\pi) = \sin(0) = 0$$

$$\therefore \qquad I_{RMS} = \frac{I_m}{\sqrt{2}}$$

3.4.6 DC Power Output (P_{DC})

$$\text{D.C. Power output} = E_{DC}I_{DC} = I_{DC}^2 R_L$$

$$\therefore \qquad P_{DC} = I_{DC}^2 R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$\therefore \qquad P_{DC} = \frac{4}{\pi^2} I_m^2 R_L$$

Substituting value of I_m we get,

$$P_{DC} = \frac{4}{\pi^2}\frac{E_{sm}^2}{(R_s + R_f + R_L)^2} \times R_L$$

3.4.7 AC Power Input (P_{AC})

The a.c. power input is given by,

$$P_{AC} = I_{RMS}^2 (R_f + R_s + R_L)$$

$$= \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$\therefore \quad P_{AC} = \frac{I_m^2 (R_f + R_s + R_L)}{2}$$

Substituting value of I_m we get,

$$\therefore \quad P_{AC} = \frac{E_{sm}^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L)$$

$$\therefore \quad P_{AC} = \frac{E_{sm}^2}{2(R_f + R_s + R_L)}$$

3.4.8 Rectifier Efficiency (η)

$$\eta = \frac{P_{DC} \text{ output}}{P_{AC} \text{ input}}$$

$$\therefore \quad \eta = \frac{\frac{4}{\pi^2} I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}}$$

$$\therefore \quad \eta = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

But if $R_f + R_s << R_L$, neglecting it from denominator

$$\eta = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2}$$

$$\therefore \quad \% \eta_{max} = \frac{8}{\pi^2} \times 100 = 81.2 \%$$

This is the maximum theoretical efficiency of full wave rectifier.

3.4.9 Ripple Factor (γ)

As derived earlier in case of half wave rectifier the ripple factor is given by a general expression,

$$\text{Ripple factor} = \sqrt{\left[\frac{I_{RMS}}{I_{DC}}\right]^2 - 1}$$

For full wave $\quad I_{RMS} = I_m/\sqrt{2}$ and $I_{DC} = 2I_m/\pi$ so,

substituting in the above equation.

$$\text{Ripple factor} = \sqrt{\left[\frac{I_m/\sqrt{2}}{2I_m/\pi}\right]^2 - 1}$$

$$= \sqrt{\frac{\pi^2}{8} - 1}$$

$$\therefore \quad \text{Ripple factor} = \gamma = 0.48$$

This indicates that the ripple contents in the output are 48 % of the d.c. component which is much less than that for half wave circuit.

3.4.12 Transformer Utilization Factor (T.U.F.)

In full wave rectifier, the secondary current flows through each half separately in every half cycle. While the primary of transformer carries current continuously. Hence T.U.F is calculated for primary and secondary windings separately and then the average T.U.F. is determined.

$$\text{Secondary T.U.F} = \frac{\text{DC power to load}}{\text{AC power rating of secondary}}$$

$$= \frac{I_{DC}^2 R_L}{E_{RMS}\, I_{rms}} = \frac{\left(\frac{2}{\pi} I_m\right)^2 R_L}{\frac{E_{sm}}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

Neglecting forward resistance R_f of diode, $E_{sm} \approx I_m R_L$.

$$\therefore \quad \text{Secondary T.U.F.} = \frac{\frac{4}{\pi^2} \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2}$$

$$= 0.812$$

The primary of the transformer is feeding two half-wave rectifiers separately. These two half-wave rectifiers work independently of each other but feed a common load. We have already derived the T.U.F. for half wave circuit to be equal to 0.287. Hence

$$\text{T.U.F. for primary winding} = 2 \times \text{T.U.F. of half wave circuit}$$

$$= 2 \times 0.287$$

$$= 0.574.$$

The average T.U.F for fullwave circuit will be

$$\text{Average T.U.F. for full wave rectifier circuit} = \frac{\text{T.U.F of primary} + \text{T.U.F of secondary}}{2}$$

$$= \frac{0.574 + 0.812}{2}$$

$$= 0.693$$

∴ Average T.U.F. for full-wave rectifier = 0.693

Thus in full-wave circuit transformer gets utilized more than the half wave rectifier circuit.

3.5 Bridge Rectifier

The bridge rectifier circuits are mainly used as,

a) a power rectifier circuit for converting ac power to dc power, and

b) a rectifying system in rectifier type ac meters, such as ac voltmeter, in which the ac voltage under measurement is first converted into dc and measured with conventional meter. In this system, the rectifying elements are either copper oxide type or selenium type.

The basic bridge rectifier circuit is shown in Fig. 3.13.

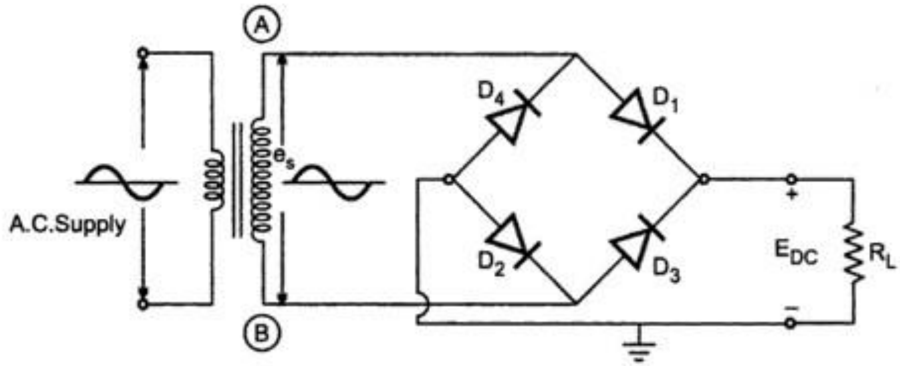


Fig. 3.13 Bridge rectifier circuit

The bridge rectifier circuit is essentially a full-wave rectifier circuit, using four diodes, forming the four arms of an electrical bridge. To one diagonal of the bridge, the ac voltage is applied through a transformer if necessary, and the rectified dc voltage is taken from the other diagonal of the bridge. The main advantage of this circuit is that it does not require a center tap on the secondary winding of the transformer. Hence wherever possible, ac voltage can be directly applied to the bridge.

3.5.1 Operation of the Circuit

Consider the positive half of ac input voltage. The point A of secondary becomes positive. The diodes D_1 and D_2 will be forward biased, while D_3 and D_4 reverse biased. The two diodes D_1 and D_2 conduct in series with the load and the current flows as shown in Fig. 3.14.

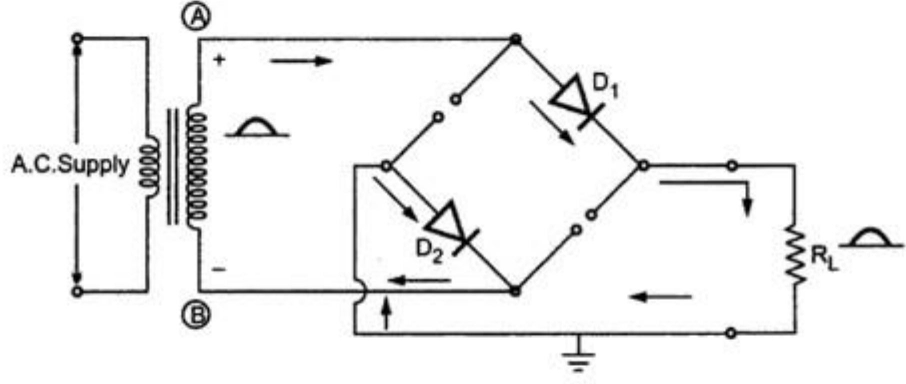


Fig. 3.14 Current flow during positive half cycle

In the next half cycle, when the polarity of ac voltage reverses hence point B becomes positive diodes D_3 and D_4 are forward biased, while D_1 and D_2 reverse biased. Now the diodes D_3 and D_4 conduct is series with the load and the current flows as shown in Fig. 3.14.

It is seen that in both cycles of ac, the load current is flowing in the same direction hence, we get a full-wave rectified output.

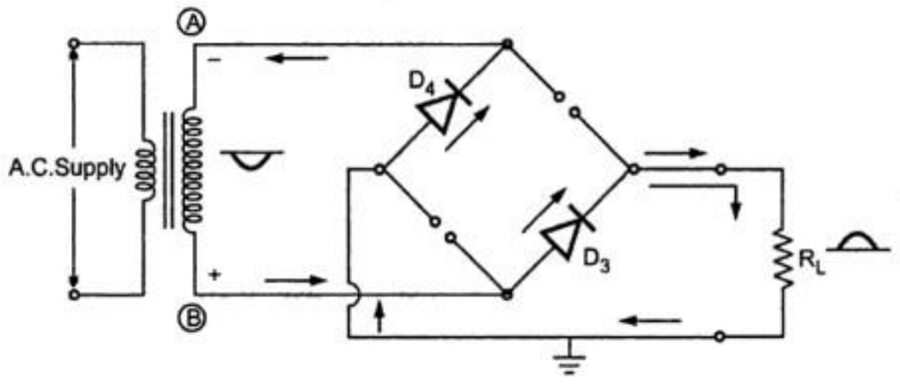


Fig. 3.15 Current flow during negative half cycle

3.5.2 Expressions for Various Parameters

The bridge rectifier circuit, being basically a full-wave rectifier circuit; all the characteristic discussed previously for a full-wave circuit using two diodes, are the characteristic of a bridge rectifier circuit.

The relation between I_m the maximum value of load current and I_{DC} , I_{RMS} remains same as derived earlier for the full wave rectifier circuit.

$$I_{DC} = \frac{2I_m}{\pi} \text{ and } I_{RMS} = \frac{I_m}{\sqrt{2}}$$

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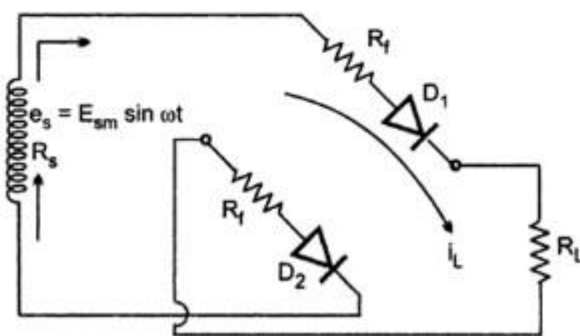
The relation between I_m the maximum value of load current and I_{DC}, I_{RMS} remains same as derived earlier for the full wave rectifier circuit.

$$I_{DC} = \frac{2I_m}{\pi} \text{ and } I_{RMS} = \frac{I_m}{\sqrt{2}}$$

The expression for I_m will change slightly. This will be clear from the equivalent circuit shown in the Fig. 3.16.



In each half cycle two diodes conduct simultaneously. Hence maximum value of load current is,

$$I_m = \frac{E_{sm}}{R_s + 2R_f + R_L}$$

So the only modification is that instead of R_f, which is forward resistance of each diode, the term 2 R_f appears in the denominator.

The remaining expressions are identical to those derived for two diode full wave rectifier and reproduced for the convenience of the reader.

$$E_{DC} = I_{DC} R_L = \frac{2E_{sm}}{\pi}$$

$$P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 R_L$$

$$P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L)$$

$$= \frac{I_m^2 (2R_f + R_s + R_L)}{2}$$

$$\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}$$

$$\%\eta_{max} = 81.2\%$$

$$\gamma = 0.48$$

3.5.3 Advantages of Bridge Rectifier Circuit

1) The current in both the primary and secondary of the power transformer flows for the entire cycle and hence for a given power output, power transformer of a small size and less cost may be used.

2) No center tap is required in the transformer secondary. Hence, wherever possible, ac voltage can directly be applied to the bridge.

3) The current in the secondary of the transformer is in opposite direction in two half cycles. Hence net d.c. component flowing is zero which reduces the losses and danger of saturation.

4) Due to pure alternating current in secondary of transformer, the transformer gets utilised effectively and hence the circuit is suitable for applications where large powers are required.

5) As two diodes conduct in series in each half cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

3.5.4 Disadvantages of Bridge Rectifier

The only disadvantage of bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term $2R_f$ present in expression of I_m instead of R_f. This reduces the output voltage.

13. With circuit explain working of different types of filter circuits.

3.7 Filter Circuits

It is seen that the output a half-wave or full-wave rectifier circuit is not pure d.c.; but it contains fluctuations or ripple, which is undesired . To minimize the ripple in the output, filter circuits are used. These circuits are connected between the rectifier and load, as shown in Fig. 3.18.

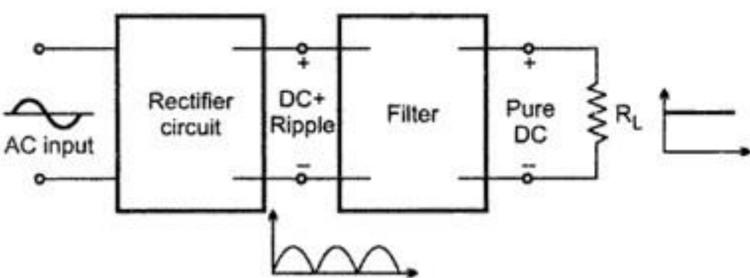


Fig. 3.18 Power supply using rectifier and filter

An ac input is applied to the rectifier. At the output of the rectifier, there will be DC and ripple voltage present, which is the input to the filter. Ideally the output of the filter should be pure DC. Practically, the filter circuit will try to minimize the ripple at the output, as far as possible.

6.21 Types of Filter Circuits

The most commonly used filter circuits are *capacitor filter*, *choke input filter* and *capacitor input filter or π-filter*. We shall discuss these filters in turn.

(i) Capacitor filter. Fig. 6.41 (*ii*) shows a typical capacitor filter circuit. It consists of a capacitor C placed across the rectifier output in parallel with load R_L. The pulsating direct voltage of the rectifier is applied across the capacitor. As the rectifier voltage increases, it charges the capacitor and also supplies current to the load. At the end of quarter cycle [Point A in Fig. 6.41 (*iii*)], the

* If such a d.c. is applied in an electronic circuit, it will produce a *hum*.

** A capacitor offers infinite reactance to d.c. For d.c., $f = 0$.

$$\therefore \qquad X_C = \frac{1}{2\pi fC} = \frac{1}{2\pi \times 0 \times C} = \infty$$

Hence, a capacitor does not allow d.c. to pass through it.

† We know $X_L = 2\pi fL$. For d.c., $f = 0$ and, therefore, $X_L = 0$. Hence inductor passes d.c. quite readily. For a.c., it offers opposition and drops a part of it.

capacitor is charged to the peak value V_m of the rectifier voltage. Now, the rectifier voltage starts to decrease. As this occurs, the capacitor discharges through the load and voltage across it (*i.e.* across parallel combination of R-C) decreases as shown by the line AB in Fig. 6.41 (*iii*). The voltage across load will decrease only slightly because immediately the next voltage peak comes and recharges the capacitor. This process is repeated again and again and the output voltage waveform becomes $ABCDEFG$. It may be seen that very little ripple is left in the output. Moreover, output voltage is higher as it remains substantially near the peak value of rectifier output voltage.

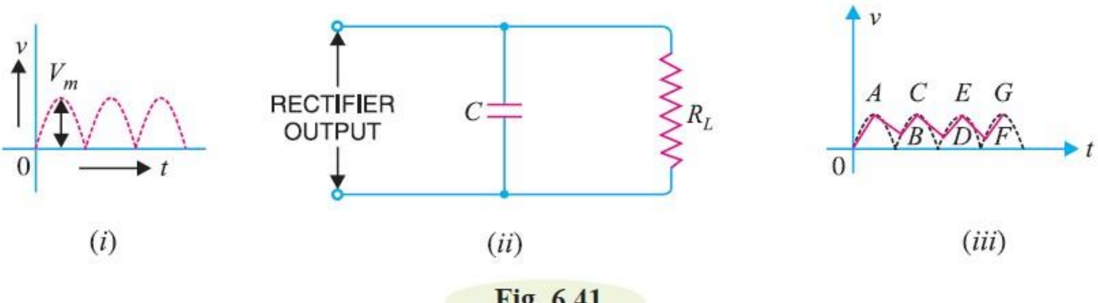


Fig. 6.41

The capacitor filter circuit is extremely popular because of its low cost, small size, little weight and good characteristics. For small load currents (say upto 50 mA), this type of filter is preferred. It is commonly used in transistor radio battery eliminators.

(ii) **Choke input filter.** Fig. 6.42 shows a typical choke input filter circuit. It consists of a *choke L connected in series with the rectifier output and a filter capacitor C across the load. Only a single filter section is shown, but several identical sections are often used to reduce the pulsations as effectively as possible.

The pulsating output of the rectifier is applied across terminals 1 and 2 of the filter circuit. As discussed before, the pulsating output of rectifier contains a.c. and d.c. components. The choke offers high opposition to the passage of a.c. component but negligible opposition to the d.c. component. The result is that most of the a.c. component appears across the choke while whole of d.c. component passes through the choke on its way to load. This results in the reduced pulsations at terminal 3.

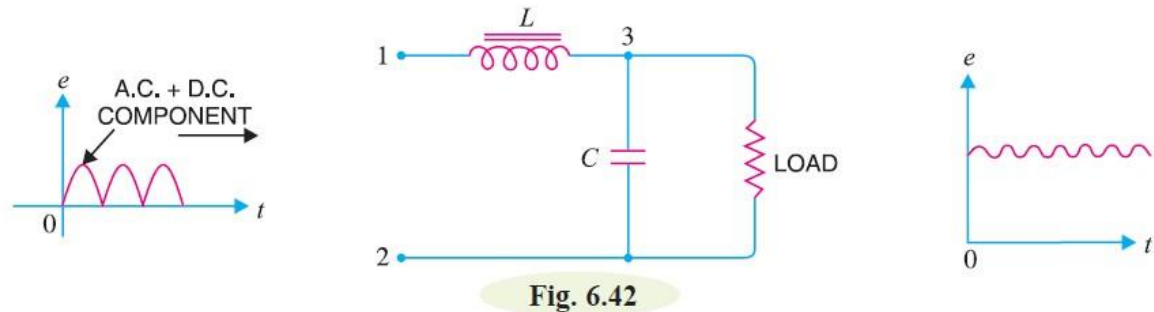


Fig. 6.42

At terminal 3, the rectifier output contains d.c. component and the remaining part of a.c. component which has managed to pass through the choke. Now, the low reactance of filter capacitor bypasses the a.c. component but prevents the d.c. component to flow through it. Therefore, only d.c. component reaches the load. In this way, the filter circuit has filtered out the a.c. component from the rectifier output, allowing d.c. component to reach the load.

(iii) **Capacitor input filter** *or* **π-filter.** Fig. 6.43 shows a typical capacitor input filter or **π-filter. It consists of a filter capacitor C_1 connected across the rectifier output, a choke L in series and another filter capacitor C_2 connected across the load. Only one filter section is shown but several identical sections are often used to improve the smoothing action.

* The shorthand name of inductor coil is choke.

** The shape of the circuit diagram of this filter circuit appears like Greek letter π (pi) and hence the name π-filter.

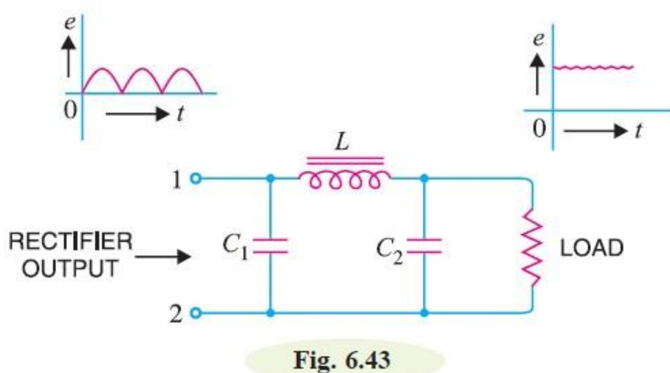


Fig. 6.43

The pulsating output from the rectifier is applied across the input terminals (*i.e.* terminals 1 and 2) of the filter. The filtering action of the three components *viz* C_1, L and C_2 of this filter is described below :

(a) The *filter capacitor C_1* offers low reactance to a.c. component of rectifier output while it offers infinite reactance to the d.c. component. Therefore, capacitor C_1 bypasses an appreciable amount of a.c. component while the d.c. component continues its journey to the choke L.

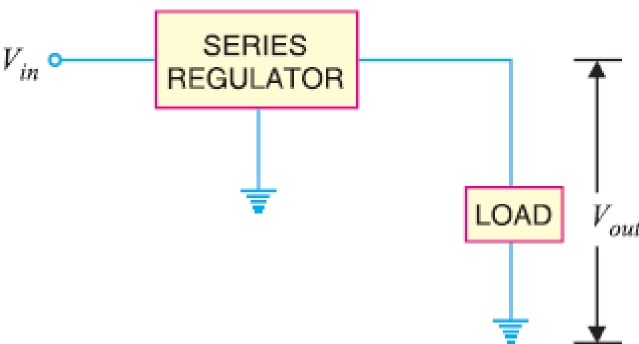
(b) The *choke L* offers high reactance to the a.c. component but it offers almost zero reactance to the d.c. component. Therefore, it allows the d.c. component to flow through it, while the *unbypassed a.c. component is blocked.

(c) The *filter capacitor C_2* bypasses the a.c. component which the choke has failed to block. Therefore, only d.c. component appears across the load and that is what we desire.

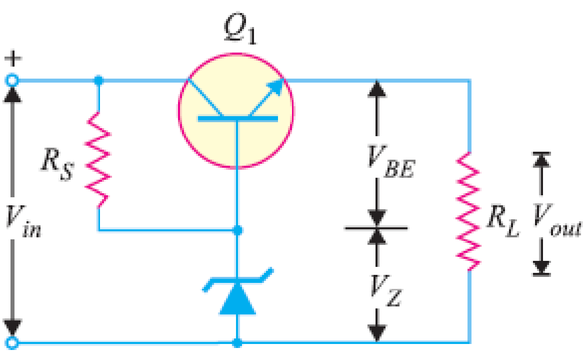
14. With circuit explain working of series voltage regulator. [Nov/Dec 2015]

- A device which maintains the output voltage of an ordinary power supply constant irrespective of load variations or changes in input a.c. voltage is known as a voltage regulator.

- The series regulator is placed in series with the load as shown in Fig. On the other hand, the shunt regulator is placed in parallel with the load. Each type of regulator provides an output voltage that remains constant even if the input voltage varies or the load current changes.



- The circuit is called a series voltage regulator because the load current passes through the series transistor *Q*1 as shown in Fig. below.
- The unregulated d.c. supply is fed to the input terminals and the regulated output is obtained across the load. The zener diode provides the reference voltage.



<u>Operation.</u>

- The base voltage of transistor Q1 is held to a relatively constant voltage across the zener diode. For example, if 8V zener (i.e., VZ = 8V) is used, the base voltage of Q1 will remain approximately 8V.

Referring to Fig.above,

$$V_{out} = V_Z - V_{BE}$$

- If the output voltage decreases, the increased base-emitter voltage causes transistor *Q*1 to conduct more, thereby raising the output voltage. As a result, the output voltage is maintained at a constant level.
- If the output voltage increases, the decreased base-emitter voltage causes transistor *Q*1 to conduct less, thereby reducing the output voltage. Consequently, the output voltage is maintained at a constant level.

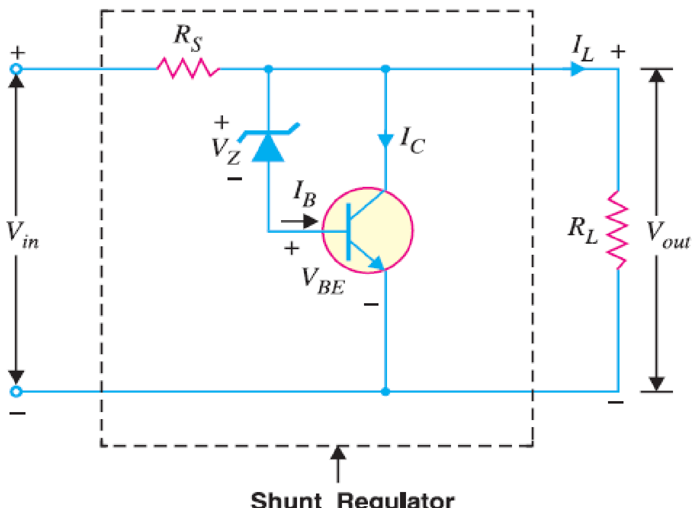
The advantage of this circuit is that the changes in zener current are reduced by a factor β. Therefore, the effect of zener impedance is greatly reduced and much more stabilised output is obtained

Limitations

- Although the changes in zener current are much reduced, yet the output is not absolutely constant.
- It is because both V_{BE} and V_Z decrease with the increase in room temperature. The output voltage cannot be changed easily as no such means is provided.

15. Draw the working of shunt voltage regulator and explain its working. [Nov/Dec 2014]

- A device which maintains the output voltage of an ordinary power supply constant irrespective of load variations or changes in input a.c. voltage is known as a voltage regulator.



- A shunt voltage regulator provides regulation by shunting current away from the load to regulate the output voltage. Fig. shows the circuit of shunt voltage regulator.
- The voltage drop across series resistance depends upon the current supplied to the load RL.
- The output voltage is equal to the sum of zener voltage (V_Z) and transistor base-emitter voltage (V_{BE})

i.e.,

$$V_{out} = V_Z + V_{BE}$$

- If the load resistance decreases, the current through base of transistor decreases.
- As a result, less collector current is shunted.
- Therefore, the load current becomes larger, thereby maintaining the regulated voltage across the load. Reverse happens should the load resistance increase.

Drawbacks:

A shunt voltage regulator has the following drawbacks:

(i) A large portion of the total current through R_S flows through transistor rather than to the load.

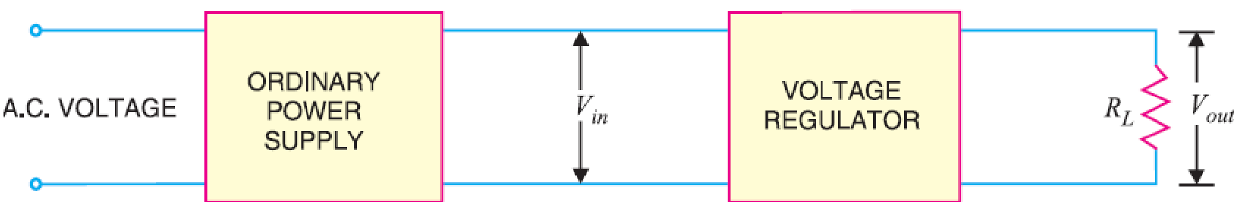
(ii) There is considerable power loss in R_S.

(iii) There are problems of overvoltage protection in this circuit.

For these reasons, a series voltage regulator is preferred over the shunt voltage regulator.

16. Draw the circuit of regulated power supply and explain its working. [Nov/Dec 2014]

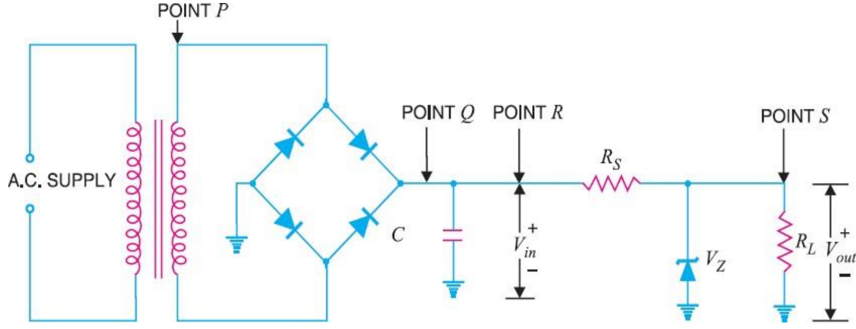
A d.c. power supply which maintains the output voltage constant irrespective of a.c. mains fluctuations or load variations is known as regulated d.c. power supply.



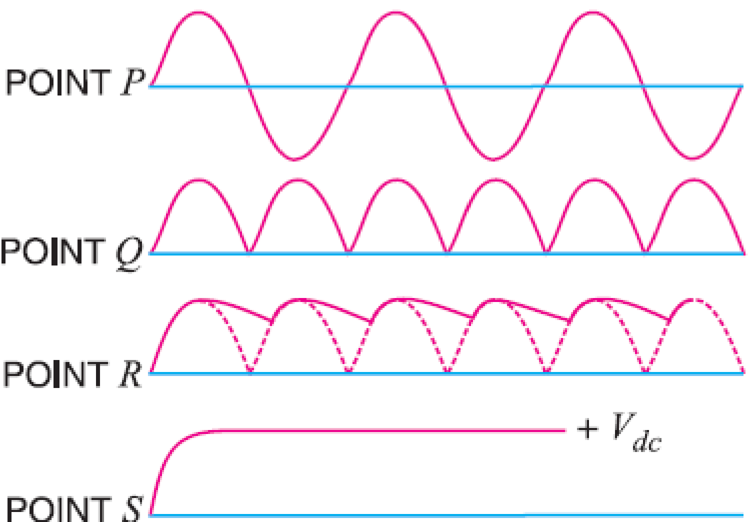
- A regulated power supply consists of an ordinary power supply and voltage regulating device. Fig. above shows the block diagram of a regulated power supply.
- The output of ordinary power supply is fed to the voltage regulator which produces the final output.
- The output voltage remains constant whether the load current changes or there are fluctuations in the input a.c. voltage. Fig. shows the complete circuit of a regulated power supply using zener diode as a voltage regulating device.
- As you can see, the regulated power supply is a combination of three circuits viz.,

  i) Bridge rectifier (ii) a capacitor filter C and (iii) zener voltage regulator.

- The bridge rectifier converts the transformer secondary a.c. voltage (point P) into pulsating voltage (point Q).
- The pulsating d.c. voltage is applied to the capacitor filter. This filter reduces the pulsations in the rectifier



- Finally, the zener voltage regulator performs two functions.
- Firstly, it reduces the variations in the filtered output voltage.
- Secondly, it keeps the output voltage (Vout) nearly constant whether the load current changes or there is change in input a.c. voltage. Fig. above shows the waveforms at various stages of regulated power supply.
- Note that bridge rectifier and capacitor filter constitute an ordinary power supply.
- However, when voltage regulating device is added to this ordinary power supply, it turns into a regulated power supply.



<u>Need for Regulated Power Supply</u>

In an ordinary power supply, the voltage regulation is poor *i.e.* d.c. output voltage changes appreciably with load current. Moreover, output voltage also changes due to variations in the input a.c. voltage.

This is due to the following reasons:

(i) In practice, there are considerable variations in a.c. line voltage caused by outside factors beyond our control. This changes the d.c. output voltage. Most of the electronic circuits will refuse to work satisfactorily on such output voltage fluctuations. This necessitates to use regulated d.c. power supply.

(ii) The internal resistance of ordinary power supply is relatively large (> 30 Ω). Therefore, output voltage is markedly affected by the amount of load current drawn from the supply. These variations in d.c. voltage may cause erratic operation of electronic circuits. Therefore, regulated d.c. power supply is the only solution in such situations.

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DEPARTMENT OF ELECTRICAL & ELECTRONICS ENGINEERING

Subject Name: **ELECTRONIC DEVICES AND CIRCUITS** Subject Code: **EE T34**

UNIT –V SPECIAL TWO-TERMINAL DEVICES

Principle of operation of Schottky diode, Varactor diode, Zener diode, Tunnel diode and PIN Diodes. OPTO ELECTRONIC DEVICES: Principle of operation and characteristics of Photo diodes, Phototransistors, Photoconductive cells, LEDs and LCDs, Opto-couplers, Solar cells and thermistors.

(2 MARKS)

1. **Give some applications of tunnel diode. [Nov/Dec 2014]**
   - Oscillator circuits
   - microwave circuits
   - Resistant to nuclear radiation
2. **Why schottky diode is called hot carrier diode? [Nov/Dec 2014]**
   - A Schottky barrier diode is also called as known as Schottky or hot carrier diode. Barrier stands for the potential energy barrier for electrons at the junction. When the diode is unbiased, electrons on the N side have low energy levels than electrons in the metal and so electrons cannot cross the junction barrier, called schottky barrier.
   - When the diode is forward biased, the electrons on the N side gain enough energy to cross the junction and enter the metal.
   - Since these electrons plunge into the metal with very large energy, they are called as hot carriers and diode is called hot carrier diode.

3. Draw the symbol and equivalent circuit of a varactor diode. [Nov/Dec 2014]

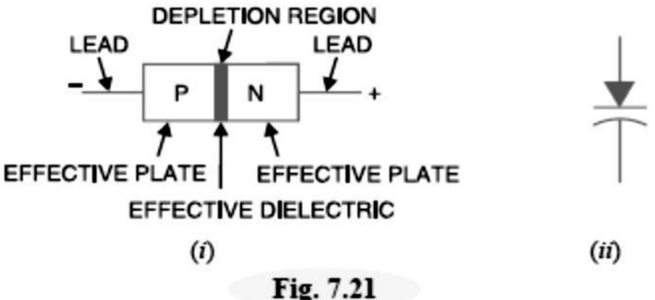
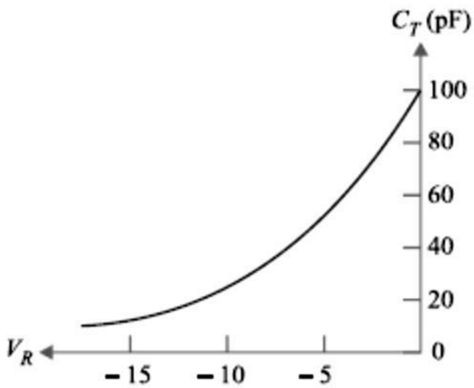


Fig. 7.21

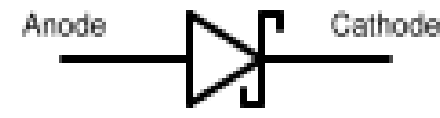
4. What are solar cells? [Nov/Dec 2014] .[April/May 2014]

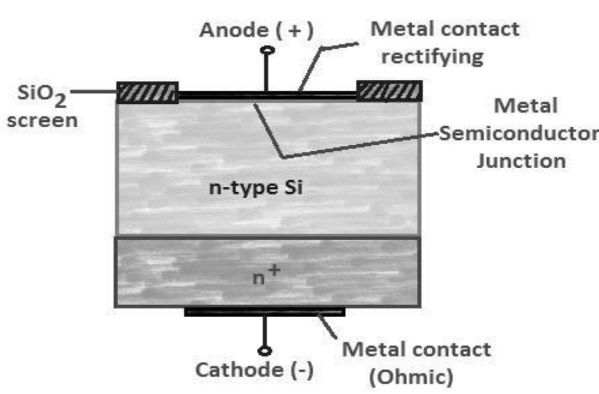
- Solar cell is a photovoltaic device that converts the light energy into electrical energy based on the principles of photovoltaic effect.
- The photovoltaic effect is the photo generation of charge carriers in a light absorbing material as a result of absorption of light radiation.

5. Draw the characteristics of varactor diode. [Nov/Dec 2015]



6. Give the symbol and structure of schottky diode[April 2015]





7. What is zener breakdown? [April 2015]

Zener break down takes place when both sides of the junction are very heavily doped and Consequently the depletion layer is thin and consequently the depletion layer is tin.When a small value of reverse bias voltage is applied , a very strong electric field is set up across the thin depletion layer. This electric field is enough to break the covalent bonds. Now extremely large number of free charge carriers are produced which constitute the zener current. This process is known as zener break down.

8. What is an optocoupler? [April 2015]

An optoisolator (also called optocoupler) is a device that uses light to couple a signal from its input (a photoemitter e.g., a LED) to its output (a photodetector e.g., a photo-diode).

9. Mention the application of zener diode. [April 2015]

Shunt regulators.

10. State the working principle of photodiode.

- Photodiode is a two terminal semiconductor PN junction device and is designed to operate in reverse bias. When light energy bombards a PN junction, it dislodges valence electrons.
- The more light striking the junction, the larger the reverse current in a diode.
- It is due to generation of more and more charge carriers with increase in level of illumination.

11. What is dark current of a photodiode?

The current that exists when no light is incident is called dark current.

12. What is PIN photodiode?

PIN photodiode consists of a P-region and N-region separated by an intrinsic region where width of intrinsic region is much larger than the space charge width of ordinary PN junction.

13. What is an optocoupler?

Optocoupler is a device that contains an infrared LED and a photodetector (such as photodiode, phototransistor) combined in a package.

(11 MARKS)

1. Explain construction, operation, applications and varactor diode [April/may2014][Nov/Dec 2014][Nov 2013]

A junction diode which acts as a variable capacitor under reverse bias and whose mode of operation depends on capacitance of the depletion layer is known as a varactor **diode.**

It is also known as **varicap, voltcap or tunning** diode.

<u>Construction</u>

- When a PN junction is formed, depletion layer is created in the junction area.
- Since there are no charge carriers within the depletion zone, the zone acts as an insulator.
- The p-type material with holes (considered positive) as majority carriers and n-type material with electrons (–ve charge) as majority carriers act as charged plates.
- Thus the diode may be considered as a capacitor with n-region and p-region forming oppositely charged plates and with depletion zone between them acting as a dielectric.

- The values of capacitance of varactor diodes are in the Pico farad (10^{-12} F) range.

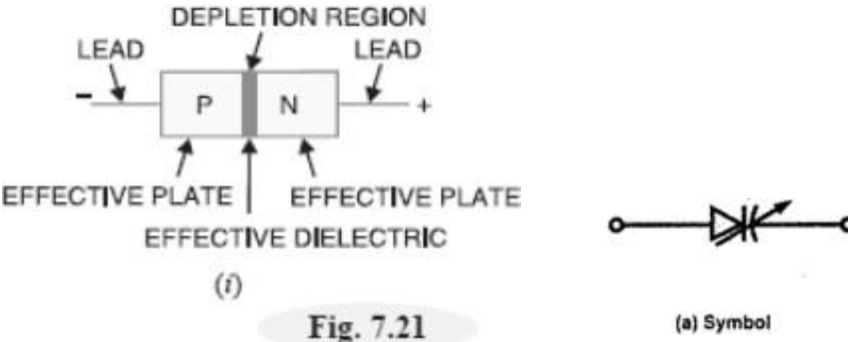


Fig. 7.21

Working:

- For normal operation, a varactor diode is always reverse biased.
- The capacitance of varactor diode is found as:

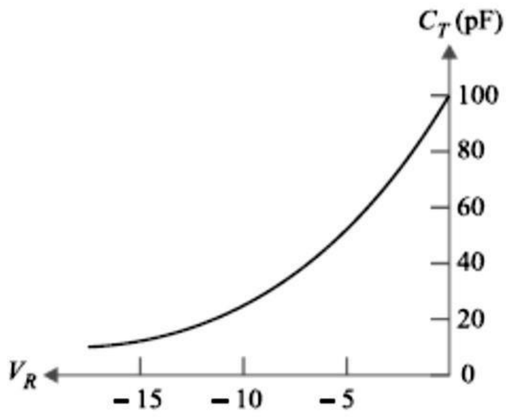
$$C_T = \varepsilon \frac{A}{W_d}$$

Where C_T = Total capacitance of the junction

ε = Permittivity of the semiconductor material

A = Cross-sectional area of the junction

W_d = Width of the depletion layer



- When reverse voltage across a varactor diode is increased, the width W_d of the depletion layer increases.
- Therefore, the total junction capacitance C_T of the junction decreases.
- On the other hand, if the reverse voltage across the diode is lowered, the width W_d of the depletion layer decreases.
- Consequently, the total junction capacitance C_T increases.
- Note that C_T can be changed simply by changing the voltage V_R.
- For this reason, a varactor diode is sometimes called **voltage-controlled capacitor.**
- In varactor diode, the capacitance parameters are controlled by the method of doping in the depletion layer or the size of the diode.

Application of Varactor Diode

- We have discussed that we can increase or decrease the junction capacitance of varactor diode simply by changing the reverse bias on the diode.
- This makes a varactor diode ideal for use in circuits that require voltage-controlled tuning. Fig. 7.23 shows the use of varactor diode in a tuned circuit.
- Note that the capacitance of the varactor is in parallel with the inductor.
- The varactor and the inductor form a parallel LC circuit. For normal operation, a varactor diode is always operated under reverse bias. In fact, this condition is met in the circuit shown in Fig. 7.23.

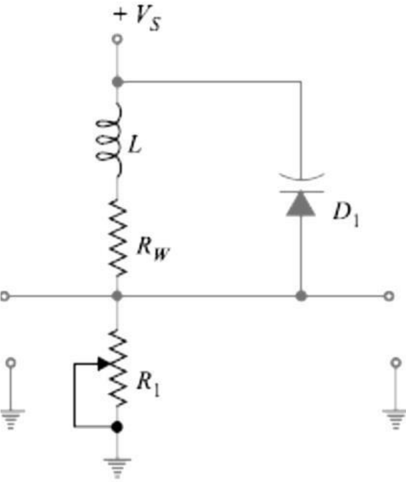


Fig. 7.23

- The resistance RW in the circuit is the winding resistance of the inductor.
- This winding resistance is in series with the potentiometer R1.
- Thus R1 and RW form a voltage divider that is used to determine the amount of reverse bias across the varactor diode D1 and therefore its capacitance.
- By adjusting the setting of R1, we can vary the diode capacitance.
- This, in turn, varies the resonant frequency of the LC circuit. The resonant frequency f_r of the LC circuit is given by;

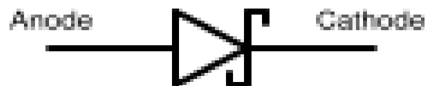
$$f_r = 1/2\pi LC$$

- If the amount of varactor reverse bias is decreased, the value of C of the varactor increases.
- The increase in C will cause the resonant frequency of the circuit to decrease.
- Thus, a decrease in reverse bias causes a decrease in resonant frequency and vice-versa.

2. With diagram and characteristics explain operation of schottky diode. [Nov/Dec 2015]

- At low frequencies, ordinary diode can be easily turned off when bias changes from forward to reverse.
- At higher frequencies, the diode cannot turn off fast due to effect of charge storage.
- The charge storage problem of P-N junction can be minimize or limited in schottky diodes.

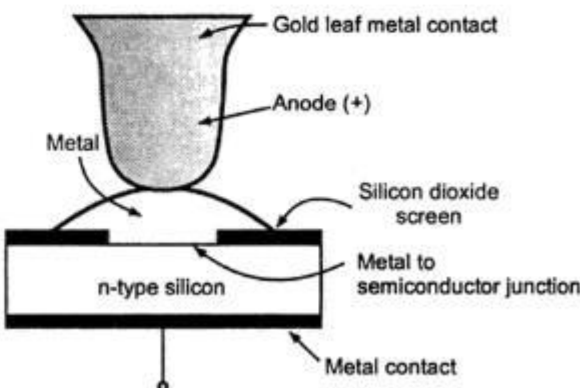
- A Schottky barrier diode is a metal semiconductor junction formed by bringing metal in contact with a moderately doped n type semiconductor material.
- A Schottky barrier diode is also called as known as Schottky or hot carrier diode. Barrier stands for the potential energy barrier for electrons at the junction.
- It is a unilateral device conducting currents in one direction (Conventional current flow from metal to semiconductor) and restricting in the other.
- It is also sometimes referred to as the surface barrier diode.
- The potential barrier is set with a contact between a metal & semiconductor.
- The rectifying action is depends on majority carrier only. As the result there are is no excess minority carrier to recombination hence low level of reverse recovery time.
- These diodes are used as rectifier at a single frequency exceeding 300 MHz to 20 GHz.



Schottky diode symbol

- If current flows through a diode there is a small voltage drop across the diode terminals.
- A normal silicon diode has a voltage drop between 0.6–0.7 volts, while a Schottky diode voltage drop is between approximately 0.15–0.45 volts. This lower voltage drop can provide higher switching speed and better system efficiency.

Construction:



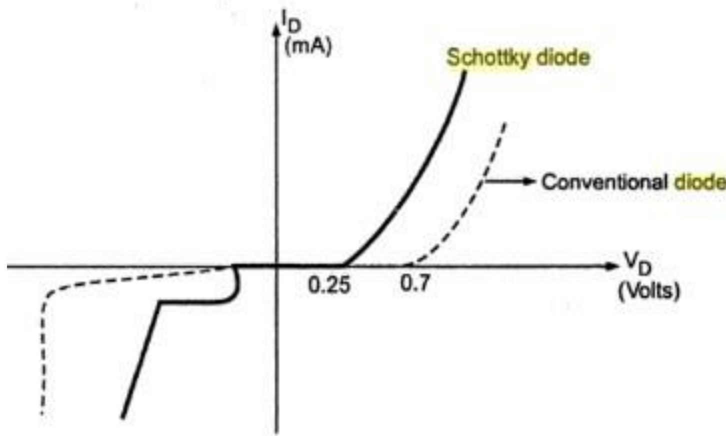
- It is a metal semiconductor junction diode without depletion layer. On one side of junction a metal like gold, silicon, platinum is used and other side N type doped semiconductor is used.
- For protection purpose metal layer is surrounded by gold or silver layer.
- The metal film forms the positive electrode and semiconductor is the cathode.

Working:

- When the diode is unbiased, electrons on the N side have low energy levels than electrons in the metal and so electrons cannot cross the junction barrier, called schottky barrier.
- When the diode is forward biased, the electrons on the N side gain enough energy to cross the junction and enter the metal.
- Since these electrons plunge into the metal with very large energy, they are called as hot carriers and diode is called hot carrier diode.

Characteristics:

- The barrier at the junction for schottly diode is less than that of normal p-n junction diode,in both forward and reverse bias region.
- The barrier potential and breakdown voltage in forward and reverse bias region are also less.
- The barrier potential of schottky diode is 0.25 V as compared to 0.7 V for normal diode.



Advantages:

- Schottky diode turns on and off faster than ordinary P-N junction diode the basic reason behind this is that schottky diodes are based on majority carrier.
- As there is no minority carrier there is no worry about depletion layer.
- It has much less voltage overshoot.

Disadvantages:

- Limited high-temperature operation
- High leakage
- Limited breakdown voltage range for Silicon Schottky diode

Applications:

- The Schottky diode or Schottky Barrier diode is an electronics component that is widely used for radio frequency, RF applications as a mixer or detector diode.
- The diode is also used in power applications as a rectifier, again because of its low forward voltage drop leading to lower levels of power loss compared to ordinary PN junction diodes.
- Solar cell applications and in voltage clamping circuits.

3. Explain the tunneling phenomena in a tunnel diode with transfer characteristics curves and state the advantages. [Nov/Dec 2014] [Nov/Dec 2015]

- A conventional diode exhibits positive resistance when it is forward biased or reverse biased.
- The tunnel diode also known as Esaki diode is a high conductivity, heavily doped two terminal P-N junction.
- A **tunnel diode** is a pn junction that exhibits negative resistance between two values of forward voltage (i.e., between peak-point voltage and valley-point voltage).

Theory:

- The tunnel diode is basically a pn junction with heavy doping of p-type and n-type semiconductor materials.
- Tunnel diodes are usually fabricated from germanium, gallium arsenide
- In fact, a tunnel diode is doped approximately 1000 times as heavily as a conventional diode.
- This heavy doping result in a large number of majority carriers.
- Because of the large number of carriers, most are not used during the initial recombination that produces the depletion layer.
- As a result, the depletion layer is very narrow.
- In comparison with conventional diode, the depletion layer of a tunnel diode is 100 times narrower.
- The operation of a tunnel diode depends upon the tunneling effect and hence the name.

Tunneling effect:

- The heavy doping provides a large number of majority carriers.
- Because of the large number of carriers, there is much drift activity in p and n sections. This causes many valence electrons to have their energy levels raised closer to the conduction region.
- Therefore, it takes only a very small applied forward voltage to cause conduction.
- The movement of valence electrons from the valence energy band to the conduction band with little or no applied forward voltage is called **tunneling.**
- Valence electrons seem to tunnel through the forbidden energy band.
- As the forward voltage is first increased, the diode current rises rapidly due to tunneling effect.

- Soon the tunneling effect is reduced and current flow starts to decrease as the forward voltage across the diode is increased.
- The tunnel diode is said to have entered the negative resistance region.
- As the voltage is further increased, the tunneling effect plays less and less part until a valley-point is reached.
- From now onwards, the tunnel diode behaves as ordinary diode i.e., diode current increases with the increase in forward voltage.

V-I Characteristic

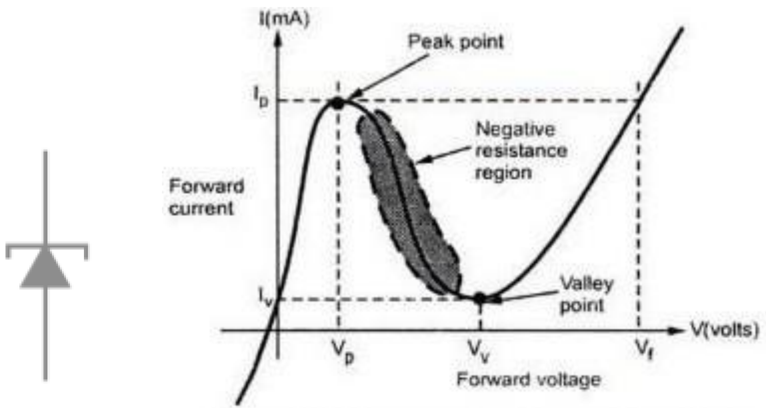


Fig. 7.18 (i) shows the V-I characteristic of a typical tunnel diode.

(i) As the forward voltage across the tunnel diode is increased from zero, electrons from the nregion "tunnel" through the potential barrier to the p-region.

As the forward voltage increases, the diode current also increases until the peak-point P is reached. The diode current has now reached peak current I_P (= 2.2 mA) at about peak-point voltage V_P (= 0.07 V). Until now the diode has exhibited positive resistance.

(ii) As the voltage is increased beyond V_P, the tunneling action starts decreasing and the diode current decreases as the forward voltage is increased until valley-point V is reached at valley-point voltage V_V (= 0.7V).

In the region between peak-point and valley-point (i.e., between points P and V), the diode exhibits negative resistance i.e., as the forward bias is increased, the current decreases. This suggests that tunnel diode, when operated in the negative resistance region, can be used as an oscillator or a switch.

(iii) When forward bias is increased beyond valley-point voltage V_V (= 0.7 V), the tunnel diode behaves as a normal diode.

In other words, from point V onwards, the diode current increases with the increase in forward voltage i.e., the diode exhibits positive resistance once again. Fig. 7.18. (ii) shows the symbol of tunnel diode.

It may be noted that a tunnel diode has a high reverse current but operation under this condition is not generally used.

Advantages:

- Low cost
- Low noise
- High speed of operation
- Low power

Disadvantages:

- It does not provide isolation between input and output circuits

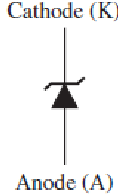
Applications:

- Can be used as an amplifier, oscillator or switch

4. Describe construction, operation, application and characteristics of zener diode. .[April/May 2014]

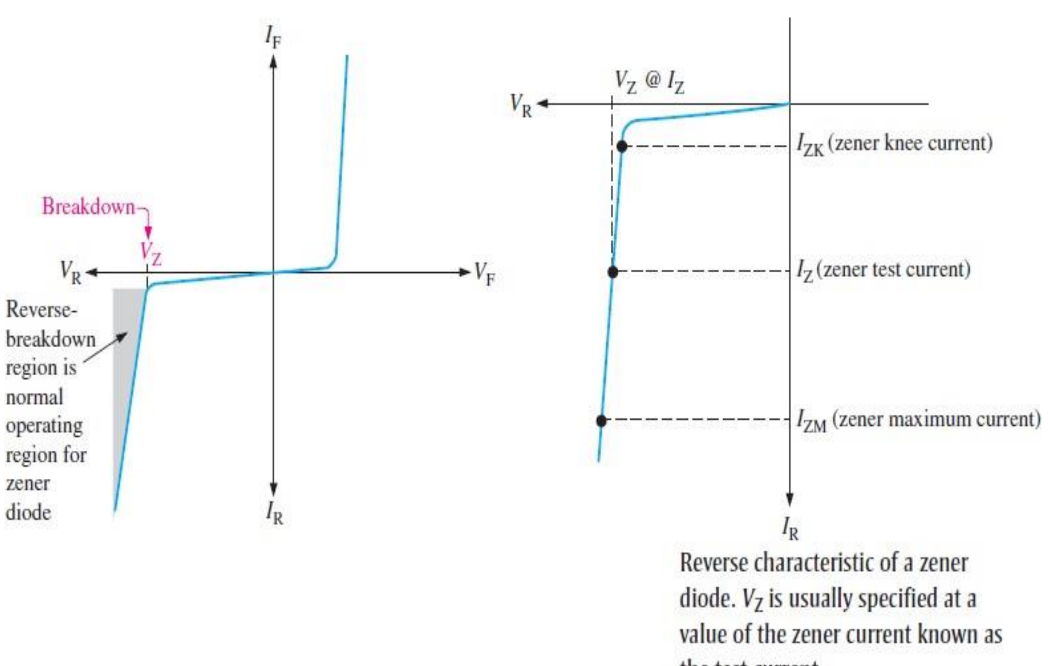
- A zener diode is a silicon PN junction device that is designed for operation in the breakdown region during reverse bias condition.
- It is also called as voltage reference, voltage regulator or breakdown diode.
- The breakdown voltage of a zener diode is set by carefully controlling the doping level during manufacture.

Symbol



- Two types of reverse breakdown in a zener diode are avalanche and zener.
- The avalanche effect occurs in both rectifier and zener diodes at a sufficiently high reverse voltage.
- Zener breakdown occurs in a zener diode at low reverse voltages.
- A zener diode is heavily doped to reduce the breakdown voltage.
- This causes a very thin depletion region.
- As a result, an intense electric field exists within the depletion region.
- Zener diodes with breakdown voltages of less than approximately 5 V operate predominately in zener breakdown.
- Those with breakdown voltages greater than approximately 5 V operate predominately in avalanche breakdown. Both types, however, are called zener diodes.
- Zeners are commercially available with breakdown voltages from less than 1 V to more than 250 V with specified tolerances from 1% to 20%.

V-I Characteristics



Reverse characteristic of a zener diode. V_Z is usually specified at a value of the zener current known as the test current.

- From the above figure it is seen that as the reverse voltage is increased, the reverse current remains negligibly small up to the „Knee" of the curve.
- At this point, the effect of breakdown process begins.
- From the bottom of the Knee, the breakdown voltage remains essentially a constant.
- There is a minimum value of zener current called **breakover current I_z** which must be maintained in order to keep the diode in breakdown region.
- There is a maximum value of Zener current above which the diode may be damaged
- Zener impedance is essentially the dynamic resistance of zener diode .
- It is defined as the reciprocal of the slope of the zener curve,

$$r_z=\frac{\Delta V_Z}{\Delta I_Z}$$

- Zener diodes with breakdown voltage near 7V have the smallest impedances.

Applications

- ✓ Used as voltage regulator
- ✓ Used as fixed reference voltage in transistor biasing circuits
- ✓ For meter protection against damage from accidental applications
- ✓ Used as peak clippers or limiters in wave shaping circuits

5. Explain photodiode and its characteristics.

- A **photo-diode** is a reverse-biased silicon or germanium pn junction in which reverse current increases when the junction is exposed to light.
- The reverse current in a photo-diode is directly proportional to the intensity of light falling on its pn junction.

- This means that greater the intensity of light falling on the pn junction of photo-diode, the greater will be the reverse current.

Principle:

- When a rectifier diode is reverse biased, it has a very small reverse leakage current. The same is true for a photo-diode.
- The reverse current is produced by thermally generated electron hole pairs which are swept across the junction by the electric field created by the reverse voltage.
- In a rectifier diode, the reverse current increases with temperature due to an increase in the number of electron-hole pairs.
- A photo-diode differs from a rectifier diode in that when its pn junction is exposed to light, the reverse current increases with the increase in light intensity and vice-versa.
- When light (photons) falls on the pn junction, the energy is imparted by the photons to the atoms in the junction.
- This will create more free electrons (and more holes). These additional free electrons will increase the reverse current.
- As the intensity of light incident on the pn junction increases, the reverse current also increases. In other words, as the incident light intensity increases, the resistance of the device (photo-diode) decreases.

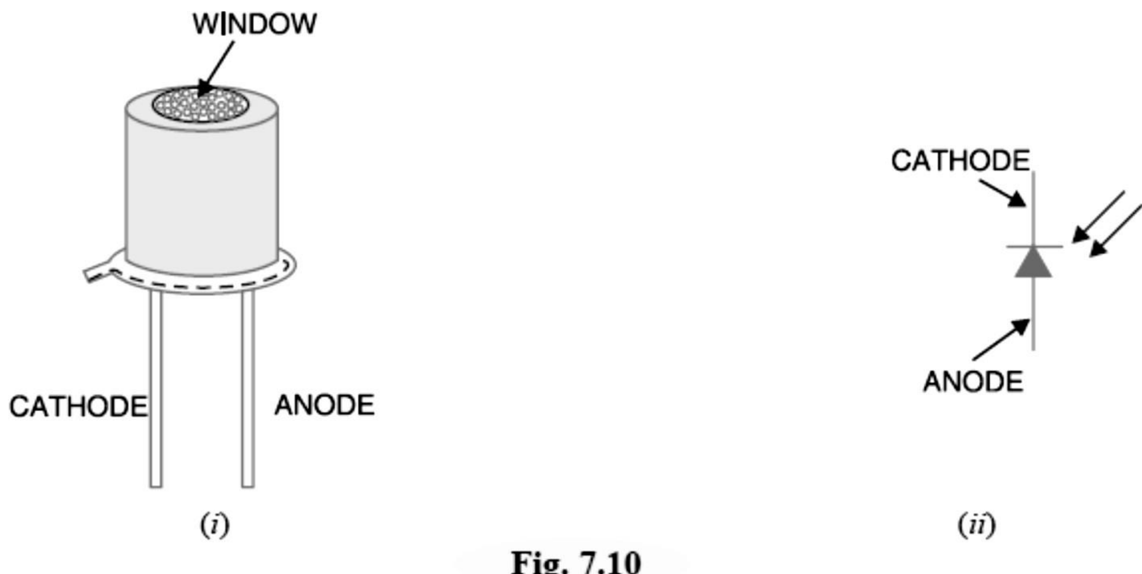


Fig. 7.10

Operation

Fig. 7.11 shows the basic photo-diode circuit. The circuit has reverse biased photo-diode, resistor R and d.c. supply. The operation of the photodiode is as under:

(i) When no light is incident on the pn junction of photo-diode, the reverse current I_r is extremely small. This is called dark current. The resistance of photo-diode with no incident light is called dark resistance (R_R).Dark resistance of photo-diode, R_R = Dark current V_R

(ii) When light is incident on the pn junction of the photo-diode, there is a transfer of energy from the incident light (photons) to the atoms in the junction. This will create more free electrons (and more holes). These additional free electrons will increase the reverse current.

(iii) As the intensity of light increases, the reverse current IR goes on increasing till it becomes maximum. This is called saturation current.

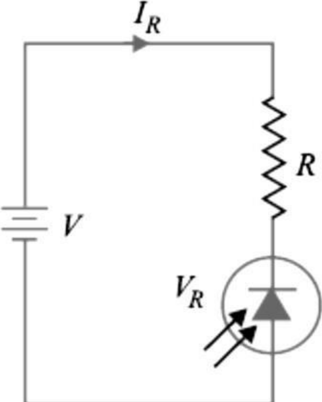


Fig. 7.11

There are two important characteristics of photodiode.

<u>(i) Reverse current-Illumination curve.</u>

Fig. 7.12 shows the graph between reverse current (I_R) and illumination (E) of a photo-diode.

- The reverse current is shown on the vertical axis and is measured in μA.
- The illumination is indicated on the horizontal axis and is measured in mW/cm2.
- Note that graph is a straight line passing through the origin.
- $\therefore I_R$ = m E where m = slope of the straight line
- The quantity m is called the sensitivity of the photo-diode.

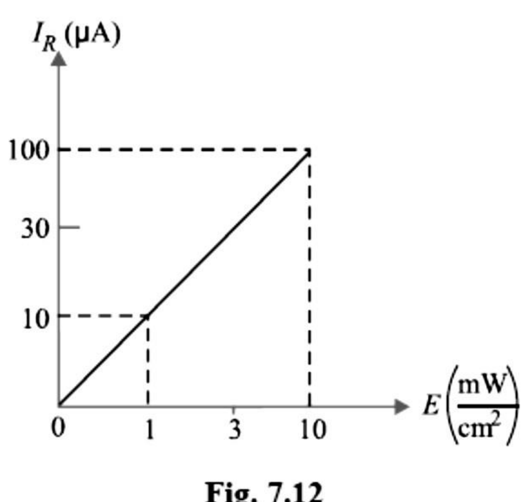


Fig. 7.12

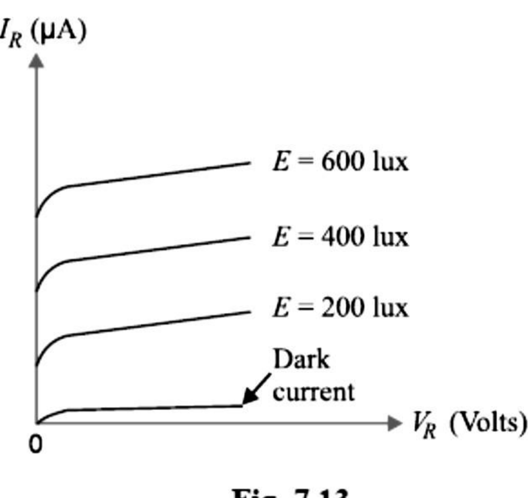


Fig. 7.13

<u>Reverse voltage-Reverse current curve:</u>

- Fig. 7.13 shows the graph between reverse current (I_R) and reverse voltage (V_R) for various illumination levels.
- It is clear that for a given reverse-biased voltage V_R, the reverse current I_R increases as the illumination (E) on the pn junction of photo-diode is increased.

Applications:

- Photodiodes are used in consumer electronic devices such as CD players, smoke detectors and for infrared remote control devices.
- Photo diodes are used as light sensors.
- It is used for accurate measurement of light intensity and industry.
- They are widely used in various medical applications such as detectors for computer tomography, instruments to analyze samples, and pulse oximeters.

6. Write the operation of photo transistor. .[April 2015]

- A Phototransistor is an electronic switching and current amplification component which relies on exposure to light to operate.
- When light falls on the junction, reverse current flows which is proportional to the luminance. Phototransistors are used extensively to detect light pulses and convert them into digital electrical signals.
- These are operated by light rather than electric current.
- Providing large amount of gain, low cost and these phototransistors might be used in numerous applications.
- It is capable of converting light energy into electric energy. Phototransistors work in a similar way to photo resistors commonly known as LDR (light dependant resistor) but are able to produce both current and voltage while photo resistors are only capable of producing current due to change in resistance.
- Phototransistors are transistors with the base terminal exposed. Instead of sending current into the base, the photons from striking light activate the transistor. This is because a phototransistor is made of a bipolar semiconductor and focuses the energy that is passed through it.
- These are activated by light particles and are used in virtually all electronic devices that depend on light in some way.

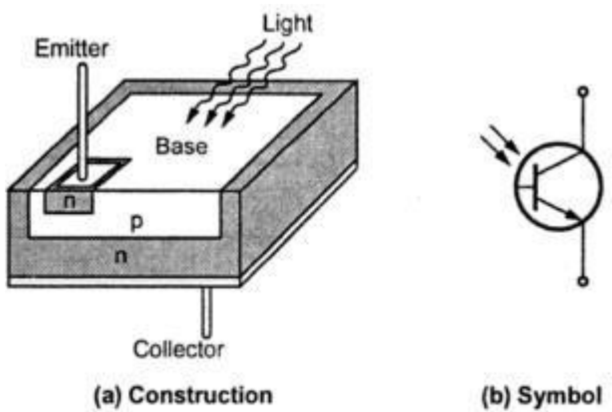
- All silicon photo sensors (phototransistors) respond to the entire visible radiation range as well as to infrared. In fact, all diodes, transistors, Darlington"s, triacs, etc. have the same basic radiation frequency response.
- The structure of the phototransistor is specifically optimized for photo applications. Compared to a normal transistor, a photo transistor has a larger base and collector width and is made using diffusion or ion implantation.

Features:

- Low-cost visible and near-IR photo detection.
- Available with gains from 100 to over 1500.
- Moderately fast response times.
- Available in a wide range of packages including epoxy-coated, transfer-molded and surface mounting technology.
- Electrical characteristics similar to that of signal transistors.

Construction:

- A photo transistor is nothing but an ordinary bi-poplar transistor in which the base region is exposed to the illumination.
- It is available in both the P-N-P and N-P-N types having different configurations like common emitter, common collector and common base. Common emitter configuration is generally used.
- It can also work while base is made open. Compared to the conventional transistor it has more base and collector areas.
- The base is the lead responsible for activating the transistor. It is the gate controller device for the larger electrical supply.
- The collector is the positive lead and the larger electrical supply. The emitter is the negative lead and the outlet for the larger electrical supply.



(a) Construction (b) Symbol

Working:

- With no light falling on the device there will be a small current flow due to thermally generated hole-electron pairs and the output voltage from the circuit will be slightly less than the supply value due to the voltage drop across the load resistor R.
- With light falling on the collector-base junction the current flow increases.
- With the base connection open circuit, the collector-base current must flow in the base-emitter circuit and hence the current flowing is amplified by normal transistor action. Collector base junction is very sensitive to light .
- Its working condition depends upon intensity of light.
- The base current from the incident photons is amplified by the gain of the transistor, resulting in current gains that range from hundreds to several thousands.
- A phototransistor is 50 to 100 times more sensitive than a photodiode with a lower level of noise.
- A phototransistor works just like a normal transistor, where the base current is multiplied to give the collector current, except that in a phototransistor, the base current is controlled by the amount of visible or infrared light where the device only needs 2 pins.
- Photo transistors available different configurations like opto isolator, optical switch, retro sensor.
- Opto isolator is similar to a transformer in that the output is electrically isolated from the input.
- An object is detected when it enters the gap of the optical switch and blocks the light path between the emitter and detector.

- The retro sensor detects the presence of an object by generating light and then looking for its reflectance off of the object to be sensed.

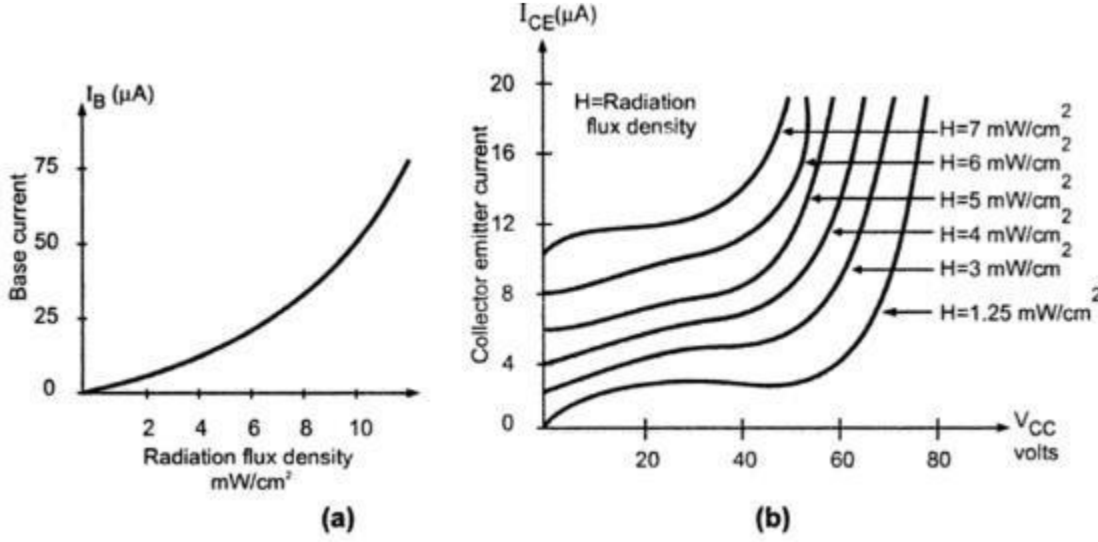


Fig. 3.77 Phototransistor characteristics

Advantages of Photo transistors:

Phototransistors have several important advantages that separate them from other optical sensor some of them are mentioned below

- Phototransistors produce a higher current than photo diodes.
- Phototransistors are relatively inexpensive, simple, and small enough to fit several of them onto a single integrated computer chip.
- Phototransistors are very fast and are capable of providing nearly instantaneous output.
- Phototransistors produce a voltage, that photo-resistors cannot do so.

Disadvantages of Photo transistors:

- Phototransistors that are made of silicon are not capable of handling voltages over 1,000 Volts.
- Phototransistors are also more vulnerable to surges and spikes of electricity as well as electromagnetic energy.
- Phototransistors also do not allow electrons to move as freely as other devices do, such as electron tubes.

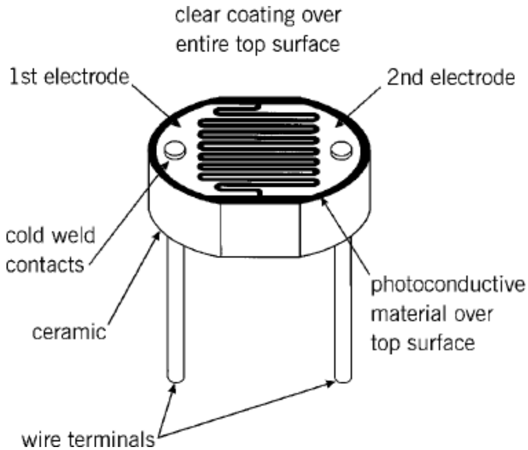
Applications

- Punch-card readers.
- Security systems
- Encoders – measure speed and direction
- IR detectors photo

- electric controls
- Computer logic circuitry.
- Relays

7. Write short notes on photoconductive cells.

- Photoconductive cells are light-sensitive resistors in which resistance decreases with an increase in light intensity when illuminated.



Construction

- These devices consist of a thin single-crystal or polycrystalline film of compound semiconductor substances.
- Most commercially available photoconductive cells are manufactured from cadmium sulfide (CdS), which is sensitive to light in the visible spectrum.
- Other materials that are less commonly used in photoconductive cells include lead sulfide (PbS), lead selenide (PbSe), and lead telluride (PbTe), although they react to infrared light, not the visible spectrum.
- CdS photoconductive cells (CdS cells) are often referred to as light dependant resistors (LDR).
- They function within the same general spectral range as the human eye, and are therefore widely used in applications where this type of spectral response is required.

Working:

- Photoconductive cells function by receiving light energy, which in turn free electrons from their valence bonds in semiconductor material.
- At room temperature, the number of free charges in a semiconductor is relatively limited, but the addition of light-released electrons raises conductivity (and thereby reduces resistance).
- This change is resistance may be as large are several hundred thousand ohms from a darkened state to only a few hundred ohms in sunlight.

- Embedding the conductive path within the semiconductor substrate, in a zig-zag pattern, will enhance the level of resistance.
- In addition to an increase in dark resistance, this same pattern will reduce the current as well, changing the output current to about one milliampere (mA) per lumen.

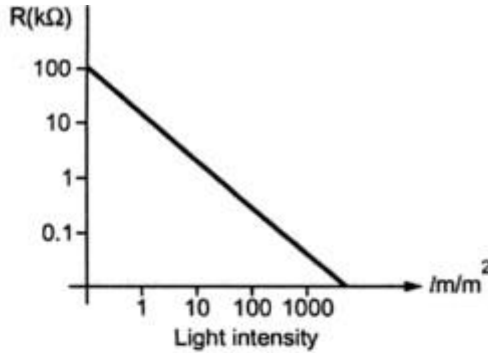


Fig. 3.61 Graph of change in resistance of photoconductive cell with light-intensity

Applications:

Photoconductive cells are generally inexpensive, and their small size and ease of use makes them popular in many applications. Some of the many uses include making street lights turn on and off automatically according to the level of daylight, in point-of-sale and inventory bar code reading devices, in security devices such as motion sensing lights and cameras, and in alarm systems. They also are used as light meters in photographic applications.

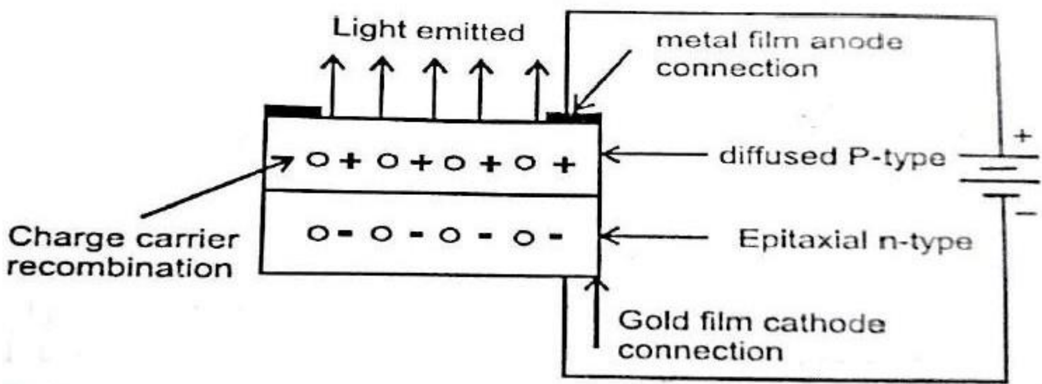
8. Explain the construction and principle of operation of LED. Also discuss the advantages, disadvantages and applications of LED. [Nov/Dec 2014]

- The LED is perhaps the most important of the display devices available today for use in instrumentation system.
- The LED is a PN junction device which emits light when a current passes through it in the forward direction. This phenomenon is called electroluminance.

Principle

- Whenever a-PN junction is forward biased, the forward current flows due to free electrons crossing from n-side and recombining with holes on the p-side.
- Recall that free electrons are found in conduction band.

- Hence they have greater energy than holes which are found in valence band.
- Whenever an electron recombines with the hole, it falls from conduction band to valence band, i.e, from higher energy level to lower energy level, as shown in fig.
  The energy is released either in the form of heat or light.
- The difference in energy between the conduction band and the valence band is called forbidden energy gap. Its value depends on the type of material.
- This value determines the wavelength of light emitted due to release of energy because of recombination of electron and hole.
- For silicon, the forbidden energy gap is approximately 1.1ev, and hence wavelength of the emitted light lies in the infrared region of the light spectrum.
- Since infrared is not visible, silicon cannot be used in the fabrication of LED. For the same reason, germanium also cannot be used.



- The material used for manufacturing LEDs is gallium arsenide, gallium phosphide and gallium arsenide phosphide.
- The colour of light emitted depends upon type amount of impurity added Red; green, yellow LEDs are commonly available.
- When forward biased, the voltage drop across LED is about 2 to 3 v, which is considerably greater than that across a silicon or germanium diode. Fig shows the characteristics of LED.

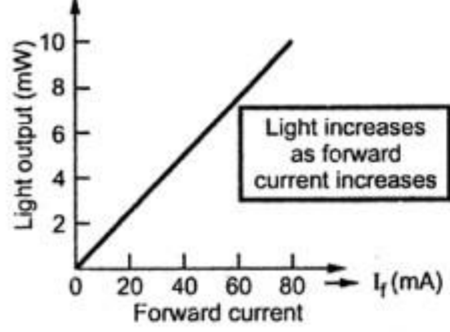


Fig. 1.8 LED output characteristic

Advantages

- Low Power consumption
- Very fast action
- Very small size and weight
- Extremely long size
- Operating voltage and current is less
- Variety of spectral output current
- No effect due to mechanical vibrations
- They can operate over wide range of temperature(0º to 700ºC)

Disadvantages

- Low efficiency
- Radiated output power is temperature dependent
- High power consumption compared to LCD
- It is a very sensitive device ie. It damages by over voltage and current.
- LED"s are not suitable for large area displays because of high cost

Applications:

- In power level indicator to indicate power ON/OFF conditions
- Displays of numeric and alpha numeric character
- In optical switching condition

9. Explain the construction and principle of operation of LCD

- LCD is passive type display devices used for display of numeric and alphanumeric character in dot-matrix and segmental display.
- The main advantage of LCD is the low power consumption because no light generation is required.
- Normally used such as noematic and cholesteric
-

Types:

Two types of LCD are

1. Dynamic scattering type

2. Field effect type

Dynamic scattering type:

Construction

- The molecules in ordinary liquids normally have random orientations.
- In liquid crystal the molecules are oriented in a definite crystal pattern, as shown in the figure1

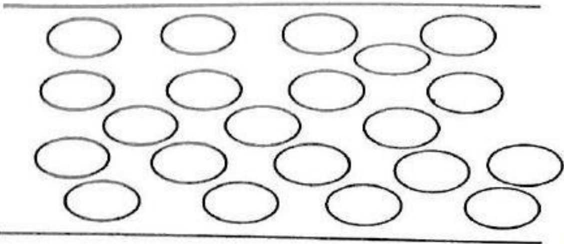


Fig. Molecules in liquid crystal when no current flows

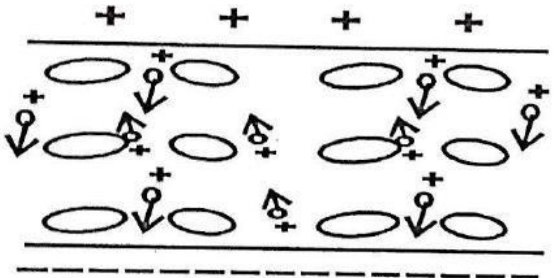


Fig 2 Charge carrier flow through liquid crystal disturbs molecular alignment and cause turbulence

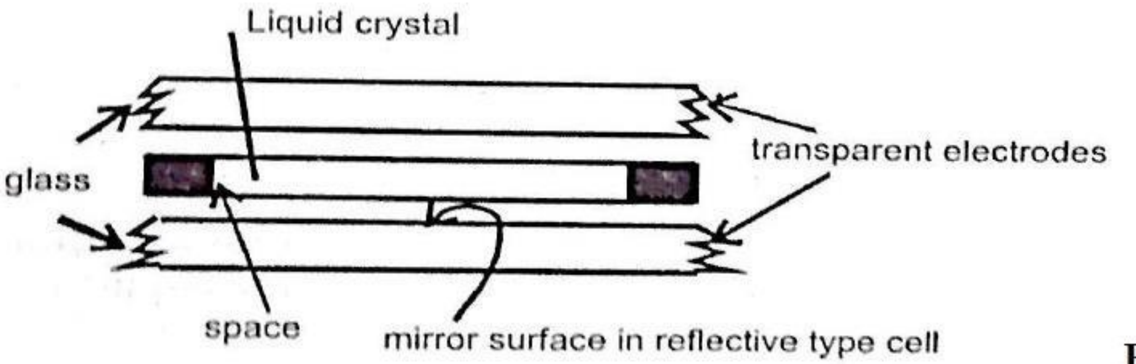


Fig. 3

- When electric fields to the liquid crystal, the molecules which are approximately cigar shaped, tend to align perpendicularly to the field charge carrier flowing through the liquid disrupts the molecular alignment and cause turbulence within the liquid when it is not activated.
- The molecular turbulence causes the light to be scattered in all direction, so that the activated areas appear bright. This phenomenon is known as **dynamic scattering**
- The actual liquid crystal materiel may be one several organic compound which exhibit the optical properties of solid while retaining the fluidity of the liquid.

➢ A liquid crystal cell consist of a liquid crystal materiel sandwiched between glass sheets with transparent metal film electrodes deposited on the inside faces as shown in the figure 3

➢ When both glass sheets are transparent the cell is known as "transmittive type cell". When only one glass sheet is transparent on the other has reflective coating, the cell is termed as "reflective type"

<u>Operation</u>

➢ When not activated, the transmittive type cell simply transmits the light through the cell in the straight lines. In this condition the cell will not appear bright.

➢ When the cell is activated, the incident light is scattered forward, as shown in the figure 4 and the cell appears quite bright even under high intensity light conditions

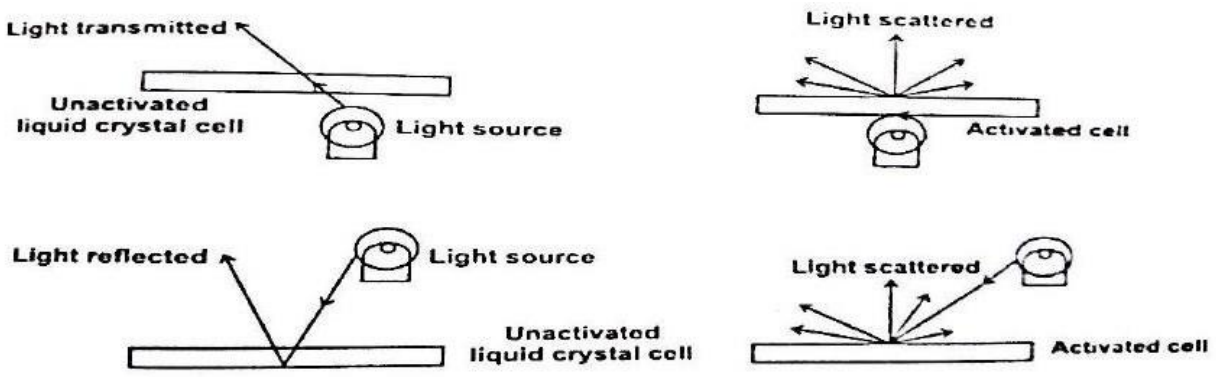


Fig 4

The reflective type LCD operation depends on the light incident on its front surface when it is not activated, light is reflected from the mirror surface, the cell does not appear bright when activated, the dynamic scattering phenomenon occurs and the cell appears quite bright.

<u>Field Effect LCD:</u>

➢ It is similar to the dynamic scattering type except that two thin polarizing optical filters are placed at the surface of each glass sheet.

➢ The liquid crystal materiel employed is known as **twisted pneumatic type**, it twists the light passing through when the coil is not energized.

➢ This twisting allows the light to pass through the polarizing filters.

➢ Thus in case of transmittive type cell, the un-energized cell can appear dark against a bright background. When energized cell becomes transparent and disappears into the back grounds

<u>Advantages of LCDs</u>

1. Less power consumption

2. Low cost

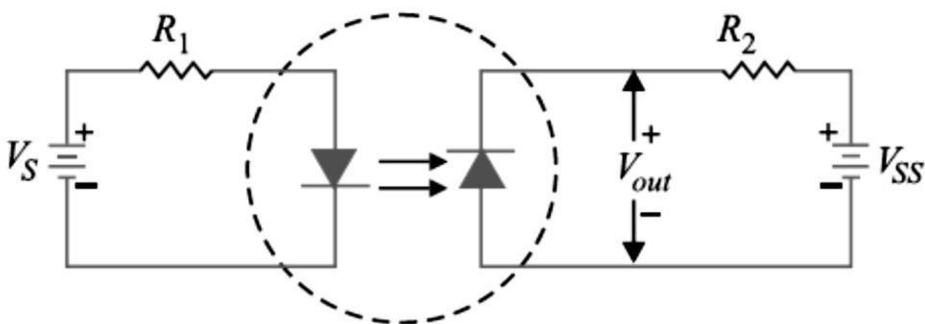
3. Uniform bright with good contrast.

4. Low operating Voltage and current

Disadvantage of LCDs

1. Poor reliability
2. Limited temperature rage
3. Poor visibility in low ambient temperature
4. Slow speed
5. Requires an A.C. drive

10. Write short notes on opto coupler[Nov/Dec 2014]



- An optoisolator (also called optocoupler) is a device that uses light to couple a signal from its input (a photoemitter e.g., a LED) to its output (a photodetector e.g., a photo-diode).
- Because of this it is possible to have an insulation resistance between the two circuits in thousands of megohms which provides electrical isolation between input and output circuits.
- Isolation is needed to prevent noise generated in one circuit from being passed to the other circuit.
- Optocouplers work s well either on ac or dc high voltage signals.
- Signal converters employing optical coupling are sometimes referred to as universal signal converters.

Fig. 7.17 shows a LED-photo diode optoisolator.

- The LED is on the left and the photo-diode is on the right.
- The arrangement shown in Fig. 7.17 is referred to as optocoupling because the output from the LED circuit is coupled via light to the photo-diode circuit.
- When the LED is energized, current flows through the LED. The light from the LED hits the photo diode and sets up a reverse current through resistor R_2.

The voltage across the photo-diode is given by:

$$V_{out} = V_{SS} – I R_2$$

- The output voltage depends on how large the reverse current is. If we vary the LED supply, the amount of light changes and this causes the photo diode current to change.
- As a result, Vout changes.

Disadvantages:

- They are fairly expensive.
- They are bulkier and heavier than optical devices.

Applications

Used as a signal converter between high voltage pilot devices and low voltage solid state logic circuits.

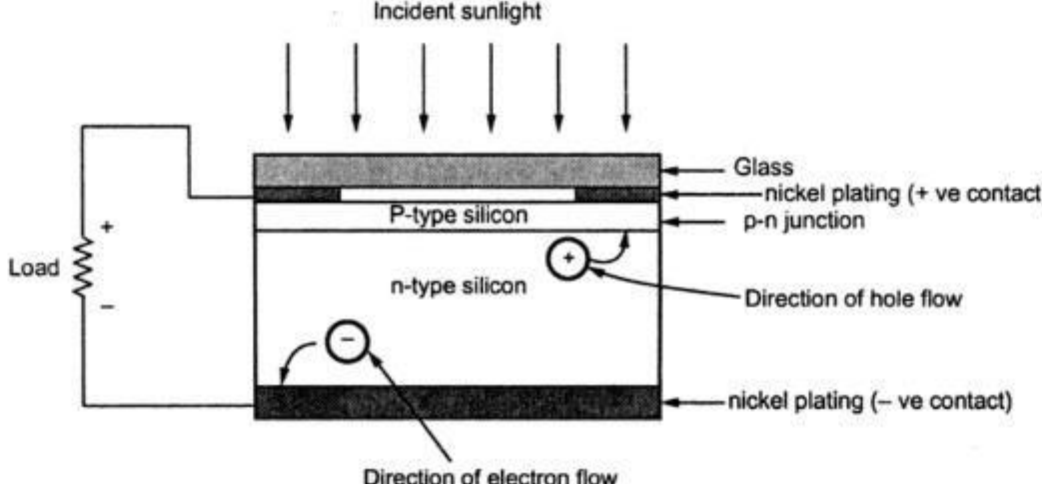
11. With neat diagram explain the operation of solar cell.(Nov 2013)

Solar cell is a photovoltaic device that converts the light energy into electrical energy based on the principles of photovoltaic effect.

Principle:

- The solar cells are based on the principles of photovoltaic effect.
- The photovoltaic effect is the photon generation of charge carriers in a light absorbing material as a result of absorption of light radiation.

Construction:



- Solar cell (crystalline Silicon) consists of a n-type semiconductor (emitter) layer and p-type semiconductor layer (base).

- The two layers are sandwiched and hence there is formation of p-n junction. The surface is coated with anti-refection coating to avoid the loss of incident light energy due to reflection.
- A proper metal contacts are made on the n-type and p-type side of the semiconductor for electrical connection

Materials for Solar cell:

Solar cells are composed of various semiconducting materials

1. Crystalline silicon
2. Cadmium telluride
3. Copper indium diselenide
4. Gallium arsenide
5. Indium phosphide
6. Zinc sulphide

Note: Semiconductors are materials, which become electrically conductive when supplied with light or heat, but which operate as insulators at low temperatures.

Working:

- When a solar panel exposed to sunlight, the light energies are absorbed by semiconducting materials.
- Due to this absorbed energy, the electrons are liberated and produce the external DC current.
- The DC current is converted into 240-volt AC current using an inverter for different applications.
- A PN junction consists of two different regions of a semiconductor material (usually silicon), with one side called the p type region and the other the n-type region.
- During the incident of light energy, in p-type material, electrons can gain energy and move into the n-type region.
- Then they can no longer go back to their original low energy position and remain at a higher energy.
- The process of moving a light- generated carrier from p-type region to n-type region is called collection.
- These collections of carriers (electrons) can be either extracted from the device to give a current, or it can remain in the device and gives rise to a voltage.

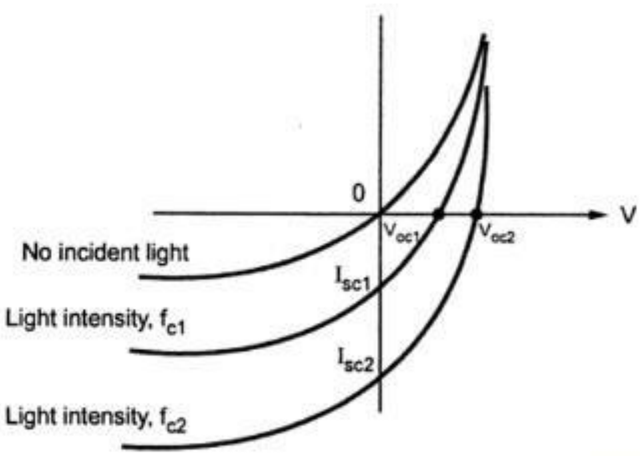


Fig. 3.73 I_{SC} and V_{OC} versus light intensity for a solar cell

Advantage:

1. It is clean and non-polluting
2. It is a renewable energy
3. Solar cells do not produce noise and they are totally silent.
4. They require very little maintenance
5. They are long lasting sources of energy which can be used almost anywhere
6. They have long life time
7. There are no fuel costs or fuel supply problems

Disadvantage:

1. Solar power can be obtained in night time.
2. Solar cells (or) solar panels are very expensive.
3. Energy has not been stored in batteries.
4. Air pollution and whether can affect the production of electricity.
5. They need large are of land to produce more efficient power supply.

Applications:

1. **Solar pumps** are used for water supply.
2. **Domestic power supply** for appliances include refrigeration, washing machine, television and lighting
3. **Ocean navigation aids:** Number of lighthouses and most buoys are powered by solar cells
4. **Telecommunication systems:** radio transceivers on mountain tops, or telephone boxes in the country can often be solar powered
5. **Electric power generation in space**: To providing electrical power to satellites in an orbit around the Earth.

12. Write short notes on thermistor.

A resistor which is thermally sensitive is called thermistor. The value of resistor is a function of temperature in case of a thermistor. The resistance value not only depends on an ambient temperature but also on temperature due to the internal power dissipation. High temperature coefficient is the feature of thermistors.

According to the temperature coefficient the thermistors are classified as,

1. Negative temperature coefficient thermistors, very commonly denoted as NTC.
2. Positive temperature coefficient thermistors, very commonly denoted as PTC.

1.2.7.1 NTC Thermistors

These thermistors are semiconductors of ceramic materials. These are manufactured by sintering various mixtures of oxides of nickel, manganese, cobalt, titanium, copper, uranium and iron. The general formula of NTC thermistor is,

$$A^{++} B^{+++} O_4$$

where A = Divalent forming oxide of type AO

i.e. NiO, CuO

and B = Trivalent forming oxide of type B_2O_3

i.e. Mn_2O_3, Fe_2O_3

By varying both the types of oxides the size, configuration and electrical characteristics of thermistors can be controlled. The standard configurations are beads, glass probes, discs, rods and washers.

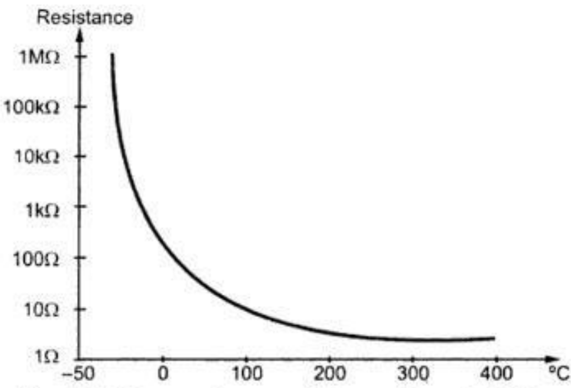


Fig. 1.16 Temperature resistance characteristics

1.2.7.2 PTC Thermistors

These thermistors are manufactured by using two kinds of material compounds having,

- Barium titanate structure called positors.
- Diamond lattice type structure as silicon called silistors.

The resistivity of PTC thermistor varies abruptly with temperature. It increases above a critical point very fast. This critical temperature is break point and is called curie temperature. This temperature can be changed up or down by controlling the composition of materials. The temperature-resistance characteristics of PTC thermistor is shown in the Fig. 1.17

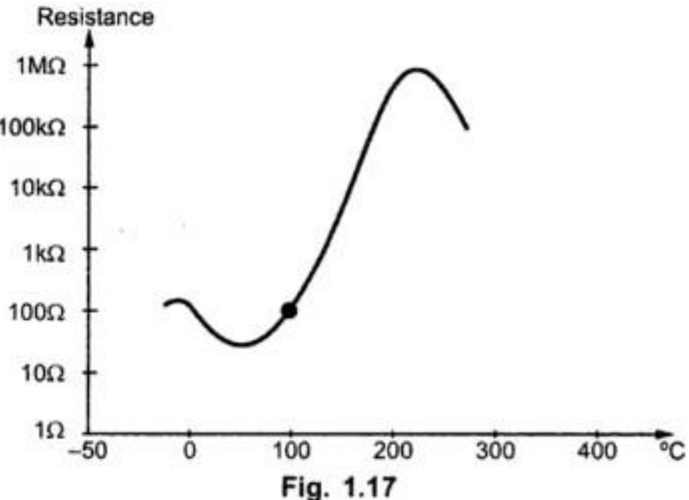


Fig. 1.17

Both PTC and NTC thermistors are operated in the two modes. One mode in which current is kept low and temperature and resistance are determined by ambient conditions only. This is called small signal or extremely heated mode. In second mode the temperature and resistance are determined mainly by internal power dissipation as well as ambient changes. This is called large signal or self heated operation mode.

1.2.7.3 Characteristic Curves of Thermistors

The time current characteristics of NTC thermistor is shown in the Fig. 1.18

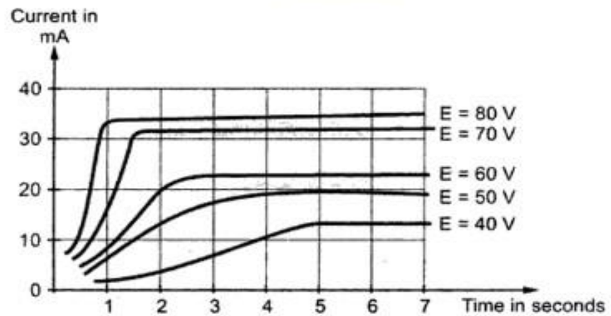


Fig. 1.18 Time current characteristics of NTC thermistor

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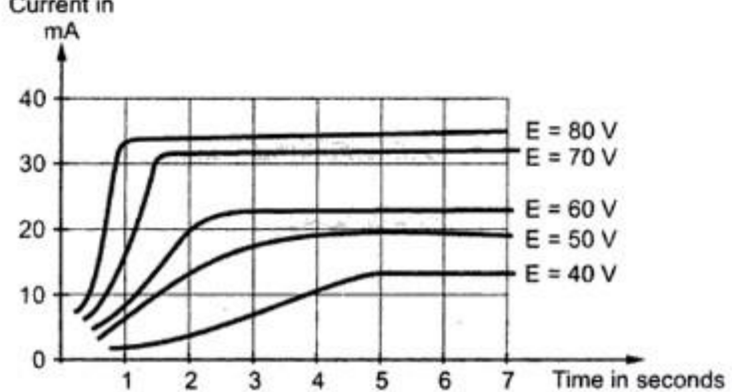

Fig. 1.18 Time current characteristics of NTC thermistor

13. Write notes n PIN diode.

- In this diode a high resistivity intrinsic layer is sandwiched between P and N regions.
- The high resistance of the intrinsic layer provides the possibility of larger electric field between the P and N regions; thereby electron hole pair generation is enhanced enabling Pin diode to process every weak signal.

<u>Working:</u>

- When there is no bias applied to diode, there will be diffusion of charge carriers due to concentration gradient across the junction.
- Consider NI junction, diffusion results in very thin depletion layer in N region and thicker in I region.
- When the reverse bias is applied and increased gradually, the thickness of the depletion layers increase until the entire I region is swept free of mobile carriers.
- The reverse bias voltage required to sweep out is called swept-out voltage.
- When forward biased is applied, more and more charge carriers inject into the I region from P-N regions and forward resistance is reduced. Thus it acts like a variable resistance.

Applications:

- Can be used a variable attenuator in microwave applications
- Phase shifter
- In construction of phase modulator and amplitude modulator.