ELECTRONIC DEVICES AND CIRCUITS BM T33

UNIT– IV MULTISTAGE AMPLIFIERS & DIFFERENTIAL AMPLIFIERS

2 MARKS

1. Define CMRR & Write its significance.(or) What is meant by CMRR of a differential amplifier.(Nov 14, May 15, Nov 15, May 17, Nov 17)

CMRR:

The common-mode rejection ratio(CMRR) of a differential amplifier is defined as the ratio of the differential-mode gain to common-mode gain.

CMRR = |Ad|Ac|

Significance of CMRR:

The **CMRR** is a very important specification, as it indicates how much of the common-mode signal will appear in your measurement. The value of the **CMRR** often depends on signal frequency as well, and must be specified as a function thereof. It is often important in reducing noise on transmission line

2. List the application of power amplifier.(May 15, Nov19)

- **Consumer Electronics:** Audio power amplifiers are used in almost all consumer electronic devices ranging from microwave ovens, headphone drivers, televisions, mobile phones and Home theatre systems to theatrical and concert reinforcement systems.
- **Industrial:** Switching type power amplifiers are used for controlling most of the industrial actuator systems like servos and DC motors.
- **Wireless Communication:** High power amplifiers are important in transmission of cellular or FM broadcasting signals to users.

3. Explain difference between voltage and power amplifier.(May 15)

S.No.	Voltage Amplifier	Power Amplifier
1	Transistor chosen should have a high value of beta about 100.	Transistor should have a small value of beta about 20 to 50.

2	The load resistance Rc has a high value about a 1OK ohm.	The load has a small value of 100 to 200 ohm.
3	An input voltage is low approx a few mV.	An input voltage is high about a few volts.
4	Has a low power output and high voltage output.	Has a high power output and a low voltage output.
5	Collector current has low-value 100mA.	Collector current has a high value in power amplifier.
6	Output impedance has a high value.	Output impedance has low value.
7	Usually, R-C coupling is used.	Transformer or tuned circuit is always used.

4. Draw the high frequency model of JFET.(Nov 15)

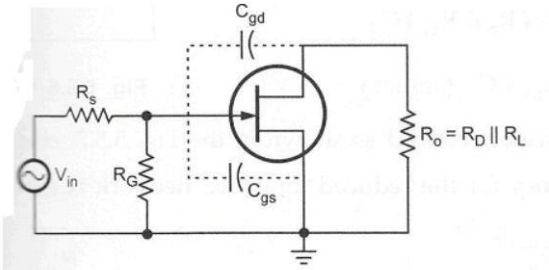


Fig. High frequency equivalent circuit

5. Mention the drawbacks of positive feedback.(Nov 16)

- The stability of circuit will be reduced or decrease with increase in gain.
- The bandwidth also decreases with increase in gain.
- The distortion will also increase.
- The noise will also increase

6. Specify the various types of power amplifier.(Nov 16)

Classification of power amplifier:

- Audio-power amplifiers
- Radio-power amplifiers

Classification According To Mode of Operation:

- Class A Power Amplifiers
- Class B Power Amplifiers
- Class C Power Amplifiers

- Class D Power Amplifiers
- Class AB Power Amplifiers

7. What are the advantages of differential amplifier?(May 16)

1. Differential Amplifier has noise cancellation property.
2. Differential Amplifier can reduce external interference.
3. The nature of these amplifiers is linear.
4. These amplifiers help to increase CMRR(Common Mode Rejection Ratio) which further helps to avoid unwanted signal.

8. What is distortion in power amplifier?(May 16)

Distortion in **Amplifier** basically implies the variation in the waveform received at the output with respect to the applied input. The unwanted alterations generated during **amplification** is known as **distortion**.

9. Write any four application of differential amplifier.(May 17)

- It is used as a series negative feedback circuit by using op amplifier
- Generally, we use differential amplifier that acts as a volume control circuit.
- The differential operational amplifier can be used as an automatic gain control circuit.
- Some of the differential operational amplifier can be used for Amplitude modulation.

10. Mention the effect of cascading single tuned amplifier on bandwidth.(Nov 17)

When a number of identical **double tuned amplifiers** are connected in cascade, the overall **bandwidth** of the system is thereby narrowed and steepness of the sides of the response is increased, just as when **single tuned** stages are **cascaded**.

11. Write about the frequency response of signal turned amplifier.(May 18)

A tuned circuit is capable of amplifying a signal over a narrow band of frequencies that are centered at resonant frequency.

When the reactance of the inductor balances the reactance of the capacitor, in the tuned circuit at some frequency, such a frequency can be called as **resonant frequency**. It is denoted by $\mathbf{f_r}$.

12. What are the effects of negative feedback on the various characteristics of the amplifier.(May 18)

If the open-loop gain, G is very large, then βG will be much greater than 1, so that the overall gain of the system is roughly equal to 1/β. If the open-loop gain decreases due to frequency or the effects of system ageing, providing that βG is still relatively large, the overall system gain does not change very much. So negative feedback tends to reduce the effects of gain change giving what is generally called **"gain stability"**.

13. What are cascade amplifier?(Nov 18)

A cascade amplifier is a two-port network designed with amplifiers which are connected in series when every amplifier transmits its o/p to the second amplifiers input in a daisy chain.

14. Compare gain and frequency.(Nov 18)

The single gain frequency is the frequency at which the gain is 0dB (1x), while the GB product is the product of the gain (unit: times) and frequency. Therefore, ideally the GB product and single gain frequency will be the same value. In an actual opamp, the gain decreases due to the influence of the 2nd pole near 0dB, and as a result the single gain frequency may be lower than the GB product.

15. What are the need for cascading the amplifier?(Nov 19)

cascading amplifiers is the need for an increase in amplifier output to meet a specific requirement, e.g., to increase the signal strength in a Television or radio receiver. Using a cascade, or multistage, amplifier can design a higher current gain or voltage gain devices.

16. Mention the advantages of negative feedback .(Nov 19)

- Less frequency distortion
- Less phase distortion
- Increase **s**tability
- Increase bandwidth
- Decrease noise

17. What are the disadvantages of tuned amplifiers?(May 19)

- The overall circuitry is costly as well as bulky due to the presence of inductors and capacitors in **tuned** circuits.
- **Amplification** in the range of audio frequency cannot be achieved.
- Increase in bandwidth leads to complexity in the circuit.

18. What are the neutralization methods?(May 19)

- It is the process by which feedback can be cancelled by introducing a current that is equal in magnitude but 180o out of phase with the feedback signal at the input of the active device. The two signals will cancel and the effect of feedback will be eliminated. This technique is termed as neutralization methods.
- Types of neutralization are
  - Hazeltine Neutralization
  - Neutralization using coil
  - Rice neutralization
  - Neutrodyne neutralization

19. What are feedback amplifiers?(May 19)

Feedback Amplifier is a device that is based on the principle of **feedback**. The process by which **some part or fraction of output is combined with the input** is known as feedback.

20. Name the types of feedback amplifier.(Nov 18)

- Positive Feedback Amplifier
- Negative Feedback Amplifier
- Voltage Series Feedback Amplifier
- Voltage Shunt Feedback Amplifier
- Current Series Feedback Amplifier
- Current Shunt Feedback Amplifier

11Marks

1. What is differential amplifier. Explain its working in common mode operation. May 14)

Or

Draw a differential amplifier and its equivalent circuit. Derive for Ad and Ac.(Nov 18)

Or

What do you understand by differential amplifier? Draw the circuit diagram and explain the working of differential amplifier. Explain the circuit operation of CM and Dm.(Nov 15)

Or

Draw the circuit diagram of an emitter couple BJT differential amplifier and Derive an expression for differential gain, common mode gain, CMRR input impedance and output impedance. (May 15)

Or

Explain the common mode and difference mode of differential amplifier. (May 16)

A device which accepts an input signal and produces an output signal proportional to the input, is called an amplifier. An amplifier which amplifies the difference between.the two input signals is called differential amplifier.

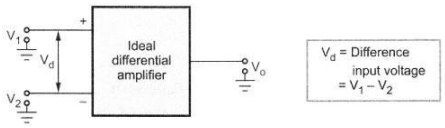


Fig. Ideal differential amplifier

Here V1 and V2 are the two input signals of the Differential amplifier and Vo is the single ended output of Differential amplifier. In an ideal differential amplifier the output voltage Vo is proportional to the difference between two input voltages.

$$\mathbf{Vo \propto (V1 - V2)}$$

$$\mathbf{Vo = A_d\,(V1 - V2)}$$

Differential Gain A_d:

Differential gain is the gain with which amplifier amplifies the difference between two input signals. It is denoted as A_d.

$$\mathbf{Vo = A_d\,(V_d)}$$

Where $V_d$is the voltage difference between two input signals i.e. V_d= V1 – V2

$$\mathbf{A_d = Vo / Vd}$$

Differential gain in dB is given as $\mathbf{A_d(dB) = 20\ \log_{10}\ (Vo / Vd)}$

Common Mode Gain Ac:

If we apply two input voltages which are equal to the differential amplifier then ideally output voltage must be zero. But it is not the case in practical amplifier because output of differential amplifier not only depends on the difference but also depends on the average level of the 2 inputs. Average level of the 2 input signals is called as common mode signal denoted as Vc.

$$\mathbf{Vc = (V1 + V2) / 2}$$

The gain with which differential amplifier amplifies the common mode signal is called as common mode gain.

$$Ac = Vo / Vc$$

$$Vo = A_d V_d + AcVc$$

CMRR (Common Mode Rejection Ratio):

In common mode configuration of differential amplifier many noise signals appear as common input to the both terminals of amplifier. So it better to reject such a common signal.

CMRR is defined as the ability of differential to reject the common mode signal. In other words it is defined as the ratio of differential mode voltage gain A_d to the common mode gain Ac.

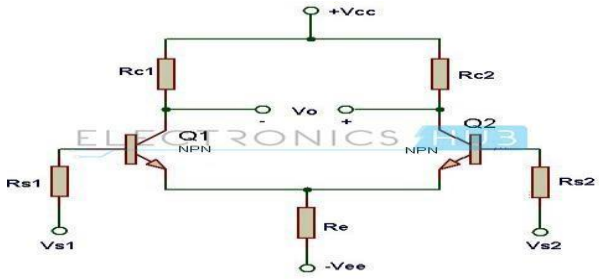
$$CMRR = \rho = A_d / Ac$$

$$Vo = AdVd[1 + (1/CMRR)(Vc/Vd]$$

Transistorized Differential Amplifier:

Differential amplifier basically uses emitter biased circuits which are identical in characteristics. This differential amplifier is also called emitter coupled differential amplifier. The below figure shows the circuit diagram of differential amplifier.

Differential Amplifier Circuit:



Working of Differential Amplifier:

- If input signal is applied to the base of transistor Q1 then there is voltage drop across collector resistor Rc1 so the output of the transistor Q1 is low.
- When there is no input voltage to the transistor Q1, the voltage drop across resistor Rc1 is very less as a result output transistor Q1 is high.
- When transistor Q1 is turned on, the current through the emitter resistor Re increases as emitter current **Ie** is almost equal to the collector current **Ic.**
- As a result voltage drop across resistor Re increases and makes emitter of both transistors positive. In this condition transistor Q2 does not conducts as there is no base voltage.

- As a result collector voltage of transistor Q2 is high. Hence it is clear that the output is produced at the collector of transistor Q2 when an input is applied to the base of Q1.
- Transistors Q1 and Q2 have the exactly same characteristics. The two collector resistors are equal while the 2rwo emitter resistances Re1 and Re2 are also equal.

Rc1 = Rc2 and Re1 = Re2.

The magnitudes of supply voltages +Vcc and -Vee also same. If the input voltages Vs1 and Vs2 are equal then emitter currents Ie1 and Ie2 are also equal.

If Vs1 = Vs2 then Ie1 = Ie2.

$$\mathbf{Ie = Ie1 + Ie2}$$

$$\mathbf{Ve = Vb - Vbe.}$$

Vc1 = Vc2 = Vcc – IcRc assuming collector resistances Rc1 = Rc2 =Rc.

Features of Differential Amplifier:

- Differential voltage gain is high
- Common mode gain is low
- CMRR (common mode rejection ratio) is high
- Input impedance is high
- Wide bandwidth
- Low offset voltages and currents
- Output impedance is low

Advantages of Differential Amplifier:

- Higher verstability
- It has excellent stability
- It contains low noise & low drift

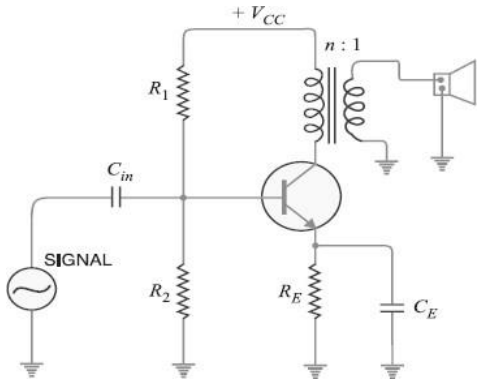
2. Compare the performance & efficiency of class A, class B & class C power amplifier. (Nov14)

Power amplifiers are classified according to their mode of operation i.e the portion of the input cycle during which the collector current is expected to flow. On this basis the power amplifiers are classified as :

1. Class A power amplifier
2. Class B power amplifier
3. Class C power amplifier

Class A Power Amplifier

- If the collector current flows all at all times during the full cycle of the signal, the power amplifier is known as class A power amplifier.
- To achieve this, the power amplifier must be biased in such a way that no part of the signal is cut off.

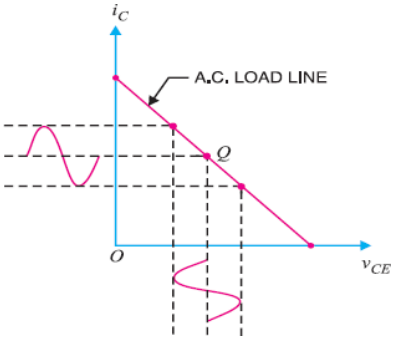


- In case of a direct-coupled class A power amplifier, the current flows through the collector resistive load causes large wastage of dc power in it. As a result this dc power dissipated in the load resistor does not contribute to the useful ac output power.
- Hence, it is generally inadvisable to pass the current through the output device such as in a voice coil of a loudspeaker.
- In a power amplifier circuit shown R_1 and R_2 provide potential divider biasing and emitter resistor R_E is meant for bias stabilization.
- The emitter bypass capacitor C_E is meant for R_E to prevent ac voltage. The input capacitor C_{in} couples ac signal voltage to the base of the transistor but blocks any dc from the previous stage.
- A step-down transformer of suitable turn ratio is provided to couple the high impedance collector circuit to low impedance load.

Impedance Matching

- The power transferred from the power amplifier to the load such as loudspeaker, will be maximum only if the amplifier output impedance equals the load impedance R_L. This is in accordance with the maximum power transfer theorem.
- If we were not able to achieve the above condition, lesser power will be transferred to the load R_L, though the amplifier is capable of delivering more power, and rest of power developed would be lost in the active device.

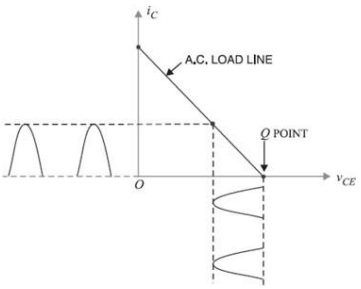
- Hence for transfer of maximum power from amplifier to the output device matching of amplifier output impedance with the impedance of output device is necessary.
- This is accomplished by using a step-down transformer of suitable turn-ratio.



- The operating point Q is so selected that collector current flows at all times throughout the full cycle of the applied signal.
- Since the output wave shape is exactly similar to the input wave shape, hence, such amplifiers have least distortion.
- The only disadvantage of class A power amplifier is the low output power and low collector efficiency.

Class B Power Amplifier

- If the collector current flows only during the positive half-cycle of the input signal, it is called as class B power amplifier.
- In class B power amplifier operation, the transistor is so adjusted that zero signal collector current is zero i.e. no biasing circuit i needed at all.
- During the positive half-cycle of the signal, the input circuit is forward biased and hence collector current flows.
- During the negative half-cycle, the input circuit is reverse biased and no collector current flows.



- The operating point Q is located at collector cut off voltage.In class B amplifier, the negative half-cycle of the signal is cut off and hence severe distortion occurs. However, it provides higher power output and hence collector efficiency.
- These amplifiers are mostly used for power amplification in push-pull arrangement. In such arrangement, two transistors are used in class B operation. One transistor amplifies the positive half cycle of the signal and the other one amplifies the negative half-cycle of the signal.

Class C Power Amplifier

- If the collector current flows for less than half-cycle of the input signal, it is called class C power amplifier.
- In class C power amplifier, the base is negatively biased, so that collector current does not flow just when the positive half-cycle of the signal starts.
- Such amplifiers are never used for power amplification but as tuned amplifier i.e. to amplify a narrow band of frequencies near the resonant frequency.

Performance Quantities of Power Amplifier

The performance quantities or criteria for a power amplifier are:

1. Collector Efficiency
2. Distortion
3. Power Dissipation Capability

(i) Collector Efficiency

- The main criterion for a power amplifier is not the power gain but the maximum a.c. power output.
- An amplifier converts d.c. power from supply into a.c. power output. Hence, the effectiveness of a power amplifier is measured in terms of its ability to convert d.c. power from supply to a.c. output power. This is called as collector efficiency.
- The collector efficiency is defined as the ratio of output power to the zero signal power or d.c. power supplied by the battery.

Expression for collector efficiency

Collector efficiency,

$$\eta = \frac{\text{a.c. power output}}{\text{d.c. power input}}$$

$$= \frac{P_o}{P_{dc}}$$

Where,

$$P_{dc} = V_{CC} I_C$$

$$P_o = V_{ce} I_c$$

Where Vce is the r.m.s. value of signal output voltage and Ic is the r.m.s. value of output signal current.

In terms of peak-to-peak values, the a.c. power output can be expressed as :

$$P_o = [(0.5 \times 0.707) v_{ce\,(p-p)}][(0.5 \times 0.707) i_{c\,(p-p)}]$$

$$= \frac{v_{ce(p-p)} \times i_{c(p-p)}}{8}$$

$$\therefore \quad \text{Collector } \eta = \frac{v_{ce\,(p-p)} \times i_{c(p-p)}}{8\, V_{CC}\, I_C}$$

(ii) Distortion

The change of output wave shape from the input wave shape of an amplifier is known as distortion.

(iii) Power Dissipation Capability

The ability of a power transistor to dissipate heat is known as power dissipation capability.

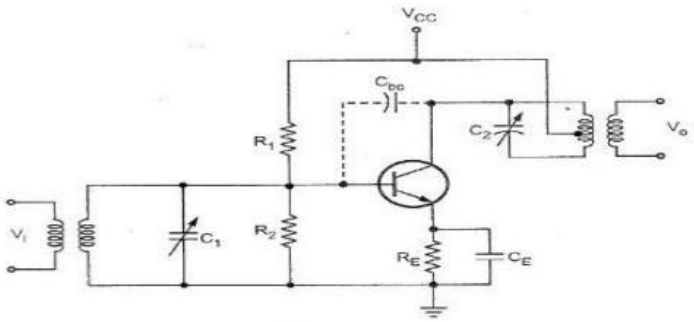
3.Explain the different types of neutralization techniques used in tuning amplifier(May 19, May 15, Nov 16)

(Or)

Elaborate about any two neutralization techniques (Nov 18)

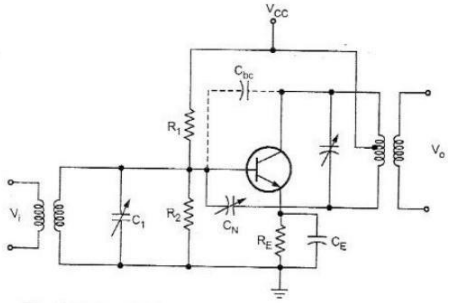
- In tuned RF amplifiers, transistor are used at the frequencies nearer to their unity gain bandwidths (i.e. fT), to amplify a narrow band of high frequencies centred around a ratio frequency.
- At this frequency, the inter junction capacitance between base and collector, Cbc of the transistor becomes dominant, i.e., its reactance between low enough to be considered, which is otherwise infinite to be neglected as open circuit. Being CE configuration capacitance Cbe come across input and output circuits of an amplifier.

- As reactance of Cbc at RF is low enough it provide the feedback path from collector to base. With this circuit condition, if some feedback signal manages to reach the input from output in a positive manner with proper phase shift, then there is possibility of circuit converted to a positive manner with proper phase shift, then there is possibility of circuit converted to an unstable one, generating its own oscillations and can stop working as an amplifier.
- This circuit will always oscillate if enough energy is fed back from the collector to the base in the correct phase to overcome circuit losses. Unfortunately, the conditions for best gain and selectivity are also those which promote oscillation.
- In order to prevent oscillations in tuned RF amplifiers it was necessary to reduce the stage gain to a level that ensured circuit stability.
- This could be accomplished in several ways such as lowering the Q of tune circuits; stager tuning, losse coupling between the stages or inserting a „loser" element into the circuit.



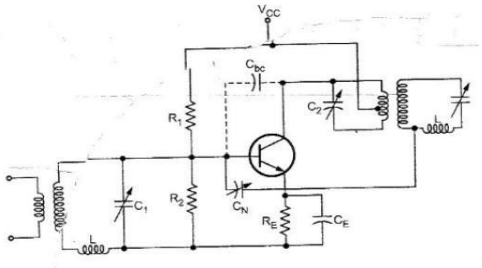
Hazeltine Neutralization

- In this circuit a small value of variable capacitance CN is connected from the bottom of coil, point B, to the base.
- The internal capacitance Cbc, shown dotted, feeds a signal from the top end of the coil, point A, to the transistor base and the CN feeds a signal o equal magnitude but opposite polarity rom the bottom o coil, point B, to the base.
- The neutralizing capacitor, CN can be adjusted correctly to completely nulliy the signal ed through the Cbc.



Neutralization using coil

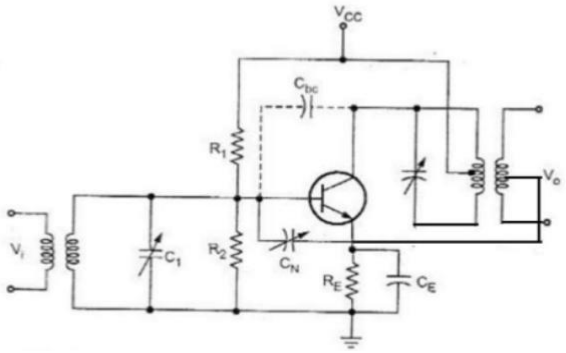
The Fig. 3.38 shows the neutralization o RF amplifier using coil. In this circuit, L part of the tuned circuit at the base o next stage is oriented or minimum coupling to the other winding. It is wound on a separate from and is mounted at right angle to the coupled windings. If the windings are properly polarized, the voltage across L due to the circulating current in the base circuit will have the proper phase to cancel the signal coupled through the base to collector, Cbc capacitance.



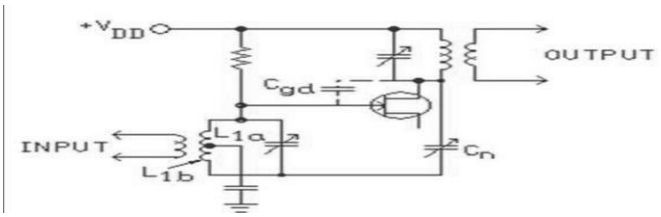
Neutrodyne neutralization:

The Neutrodyne was a particular type of tuned radio frequency radio receiver, in which the instability-causing inter-electrode capacitance of the triode RF tubes is cancelled out or "neutralized". In most designs, a small extra winding on each of the RF amplifiers' tuned anode coils was used to generate a small antiphase signal, which could be adjusted by special variable trim capacitors to cancel out the stray signal coupled to the grid via plate-to-grid capacitance.

The design also neutralized the stranglehold that RCA then held on the commercial radio industry. Compared to the technically superior Superheterodyne the Neutrodyne was cheaper to build. Also, as basically a TRF receiver, it was also considered easier for non-technical owners to use than the early superhets. To properly set up a Neutrodyne receiver, not only did the circuitry need to be aligned for peak performance, it also had to be neutralized



Rice neutralization is a well-known. method of **neutralizing** the effect of grid plate inter-electrode capacity in an unbalanced R.F. amplifier



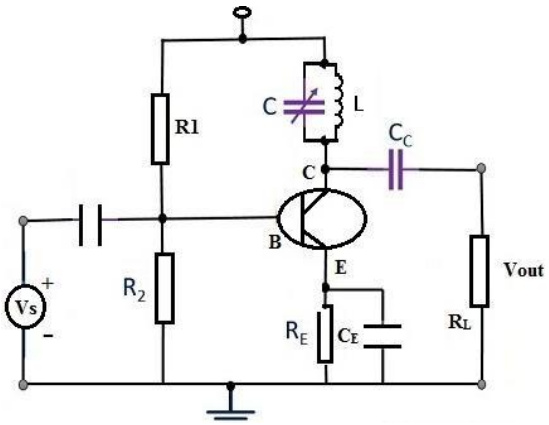
4. Explain single tuned voltage amplifier and discuss their frequency of oscillation. (Or)

With neat sketch explain the construction and working single tuned amplifier also derive the frequency response of the same. (Or) With circuit diagram give the operation of single tuned amplifier. Give its limitation. (May 16, May 17, May 18)

The single tuned amplifier is a multistage amplifier, which uses a parallel tuned circuit like a load. But, the LC circuit and tuned circuit in every stage are necessary to be selected to the same frequencies. The configuration used in this amplifier is CE amplifier configurations which contain the parallel tuned circuit. In wireless communication, the RF stage requires a tuned voltage amplifier to choose the preferred carrier frequency as well as to change the passband signal which is allowed.

Construction

The single tuned amplifier circuit diagram using capacitive coupling is shown below. It is important to notice that for an LC circuit, the value of inductance (L) and capacitance (C) should be chosen that the resonance frequency of resonance must be equal to the frequency signal which is applied.



circuit-diagram-of-single-tuned-amplifier

The output of this circuit can be attained by using inductive and capacitive coupling. But, this circuit uses capacitive coupling. The common emitter capacitor used within the circuit can be a bypass capacitor while the circuits like stabilization & biasing follow by these resistors like R1, R2, and RE The LC circuit used within the collector region acts likes a load. The capacitor is changeable in order to contain a changeable resonant frequency. Huge signal amplification can be attained if the input signal frequency is comparable to the resonance frequency of the tuned circuit.

Single Tuned Amplifier Operation

The single tuned amplifier operation mainly starts with the high-frequency signal application which can be improved at the transistor‟s BE terminal shown in the above circuit. By changing the capacitor used within the LC circuit, the circuit‟s resonant frequency is made equal to the given input signal‟s frequency.

Here, the higher impedance can be given to the frequency of the signal through the LC circuit. Therefore, a huge o/p can be attained. For an i/p signal with various frequencies, simply the frequency communicates with resonant frequency so that it will get amplified. Whereas other types of frequencies will discard the tuned circuit.

Therefore, merely the preferred frequency signal will be selected & therefore this can be amplified through the LC circuit.

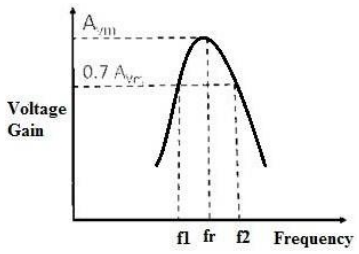
Voltage Gain and Frequency Response

The voltage gain for the LC circuit can be given by the following equation.

$$\mathbf{Av = \beta\ Rac/rin}$$

Here Rac is the LC circuit‟s impedance (Rac = L/CR), so the above equation will become

The frequency response of this amplifier is shown below.



Frequency-response-of-single-tuned-amplifier

We know that the circuit‟s impedance is extremely high & completely resistive within nature at the resonance frequency.

As a result, the utmost voltage is attained across RL for an LC circuit at the frequency of resonant.

The tuned amplifier bandwidth is given below.

$$\mathbf{BW = f2\text{-}f1 => fr/Q}$$

Here, the amplifier amplifies any frequency in this range.

Cascading Effect

Basically, cascading of several stages within a tuned amplifier can be done for enhancing the overall system gain. As the entire system gain is the outcome of the product‟s gain for every stage within the amplifier.

In a tuned amplifier, when the voltage gain increases, then the bandwidth will decrease. So let‟s have a look at how the cascading will affect the entire system‟s bandwidth.

Consider an n-stages cascade connection in a single tuned amplifier. The amplifier‟s relative gain is equivalent to the system‟s gain at the resonant frequency can be represented with the following equation

$$\mathbf{|A/A\ resonance| = 1/\sqrt{1 + (2\square\ Qe)^2}}$$

In the above equation, Qe denotes an efficient quality factor

δ denotes fractional differences within the frequency.

The overall gain can be obtained by merging the gain of numerous stages in the tuned amplifier

$$\mathbf{|A/A\ resonance| = [1/\sqrt{1 + (2\square\ Qe)^2}]^n = 1/[1 + (2\square\ Qe)^2]n/2}$$

By comparing the total gain to $1/\sqrt{2}$ then we can terminate the 3dB frequencies to this amplifier.

Therefore we will have

$$\mathbf{1/[\sqrt{1 + (2\square Qe)^2}]^n = 1/\sqrt{2}}$$

The above equation can be written as

$$1 + (2 Qe)^2 = 2^{1/n}$$

From the above equation

$$2 Qe = + or – \sqrt{21/n} -1$$

It is a fractional difference within frequency, so it can be written like the following.

$$ = \omega – \omega r/ \omega r = f – fr/fr$$

Substitute this into the above equation so we can get

$$2 (f – fr/fr) Qe = + or – \sqrt{2^{1/n}} -1$$

$$2 (f – fr) Qe = + or – fr\sqrt{2^{1/n}} -1$$

$$f – fr = +fr / 2Qe \sqrt{2^{1/n}} -1$$

Now, $f2 – fr = + fr/2Qe \sqrt{2^{1/n}} -1$ and $fr-f1 = + fr/2Qe \sqrt{2^{1/n}} -1$

The amplifier‟s BW using number of cascaded stages can be written as

$$B12 = f2 –f1 = (f2 – fr) + (fr-f1)$$

Substitute the values in the above equation we can get the following equation.

$$B12 = f2 –f1 = fr/2Qe \sqrt{2^{1/n}} -1 + fr/2Qe \sqrt{2^{1/n}} -1$$

From the above equation

$$B12 = 2fr/2Qe \sqrt{2^{1/n}} -1 = > fr/Qe \sqrt{2^{1/n}} -1$$

$$B1 = fr/Qe$$

$$B12 = B1 fr/Qe \sqrt{2^{1/n}} -1$$

From the above B12 equation, we can conclude that basically n-stages BW is equal to the sum of a factor & single stage BW.

If the digit of stages can be two, then

$$\sqrt{2^{1/n}} -1 = \sqrt{2^{1/2}} -1 = 0.643$$

If the digit of stages can be three, then

$$\sqrt{2^{1/n}} -1 = \sqrt{2^{1/3}} -1 = 051$$

Therefore, from the above information, it is understandable that when the number of stages increases then BW will be decreased.

Advantages

- The power loss is less due to the lack of collector resistance**.**
- Selectivity is high.
- The voltage supply of the collector is small due to the lack of Rc.

Disadvantages.

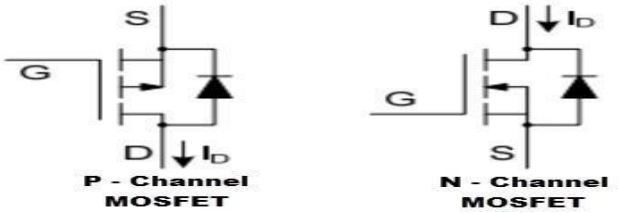
- The product of gain bandwidth is small

Applications of Single Tuned Amplifier

- This amplifier is used in the primary internal stage of the radio receiver wherever the selection of the front end can be done using an RF amplifier.
- This amplifier can be used in television circuits.

5. Describe the working of the power MOSFET with characteristics.(May 19)

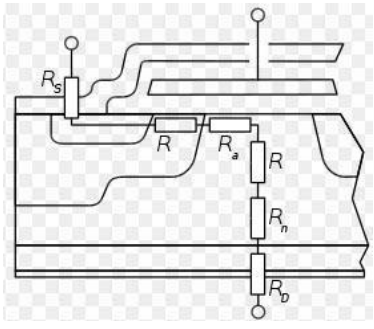
A power MOSFET is a special type of metal oxide semiconductor field effect transistor. It is specially designed to handle high-level powers. The power MOSFET‟s are constructed in a V configuration. Therefore, it is also called as V-MOSFET, VFET. The symbols of N-channel & P- channel power MOSFET are shown



The Power MOSFET is a type of MOSFET. The operating principle of power MOSFET is similar to the general MOSFET. The power MOSFETS are very special to handle the high level of powers. It shows the high switching speed and by comparing with the normal MOSFET, the power MOSFET will work better. The power MOSFETs is widely used in the n-channel enhancement mode, p-channel enhancement mode, and in the nature of n-channel depletion mode.

On State Resistance

If the power MOSFET is in ON sate, then it produces the resistive behavior in-between the drain & source terminals. The RS resistance is the source resistance. It will show all resistance between the source terminals of the package to the channel of the MOSFET.



On State Resistance

The Rch resistance is the channel resistance and this resistance is inversely proportional to the channel width & for a given die size, to the channel density. This resistance is very

important contributors to the RDSon of the low voltage MOSFET. The intensive work has done to reduce their cell size with respect to increase the channel density.

The access resistance is represented by the Ra. The access resistance shows the resistance of the epitaxial zone directly to the gate electrode. The current direction is changed from the channel to the vertical.

RJFET is the detrimental effect of the cell size reduction. The P implantation is observed from the gate of a parasitic JFET transistor and it has reduced the width of the current flow.

Rn represents the epitaxial layer and it is used for sustaining the blocking voltage. This resistance is directly related to the voltage rating of the device. The high voltage MOSFET requires a thick low dependent layer which is highly resistive and a low voltage transistor requires a thin layer with the higher doping layer which is very less resistive. This is the main factor for the resistance of high voltage MOSFET.

The RD resistance is the equivalent of resistance of the RS for the drain. The RD resistance, represent the transistor substrate and the package connections.

Break Down Voltage

The power MOSFET is equivalent to the PIN diode, if it is in the OFF state and it is initiated by the P+ diffusion, the N- epitaxial layer and the N+ substrate. This structure is reverse biased when it is highly nonsymmetrical structure and the space charge region extends principally to the lightly doped side, which is the N- layers.

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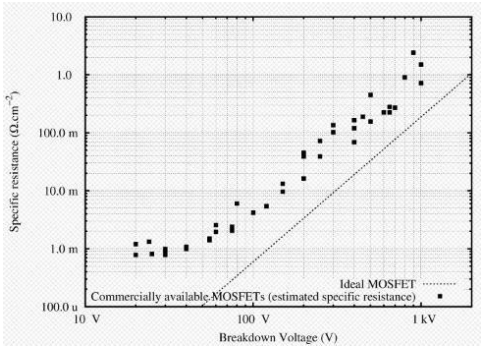
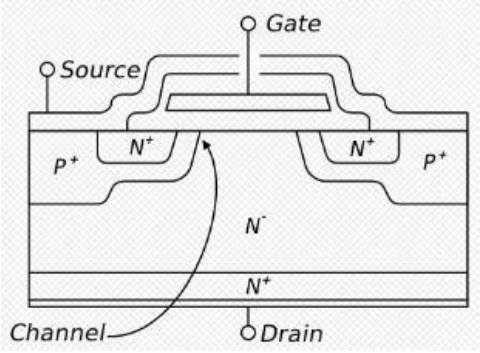


Break Down Voltage

There are two important parameters to run both the breakdown voltage and the RDSon of the transistor, which is the doping level and the thickness of the N- epitaxial layer. If the layer is thicker, it has low doping level and the breakdown voltage is high. Similarly, thicker the layer, it has the high doping level and the radon is low.

Body Diode

The body diode can be seen in the following figure that the source metallization is connected to both the N+ and P implantations. Even though the basic principle of the MOSFET requires only that the source should be connected to the N+ zone. Thus, this would result in a floating P zone between the N-doped source and drain. It is equivalent to an NPN transistor with a nonconnected base. Under some conditions like high drain current, in the order of the same volts of an on-state drain to source voltage, this parasitic transistor of NPN should be triggered and make the MOSFET uncontrollable.



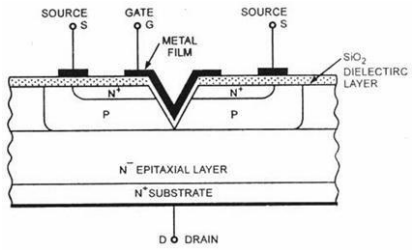
Body Diode

The connections of the P implantation to the source metallization short the base terminal of the transistor parasitic to its emitter and it prevents the latching. Hence this solution creates a diode between the cathode & anode of the MOSFET and the current blocks in one direction.

For inductive loads, the body diodes utilize the freewheeling diodes in the configuration of H Bridge & half bridge.

Working of Power MOSFET and Characteristics

The construction of the power MOSFET is in V-configurations, as we can see in the following figure. Thus the device is also called as the V-MOSFET or V-FET. The V- the shape of power MOSFET is cut to penetrate from the device surface is almost to the N+ substrate to the N+, P, and N – layers. The N+ layer is the heavily doped layer with a low resistive material and the N- layer is a lightly doped layer with the high resistance region.

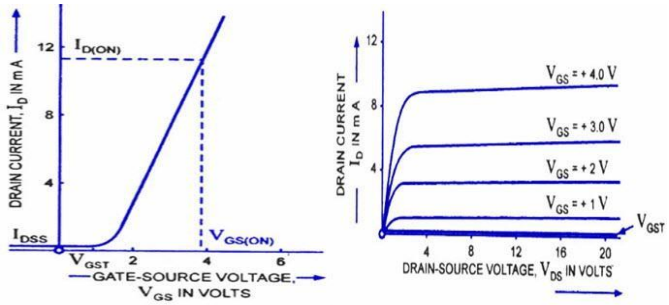


N – Channel Power MOSFET

Both the horizontal and the V cut surface are covered by the silicon dioxide dielectric layer and the insulated gate metal film is deposited on the SiO2 in the V shape. The source terminal contacts with the both N+ and P- layers through the SiO2 layer. The drain terminal of this device is N+.

The V-MOSFET is an E-mode FET and there is no exists of the channel in between the drain & source till the gate is positive with respect to the source. If we consider the gate is positive with respect to the source, then there is a formation of the N-type channel which is close to the gate and it is in the case of the E-MOSFET. In the case of E-MOSFET, the N-type channel provides the vertical path for the charge carriers. To flow between the drain and source terminals. If the VGS is zero or negative, then there is no channel of presence and the drain current is zero.

If there is an increase in the gate voltage then the channel resistance is reduced, therefore the drain current ID is increased. Hence the drain current ID is controlled by the gate voltage control. So that for a given level of VGS, ID is remaining constant through a wide range of VDS levels.



Transfer & Drain characteristics

- The channel length of the power MOSFET is in the diffusion process, but in the MOSFET the channel length is in the dimensions of the photographic masks employed in the diffusion process. By controlling the doping density and diffusion time, the channel length will become shorter. The shorter channels will give, the more current densities which will contribute again to larger power dissipation. It also allows a larger transconductance gm to be attained in the V-FET.
- In the geometry of power MOSFET, there is an important factor which is the presence of lightly doped, N- epitaxial layer which is close to the N+ substrate. If the VGS is at zero or negative, then the drain is positive with respect to the source and there is a reverse biased between the P- layer & N- layer. At the junction the

depletion region penetrates into the N- layer, therefore it punch-through the drain to the source are avoided. Hence, relatively high VDS are applied without any danger of device breakdown.

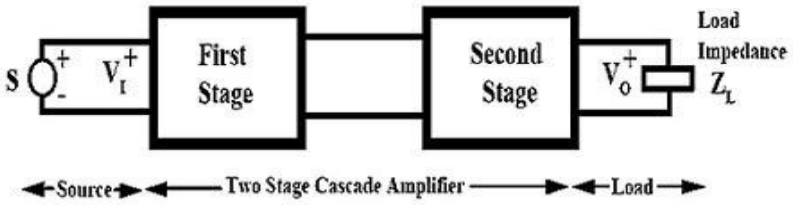
- ❖ In the power MOSFET, there is available of P-channel. The characteristics are similar to the N-channel MOSFET. The direction of the current and voltage polarities are in reverse direction..

Applications of Power MOSFET

- Low voltage motor controllers
- DC to DC converters
- These are widely used in the low voltage switches which are less than the 200V

6.With neat sketch explain two stage cascade amplifier and derive its voltage gain, current gain, input impedance and output impedance.(Nov 19)

A cascade amplifier is a two-port network designed with amplifiers which are connected in series when every amplifier transmits its o/p to the second amplifiers input in a daisy chain. The problem in measuring the gain of the cascaded stage is the non-perfect coupling among two stages because of loading. The two stages of cascaded CE (common-emitter) are shown in the following circuit. Here the voltage divider can be formed by using the input and output resistances of the first and next stage. The complete gain cannot be the result of the individual stages.



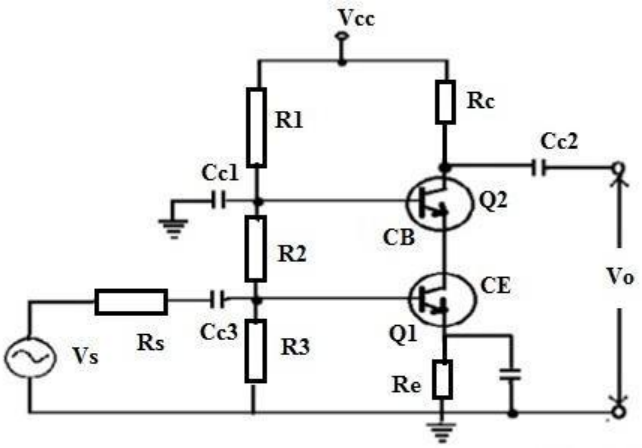
This amplifier is used to enhance the strength of a signal in a TV receiver. In this amplifier, the primary stage of the amplifier can be connected to the secondary stage of the amplifier. To build a practical electronic system, a single-stage amplifier is not enough.

Even though the amplifier‟s gain mainly depends on parameters of the device as well as components of the circuit, there exists a higher limit of gain which can be attained from a single-stage amplifier. Therefore, the gain of this amplifier cannot be sufficient in practical application.

To conquer this trouble, we require this amplifier‟s two or more stages to amplify the overall amplifier‟s voltage gain. As above one stage is used within series it is named as a multi-stage amplifier. The main drawback of the cascade amplifier is when several stages increases then the bandwidth will decrease.

Cascade Amplifier Circuit

The circuit diagram of cascade amplifier is shown below. The circuit can be designed with two configurations of a transistor namely CE (common-emitter) and CB (common base). The CB (common base) configuration provides a good high-frequency operation.



The current gain, as well as the i/p resistance of the cascade arrangement, is equivalent to the related value of a common emitter single-stage amplifier. The o/p resistance can be equivalent to the common base configuration. The miller‟s capacitor shunting the common emitter input stage is extremely small.

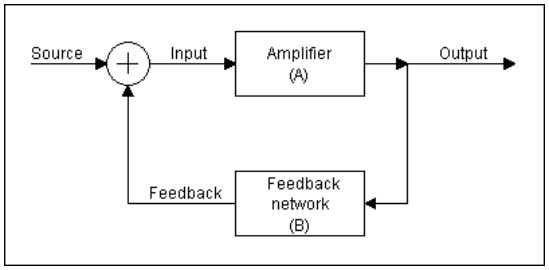
Applications

- This amplifier is used in tuned RF amplifiers within television circuits.
- This amplifier can also be used as a wideband amplifier.
- The isolation offered among input & output with these amplifiers is extremely high.

Thus, this is all about the cascade amplifier analysis. The configuration of this amplifier mainly include some advantages like less input resistance, moderate to high current gain, voltage as well as high o/p resistance. The main drawback of the cascade amplifier is when several stages increases then the bandwidth will decrease

7. Explain the concept of negative feedback in amplifier. Derive the expression for voltage gain, input impedance and output impedance. (Nov 15)

The feedback in which the feedback energy i.e., either voltage or current is out of phase with the input and thus opposes it, is called as **negative feedback**.



In negative feedback, the amplifier introduces a phase shift of 180° into the circuit while the feedback network is so designed that it produces no phase shift or zero phase shift. Thus the resultant feedback voltage V_f is 180° out of phase with the input signal V_{in}.

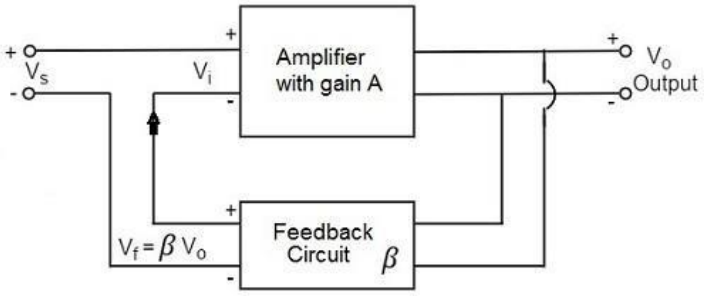
Though the **gain** of negative feedback amplifier is **reduced**, there are many advantages of negative feedback such as

- Stability of gain is improved
- Reduction in distortion
- Reduction in noise
- Increase in input impedance
- Decrease in output impedance
- Increase in the range of uniform application

It is because of these advantages negative feedback is frequently employed in amplifiers.

Principle of Feedback Amplifier:

A feedback amplifier generally consists of two parts. They are the amplifier and the feedback circuit. The feedback circuit usually consists of resistors. The concept of feedback amplifier can be understood from the following figure



In the above figure, the gain of the amplifier is represented as **A**. The gain of the amplifier is the ratio of output voltage **Vo** to the input voltage **Vi** . The feedback network extracts a voltage **Vf = β** Vo from the output **Vo** of the amplifier.

This voltage is subtracted for negative feedback, from the signal voltage Vs . Now,

$$\mathbf{Vi=Vs-Vf=Vs-\beta Vo}$$

The quantity $\boldsymbol{\beta = Vf / Vo}$ is called as feedback ratio or feedback fraction.

The output **Vo** must be equal to the input voltage **(Vs - βVo)** multiplied by the gain **A** of the amplifier. Hence,

$$\mathbf{(Vs-\beta Vo)A=Vo}$$

$$\mathbf{AVs-A\beta Vo=Vo}$$

$$\mathbf{AVs=Vo(1+A\beta)}$$

$$\mathbf{Vo/Vs=A/(1+A\beta)}$$

Therefore, the gain of the amplifier with feedback is given by

$$\mathbf{Af=A/(1+A\beta)}$$

Effect of negative feedback on amplifier performance:

The effect of negative feedback on an amplifier is considered in relation to gain, gain stability, distortion, noise, input/output impedance and bandwidth and gain-bandwidth product.

Gain:

The gain of the amplifier with feedback is given by

$$\mathbf{Af=A/(1+A\beta)}$$

Hence, gain decreases with feedback.

Gain Stability:

An important advantage of negative voltage feedback is that the resultant gain of the amplifier can be made independent of transistor parameters or the supply voltage variations,

$$\mathbf{Af=A/(1+A\beta)}$$

For negative voltage feedback in an amplifier to be effective, the designer deliberately makes the product **Aβ** much greater than unity. Therefore, in the above relation, „1“ can be neglected as compared to **Aβ** and the expression becomes

$$\mathbf{Af = A/(1+A\beta) = 1/\beta}$$

It may be seen that the gain now depends only upon feedback fraction, **β**, i.e., on the characteristics of feedback circuit. As feedback circuit is usually a voltage divider (a resistive network), therefore, it is unaffected by changes in temperature, variations in transistor parameters and frequency. Hence, the gain of the amplifier is extremely stable.

Distortion:

A power amplifier will have non-linear distortion because of large signal variations. The negative feedback reduces the nonlinear distortion. It can be proved mathematically that:

$$\mathbf{Df = D/(1+A\beta)}$$

Where D = distortion in amplifier without feedback

Df = distortion in amplifier with negative feedback

It is clear that by applying negative feedback, the distortion is reduced by a factor **(1+Aβ)**

Noise :

There are numbers of sources of noise in an amplifier. The noise **N** can be reduced by the factor of **(1+Aβ),** in a similar manner to non-linear distortion, so that the noise with feedback is given by

$$\mathbf{Nf = N/(1+A\beta)}$$

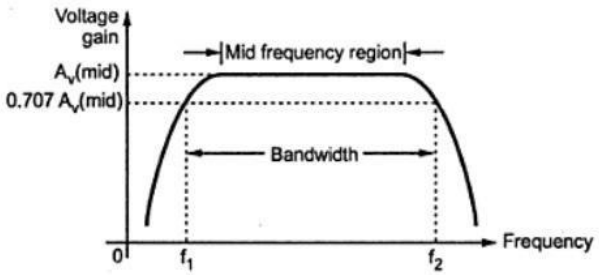
However, if it is necessary to increase the gain to its original level by the addition of another stage, it is quite possible that the overall system will be noisier that it was at the start. If the increase in gain can be accomplished by the adjustment of circuit parameters, a definite reduction in noise will result from the use of negative feedback.

Input / Output Impedance :

The input and output impedances will also improve by a factor of **(1+Aβ),** based on feedback connection type.

Bandwidth and Gain-bandwidth Product:

Bandwidth and Gain-bandwidth Product



$$\mathbf{f\,hf = f\,h\,(1+A\beta)}$$

$$\mathbf{f\,lf = f\,l\,/(1+A\beta}$$

Each of higher and lower cut-off frequencies will improve by a factor of **(1+Aβ).** However, gain-bandwidth product remains constant) An important piece of information that can be obtained from a frequency response curve is the bandwidth of the amplifier. This refers to the „band" of frequencies for which the amplifier has a useful gain. Outside

this useful band, the gain of the amplifier is considered to be insufficient compared with the gain at the centre of the bandwidth.

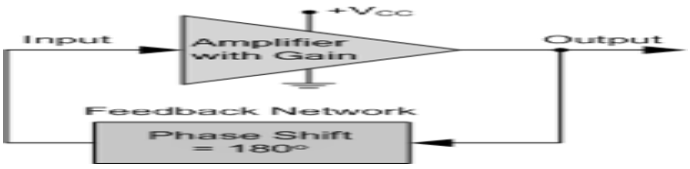
The bandwidth specified for the voltage amplifiers is the range of frequencies for which the amplifiers gain is greater than 0.707 of the maximum gain Alternatively, decibels are used to indicate gain, the ratio of output to input voltage. The useful bandwidth would be described as extending to those frequencies at which the gain is -3db down compared to the gain at the mid-band frequency.

8. Draw the frequency oscillation and the minimum gain required to sustained oscillation of the RC phase shift oscillation.(Nov 16)

RC Oscillators use a combination of an amplifier and an RC feedback network to produce output oscillations due to the phase shift between the stages

In the amplifier tutorials we saw that a single stage transistor amplifier can produce 180^o of phase shift between its output and input signals when connected as a common-emitter type amplifier and that its output signal across the collector load depends entirely on the input signal injected into the transistors base terminal.

For an RC oscillator to sustain its oscillations indefinitely, sufficient feedback of the correct phase, that is positive Feedback must be provided along with the voltage gain of the single transistor amplifier being used to inject adequate loop gain into the closed-loop circuit in order to maintain oscillations allowing it to oscillates continuously at the selected frequency.

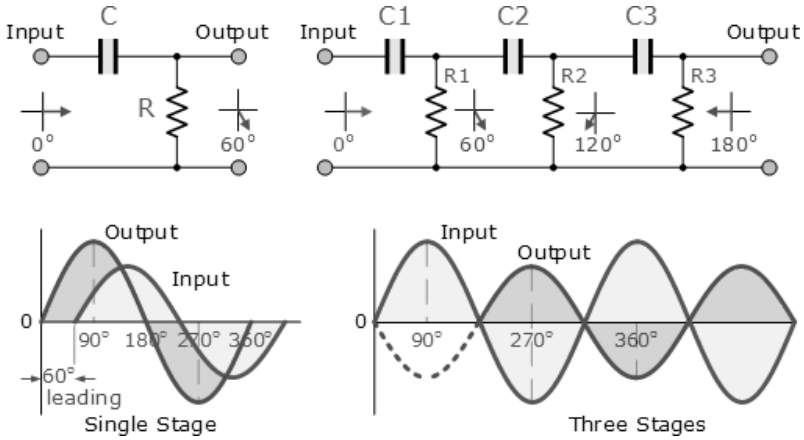


In an **RC Oscillator** circuit the input is shifted 180^o through the feedback circuit returning the signal out-of-phase and 180^o again through an inverting amplifier stage to produces the required positive feedback. This then gives us "$180^o + 180^o = 360^o$" of phase shift which is effectively the same as 0^o, thereby giving us the required positive feedback. In other words, the total phase shift of the feedback loop should be "0" or any multiple of 360^o to obtain the same effect.

In a **Resistance-Capacitance Oscillator** or simply known as an **RC Oscillator**, we can make use of the fact that a phase shift occurs between the input to a RC network and the

output from the same network by using interconnected RC elements in the feedback branch.

RC Phase-Shift Network



The circuit on the left shows a single resistor-capacitor network whose output voltage "leads" the input voltage by some angle less than 90º. In a pure or ideal single-pole RC network. it would produce a maximum phase shift of exactly 90º, and because 180º of phase shift is required for oscillation, at least two single-poles networks must be used within an *RC oscillator* design.

However in reality it is difficult to obtain exactly 90º of phase shift for each RC stage so we must therefore use more RC stages cascaded together to obtain the required value at the oscillation frequency. The amount of actual phase shift in the circuit depends upon the values of the resistor (R) and the capacitor (C), at the chosen frequency of oscillations with the phase angle (φ) being given as:

RC Phase Angle

$$X_C = \frac{1}{2\pi f C} \qquad R = R,$$

$$Z = \sqrt{R^2 + (X_C)^2}$$

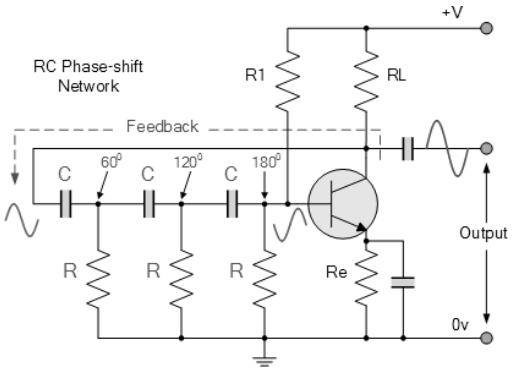
$$\therefore \quad \phi = \tan^{-1} \frac{X_C}{R}$$

Where: X_C is the Capacitive Reactance of the capacitor, R is the Resistance of the resistor, and f is the Frequency.

In our simple example above, the values of R and C have been chosen so that at the required frequency the output voltage leads the input voltage by an angle of about 60º.

Then the phase angle between each successive RC section increases by another 60º giving a phase difference between the input and output of 180º (3 x 60º) .

Basic RC Oscillator Circuit



The basic **RC Oscillator** which is also known as a **Phase-shift Oscillator**, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor (RC) ladder network. This regenerative feedback from the RC network is due to the ability of the capacitor to store an electric charge, (similar to the LC tank circuit).

This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360º.

By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor because capacitive reactance (X_C) changes with a change in frequency as capacitors are frequency-sensitive components. However, it may be required to re-adjust the voltage gain of the amplifier for the new frequency.

If the three resistors, R are equal in value, that is $R_1 = R_2 = R_3$, and the capacitors, C in the phase shift network are also equal in value, $C_1 = C_2 = C_3$, then the frequency of oscillations produced by the RC oscillator is simply given as:

$$f_r = \frac{1}{2\pi RC\sqrt{2N}}$$

Where:

- f_r is the oscillators output frequency in Hertz
- R is the feedback resistance in Ohms
- C is the feddback capacitance in Farads
- N is the number of RC feedback stages.

This is the frequency at which the phase shift circuit oscillates. In our simple example above, the number of stages is given as three, so N = 3 ($\sqrt{2*3} = \sqrt{6}$). For a four stage RC network, N = 4 ($\sqrt{2*4} = \sqrt{8}$), etc.

Since the resistor-capacitor combination in the **RC Oscillator** ladder network also acts as an attenuator, that is the signal reduces by some amount as it passes through each passive stage. It could be assumed that the three phase shift sections are independent of each other but this is not the case as the total accumulative feedback attenuation becomes -1/29th ($Vo/Vi = \beta = -1/29$) across all three stages. Thus the voltage gain of the amplifier must be sufficiently high enough to overcome these passive RC losses. Clearly then in order to produce a total loop gain of -1, in our three stage RC network above, the amplifier gain must be equal too, or greater than, 29 to compensate for the attenuation of the RC network.

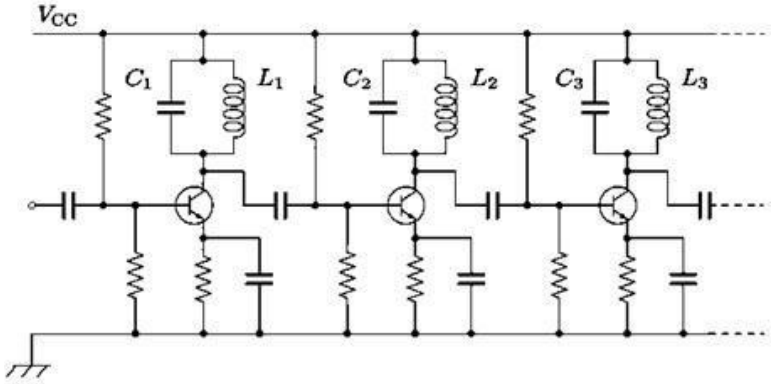
The loading effect of the amplifier on the feedback network has an effect on the frequency of oscillations and can cause the oscillator frequency to be up to 25% higher than calculated. Then the feedback network should be driven from a high impedance output source and fed into a low impedance load such as a common emitter transistor amplifier but better still is to use an Operational Amplifier as it satisfies these conditions perfectly.

9.With neat diagram explain the operation of stagger tuned amplifier. (May 18)

Staggered tuned amplifier definition is an amplifier that is used to improve the total frequency response of the tuned amplifier. Usually, these amplifiers are designed to exhibit an overall response for maximal flatness in the region of the center frequency. This amplifier uses tuned circuits to operate in union. The total frequency response of this amplifier can be achieved by adding up the separate response as one. When the different tuned circuit‟s resonant frequencies are staggered otherwise displaced, then it is known as a stagger tuned amplifier.

Stagger Tuned Amplifier Working

The circuit diagram shown below is a two-stage stagger tuned amplifier. In this circuit, the stagger tuning can be achieved by producing the tuned circuits like L1C1 and L2C2 to a little different frequency. The stagger tuned amplifier circuit is shown below.

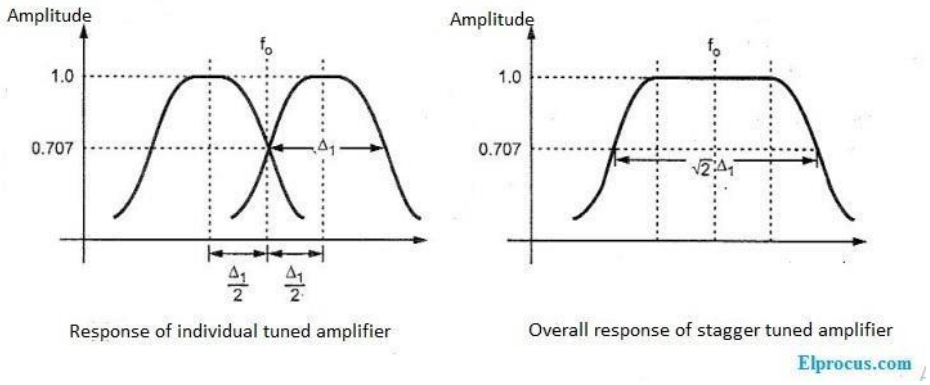


stagger-tuned-amplifier

The double-tuned amplifier offers high BW like 3dB. However, the arrangement of this amplifier is not easy. So to conquer this difficulty two single tuned cascaded amplifiers are employed which have certain bandwidth. The resonant frequencies of BWs are adjusted and divided through an amount equivalent to the BW of every stage.

As these frequencies are staggered and called as stagger tuned amplifiers. The following image shows the main relationship between individual stages amplification characteristics within a stagger tuned amplifier.

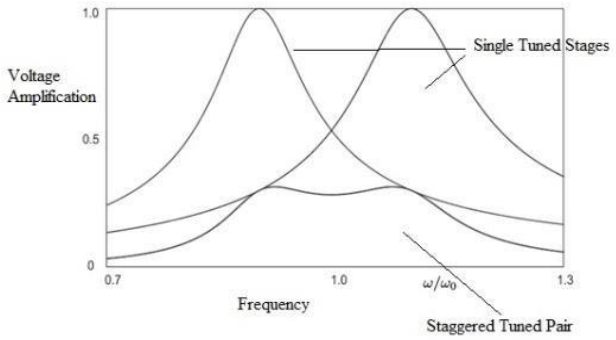
The amplifier using stagger tuning has greater BW, faster passband and number of stages used. The flatter will be the passband. The circuit is called stagger because the tuned circuit‟s resonance frequencies are displaced.



stagger-tuned-amplifier-output-response

The stagger tuned amplifier‟s total frequency response is contrasted with the equivalent and separate single tuned stages. These stages include similar resonant circuits. In the following characteristics, the staggering decrease in the total amplification of the middle frequency to 0.5 of the crest amplification of the separation stage. At middle frequency, every stage includes 0.707 crest amplification of the separation stage. Therefore, the

corresponding voltage amplification for each stage of the stagger will be 0.707 times higher when the two similar stages are utilized without staggering.



stagger-tuned-amplifier-characteristics

the 3dB BW of the stagger pair is √2 times higher than the BW of an individual single tuned stage. Therefore the corresponding gain BW product for each stage of stagger tuned pair can be 0.707 x √2 is equal to 1.00 times with the separate single tuned stages.

The thought of stagger tuned can be simply expanded to additional stages. In 3 -stage staggering, the tuning of the primary circuit can be adjusted to a lower frequency than the center frequency. The 3rd circuit can be adjusted to high frequency compared with middle frequency. The tuned frequency which is in middle is adjusted at the precise center frequency.

Stagger Tuned Amplifier Derivation

Av/Av (resonance) = 1/ 1+2jQeff δ

= 1/1+jX

Where X = 2Qeff δ

Assume that, if one stage of the amplifier is tuned with the frequency like fr + δ and another stage of the amplifier is tuned with the frequency like fr – δ. Thus we have fr1 = fr + δ and fr2 = fr – δ.

Based on the above two frequencies fr1 and fr2, the selectivity function can be written as

Av/Av (resonance)1 = 1/ j(X+1)

Av/Av (resonance)2 = 1/ j(X-1)

The total gain of these stages is equal to the product of two stages of individual gains

Av/Av (resonance) cascaded = Av/Av (resonance)1 * Av/Av (resonance)2

= 1/ j(X+1) * 1/ j(X-1)

= 1/ 2+2jX-X2 = 1/ (2-X2) + 2jX

|Av/Av (resonance) cascaded| = 1/√ (2-X2)2 + (2jX) 2

= 1/√ (4-4X2+X4+4X2) = 1/√4+X4

We know the value of X = 2Qeff δ

Substitute this value in the above equation.

= 1/√4+(2Qeff δ)4

= 1/√4+16Q4eff δ 4 = 1/2√1+4Q4eff δ 4

Advantages and Disadvantages

- By using this amplifier an increased BW can be obtained. Compare with a single tune, the BW is √2 times.
- This amplifier has a high value of gain BW.
- In every stage of the amplifier, there is a small difference within the resonance. Therefore, enhanced stability within an operation can be obtained.
- The bandpass of this amplifier is faster compare with a single tuned amplifier. The alignment of this circuit is easy when we compare it with the single tuned amplifier.

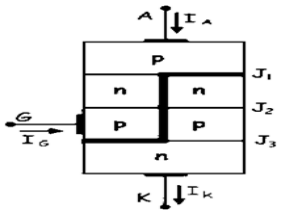
Applications

- The stagger tuned amplifier applications include the following.
- It is used in a superheterodyne receiver as an IF (intermediate frequency) amplifier
- It is used in UHF radio relay systems.
- It is extremely narrow-band intermediate frequency amplifier within a spectrum analyzer

10.Explain the two transistor equivalent of SCR. (May 17)

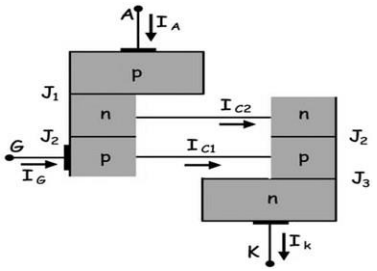
Two Transistor Model of SCR or Thyristor

Basic operating principle of SCR, can easily be understood by the **two transistor model of SCR**, as it is a combination of p and n layers.

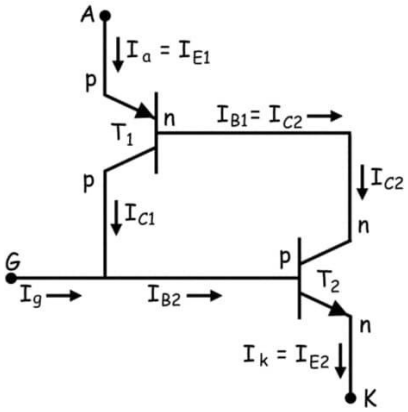


This is a pnpn thyristor. If we bisect it through the dotted line then we will get two transistors i.e. one pnp transistor with J_1 and J_2 junctions and another is with J_2 and J_3

junctions .



The relation between the collector current and emitter current is shown below



Here, I_C is collector current, I_E is emitter current, I_{CBO} is forward leakage current, α is common base forward current gain and relationship between I_C and I_B is

$$I_C = \beta I_B$$

Where, I_B is base current and β is common emitter forward current gain. Let‟s for transistor T_1 this relation holds

$$I_{C1} = \alpha_1 I_a + I_{CBO1} \ldots\ldots (i)$$

And that for transistor T_2

$$I_{C2} = \alpha_2 I_k + I_{CBO2} \ldots\ldots (ii) \; again \; I_{C2} = \beta_2 I_{B2}$$

Now, by the analysis of two transistors model we can get anode current,

$$I_a = I_{C1} + I_{C2} \; [applying \; KCL]$$

From equation (i) and (ii), we get,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 I_k + I_{CBO2} \ldots\ldots (iii)$$

If applied gate current is I_g then cathode current will be the summation of anode current and gate current i.e.

$$I_k = I_a + I_g$$

By substituting this valyue of I_k in (iii) we get,

$$I_a = \alpha_1 I_a + I_{CBO1} + \alpha_2 (I_a + I_g) + I_{CBO2}$$

$$I_a = \frac{\alpha_2 I_g + I_{CBO1} + I_{CBO2}}{1 - (\alpha_1 + \alpha_2)}$$

From this relation we can assure that with increasing the value of $(\alpha_1 + \alpha_2)$towards unity, corresponding anode current will increase.

At the first stage when we apply a gate current I_g, it acts as base current of T_2 transistor i.e. $I_{B2} = I_g$ and emitter current of the T_2 transistor $I_{E2} = I_k$. Hence establishment of the emitter current gives rise α_2 as

$$\alpha_2 = \frac{I_{CBO1}}{I_g}$$

Presence of base current will generate collector current as

$$I_{C2} = \beta_2 \times I_{B2} = \beta_2 I_g$$

I_{C2} is nothing but base current I_{B1} of transistor T_1, which will cause the flow of collector current,

$$I_{C2} = \beta_1 \times I_{B1} = \beta_1 \beta_2 I_g$$

I_{C1} and I_{B1} lead to increase I_{C1} as

$$I_a = I_{C1} + I_{B1}$$

and hence, α_1 increases. Now, new base current of T_2 is

$$I_g + I_{C1} = (1 + \beta_1 \beta_2) I_g,$$

which will lead to increase emitter current

$$I_k = I_g + I_{C1}$$

and as a result α_2 also increases and this further increases

$$I_{C2} = \beta_2 (1 + \beta_1 \beta_2) I_g .$$

$$I_{B1} = I_{C2} ,$$

α_1 again increases. This continuous positive feedback effect increases $(\alpha_1 + \alpha_2)$towards unity and anode current tends to flow at a very large value. The value current then can only be controlled by external resistance of the circuit.

Application of SCRs

- SCRs are mainly used in devices where the control of high power, possibly coupled with high voltage, is demanded. Their operation makes them suitable for use in medium to high-voltage AC power control applications, such as lamp dimming, regulators and motor control.
- SCRs and similar devices are used for rectification of high power AC in high-voltage direct current power transmission.

ELECTRONICS DEVICES AND CIRCUITS BMT33

UNIT - II TRANSISTORS

2 Marks

1. What is thermal runaway? (April/ May 2015)

- The power loss in transistor is primarily at the collector junction because the voltage there is high compared to the low voltage at the forward biased emitter junction.
- If collector current increases, the power developed tends to raise the junction temperature.
- This causes an increase in β and α further increase in collector current in temperature may occur resulting in "thermal run away."

2. Define pinch off voltage? (Dec 2017)

As the reverse bias is further increased, the effective width of the channel decreases, the depletion region or the space charge region widens, reaching further into the channel and restricting the passage of electrons from the source to drain. Finally at a certain gate to source voltage VGS = VP.

3. Why transistor (BJT) is called current controlled device? (April/ May 2018)

Output voltage, current or power is controlled by the input current in transistor. So, it is called the current controlled device.

4. What are the characteristics features of BJT? (Nov 2014)

CHARACTERISTICS	COMMON BASE	COMMON COLLECTOR
Phase shift	0°	0°
Voltage gain	High	Low
Current gain	Low	High
Power gain	Low	Medium

5. What is intrinsic standoff ratio? (Nov 2014, April/May 2016)

- Intrinsic standoff ratio is the ratio of the standoff voltage to the power supply voltage.
- The standoff voltage is the voltage needed to fire e unijunction transistor's emitter.
- The intrinsic standoff voltage is also defined as the ratio of the RB1 (base resistance 1) and the interbase resistance.

6. Difference between JFET and MOSFET. (April/May 2015)

JFET(Junction Gate Field- Oxide Effect transistor)	**MOSFET(Metal Oxide - semiconductor field Effect Transistor)**
It is a three-terminal semiconductor device.	It is a four-terminal semiconductor device.
It can only operates in the depletion mode.	It operates in both depletion mode and enhancement mode.
It is relatively cheaper than Mosfet.	It is expensive one.
JFETs is simple.	MOSFETs is complex.

7. Among CB, CE, CC, which is popular why? (Nov 2015)

• CE is most widely used because it provides the voltage gain required for most of the day to day applications of preamp and power amps. This is not possible in CB mode. Moreover, the CC has the avatar of CE as in Emitter Follower, This circuit also closely resemble a Common Emitter, and its work is to provide current gain.

• Common emitter is the most basic configuration for amplifier circuits. It also provide the maximum transconductance or voltage gain for a given load.

• The common emitter configuration has the highest power gain combined with medium voltage and current gain.

8. What are the disadvantages of FET when compared to BJT? (Nov 2015)

• It has relatively lower gain-bandwidth product compare to BJT.

• Transconductance is low and hence voltage gain is low.

• FET has slower switching times compare to BJT. The internal junction capacitance of FET is responsible for high delay times.

9. What are the disadvantages of JFET when compared to BJT? (Nov 2016)

• BJT is a bipolar device hence it has noise due to storage of minority carriers, while JFET is a majority carrier device hence less prone to noise.

• FET works in concept of field effect which is different from the concept of BJT hence they all have common advantage of high i/p impedance and low power consumption and they don't suffer from thermal runaway.

10. What is current application factor in transister? (Nov 2016)

The ratio of change in emitter current (ΔIE) to the change in base current (ΔIB) is known as Current Amplification factor in common collector (CC) configuration. It is denoted by γ.

$$\gamma = \Delta IE / \Delta IB$$

- The current gain in CC configuration is same as in CE configuration.
- The voltage gain in CC configuration is always less than 1.

11. What are the advantages of CE transistor? (Nov 2017)

The advantages of a common emitter amplifier include the following.

- The common emitter amplifier has a low input impedance and it is an inverting amplifier
- The output impedance of this amplifier is high
- This amplifier has the highest power gain when combined with medium voltage and current gain
- The current gain of the common emitter amplifier is high

12. Why transister consume power while it act as switch? (April/May 2018)

One of the most fundamental applications of a transistor is using it to control the flow of power to another part of the circuit - using it as an electric switch. Driving it in either cutoff or saturation mode, the transistor can create the binary on/off effect of a switch.

13. What are the application of UJT? (Nov/Dec 2018)

- The UJT is used in timing circuit.
- The uni-junction transistor (UJT) used as relaxation oscillator.
- It is used as voltage detector.
- The UJT is used for switching.
- It is widely used as triggering device for silicon control rectifier (SCR) and TRIAC.

14. What is Biasing? (Nov/Dec 2019)

• Biasing is the method of establishing predetermined voltages or currents at various points of an electronic circuit for the purpose of establishing proper operating conditions in electronic components.

• The AC signal applied to them is superposed on this DC bias current or voltage.

• Other types of devices, for example magnetic recording heads, require a time varying signal as bias.

• The operating point of a device, also known as bias point, quiescent point, or Q-point, is the steady state voltage or current at a specified terminal of an active device with no input signal applied.

15. Difference between enhancement and depletion type MOSFET. (Nov/Dec 2019)

S. No	**Depletion type MOSFET(D- MOSFET)**	**Enhancement type MOSFET(E-MOSFET)**
1.	It is called a depletion MOSFET because of channel depletion.	It only works in enhancement mode and is therefore called Enhancement MOSFET

2.	It can be used as E-MOSFET	It cannot be used as a D-MOSFET
3.	If Vgs=0v, Ids flows due to Vds	If Vgs=0v , Ids=0, although Vds

16. Why is collection region is greater than emitter region? (May 2019)

The collector region is the largest of all regions because it must dissipate more heat than the emitter or base regions. It is designed to be large because in order to dissipate all the heater, the extra surface area allows it to do so.

17. What are the 2 modes of MOSFET? (May 2019)

There are two classes of MOSFETs. There is depletion mode and there is enhancement mode. Each class is available as n- or a p-channel, giving a total of four types of MOSFETS. Depletion mode comes in an N or a P and an enhancement mode comes in an N or a P.

11 MARKS

1. (A) Explain the input and output characteristics of a common emitter configuration with a neat sketch? (Nov 2014) (or)

(B) Explain the input and output characteristics of a common emitter configuration. comparison b/w CE, CC, configuration. (Nov 2016) (or)

(C) Explain the input and output characteristics of BJT in common emitter configuration?

(April/May 2015, May 2019)

Common-Emitter Configuration:

- It is called common-emitter configuration since emitter is common or reference to both input and output terminals.emitter is usually the terminal closest to or at ground potential.
- Almost amplifier design is using connection of CE due to the high gain for current and voltage.

- Two set of characteristics are necessary to describe the behavior for CE; input (base terminal) and output (collector terminal) parameters. Proper Biasing common-emitter configuration in active region.

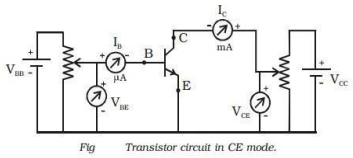


Fig Transistor circuit in CE mode.

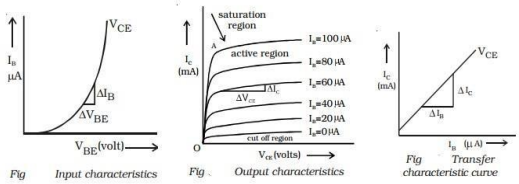
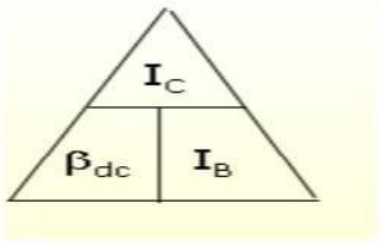


Fig Input characteristics Fig Output characteristics Fig Transfer characteristic curve

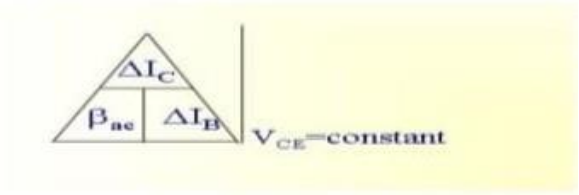
CE Configuration

Beta (β) or amplification factor:

The ratio of dc collector current (IC) to the dc base current (IB) is dc beta (βdc) which is dc current gain where IC and IB are determined at a particular operating point, Q-point (quiescent point). It's define by the following equation: 30 < βdc < 300 ◊ 2N3904 On data sheet, βdc=hfe with h is derived from ac hybrid equivalent cct. FE are derived from forwardcurrent amplification and common-emitter configuration respectively.



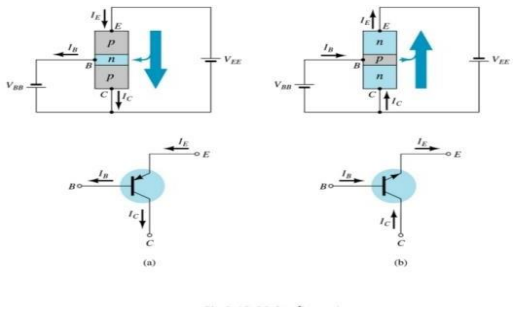
For ac conditions, an ac beta has been defined as the changes of collector current (IC) compared to the changes of base current (IB) where IC and IB are determined at operating point.



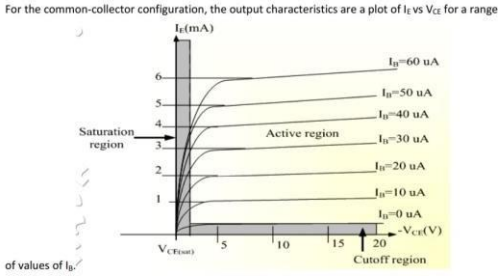
Common - Collector Configuration:

- It is called common-emitter configuration since both the signal source and the load share the collector terminal as a common connection point.
- The output voltage is obtained at emitter terminal. The input characteristic of common-collector configuration is similar with common-emitter.

Common-collector circuit configuration is provided with the load resistor connected from emitter to ground. It is used primarily for impedance matching purpose since it has high input impedance and low output impedance.



For the common-collector configuration, the output characteristics are a plot of le vs Vce for a range of values of Ig.



Output of common-collector

2. A) Explain negative resistance of UJT with neat sketch (Nov 2014, April/May 2016) (Or)

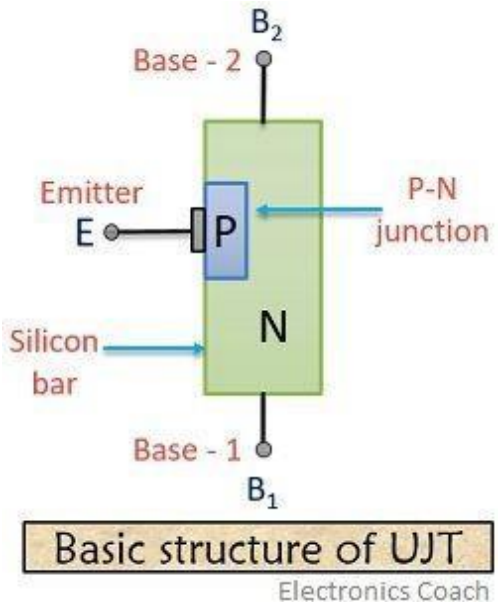
B) Explain construction, equivalent and operation of UJT (May 2017, April /May 2018)

Definition: Uni-junction Transistor is a semiconductor switching device having 2 layers and 3 terminals and is abbreviated as UJT.

- It is called so because of the presence of only one junction. It has the ability to limit large power with a small input signal and is also known as a double base diode.
- UJT is a device that possesses negative resistance characteristic that means its emitter current rises regeneratively when triggered.
- Thus an emitter supply is needed in order to restrict it. In normal operating conditions, it generally absorbs less power and hence is an efficient device.
- As it is a low-cost device, hence it is widely used in circuits such as oscillators, triggers and pulse generators etc.
- It is to be noted that UJT possesses dissimilar switching characteristics from that of the BJT or FET.

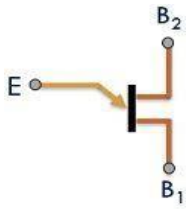
Constructional details of Unijunction transistor

The figure below shows the basic structure of a Unijunction transistor,

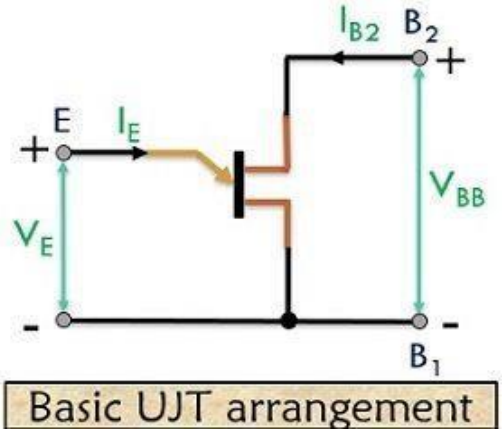


Its structure is almost similar to an N-channel JFET. UJT consists of a lightly doped N-type silicon bar in which a P-type material is diffused thus producing PN junction. Due to the existence of a single PN junction, it is termed as a Unijunction device.

It consists of two ohmic contacts at the end of the bar which is labelled as base 1 (B1) and base 2 (B2). Here, as we can see in the figure above, the structure is not symmetrical as the emitter region is closer to B2 in order to have the optimum electrical characteristic.



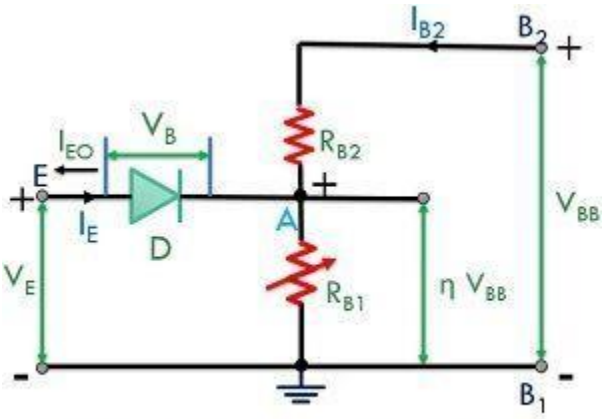
Now, let us have a look at the basic arrangement of a UJT,



In order to form a complementary UJT, an N-type material is diffused on a P-type bar. A complementary UJT differs from a conventional UJT only by the polarities of current and voltage as the other characteristics of the two are similar.

Working of Unijunction transistor:

Let's now consider an equivalent circuit of UJT shown below:



Equivalent circuit of UJT

Here, RB1 is variable resistance, due to variation in the resistance with changes in emitter current.

The two resistor of the circuit together constitutes the total resistance which is the resistance between B2 and B1 where the emitter is kept open is known as Interbase resistance RBB.

So, we can write,

$$RBB = RB1 + RB2$$

where emitter terminal is kept open.

Normally the value of RB1 is greater than that of RB2.

When a voltage VBB is applied between the two base terminal B1 and B2, the voltage at point A will be,

$$V_A = V_{BB} \, X \, \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

$$VA = \eta \, VBB$$

Here, η is termed as an intrinsic standoff ratio and is given by,

$$\eta = \frac{R_{B_1}}{R_{B_1} + R_{B_2}}$$

Now, let's discuss the above-stated condition in detail.

Consider a condition when there is no emitter potential supplied to the circuit. In such a case the diode gets reverse biased. Thus, including the barrier potential of the diode, the total reverse biased voltage will become,

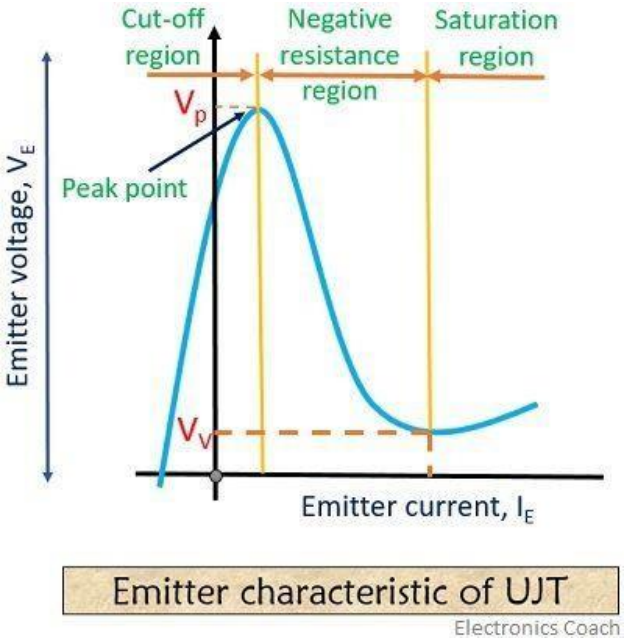
$$VA + VB = \eta VBB + VB$$

As we have considered a silicon bar so in that case the value of VB will be 0.7 V.

If the emitter potential that was previously 0, is increased by a small value and it becomes equal to ηVBB. It will cause the emitter current IE to become 0. This prevents no current to flow through the diode because of equal voltage level.

Characteristics of Unijunction transistor:

The figure below shows the characteristic of UJT, it derives the relationship between VE and IE.



As we can see in the figure, IE does not exceed IEo, which is nothing but equivalent to the leakage current in the reverse direction of BJT. However, it is noteworthy that the above-stated condition is for emitter voltage that lies in the left direction towards the peak point. The region is known as the cut-off region.

As we have already discussed that conduction starts when emitter potential becomes equal to peak voltage. After this emitter potential reduces on, any further increase in IE that simply shows a reduction in RB1.

This is the reason why the device is said to possess negative resistance characteristic and the region is called negative resistance region.

After this, a valley point is reached, where the device comes to saturation region with any additional increase in the emitter current of the device.

Special features of UJT:

- It is a low-cost device.
- UJT is a device with a high pulse current capability.
- It possesses negative resistance characteristic and is a device that absorbs less power during operation.

Applications of UJT:

- UJT is a device that is used in thyristor triggering.
- It is used in controlling of DC voltage, in the case of overvoltage detection and measurement of magnetic flux.
- UJTs are used in relaxation oscillator circuitry.
- The negative resistance characteristic of a Unijunction transistor is the basis for its operation and due to this, the device can be used as an oscillator.

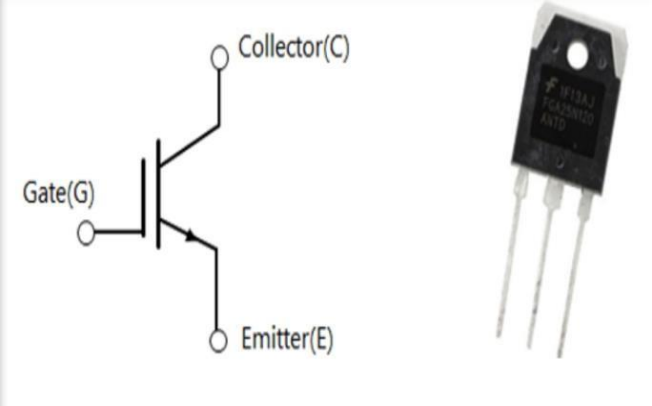
3. Explain construction and working of IGBT with neat sketch (April/May 2015, Nov/Dec 2017)

IGBT

- IGBT is the short form of Insulated Gate Bipolar Transistor.
- It is a three-terminal semiconductor switching device that can be used for fast switching with high efficiency in many types of electronic devices.

➢ These devices are mostly used in amplifiers for switching processing complex wave patters with pulse width modulation (PWM).

➢ The typical symbol of IGBT along with its image is shown below.

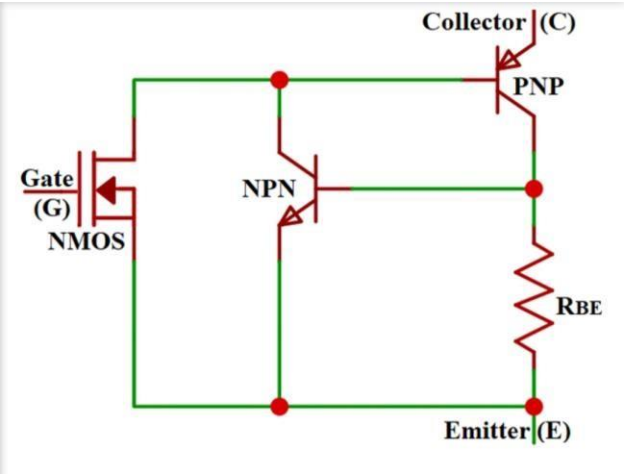


Internal Structure of IGBT

➢ IGBT can be constructed with the equivalent circuit that consists of two transistors and MOSFET, as the IGBT posses the output of the below combination of the PNP transistor, NPN transistor, and MOSFET.

➢ IGBT combines the low saturation voltage of a transistor with the high input impedance and switching speed of a MOSFET.

➢ The outcome obtained from this combination delivers the output switching and conduction characteristics of a bipolar transistor, but the voltage is controlled like a MOSFET.



➢ Since IGBT is the combination of MOSFET and BJT they are also called by different names.

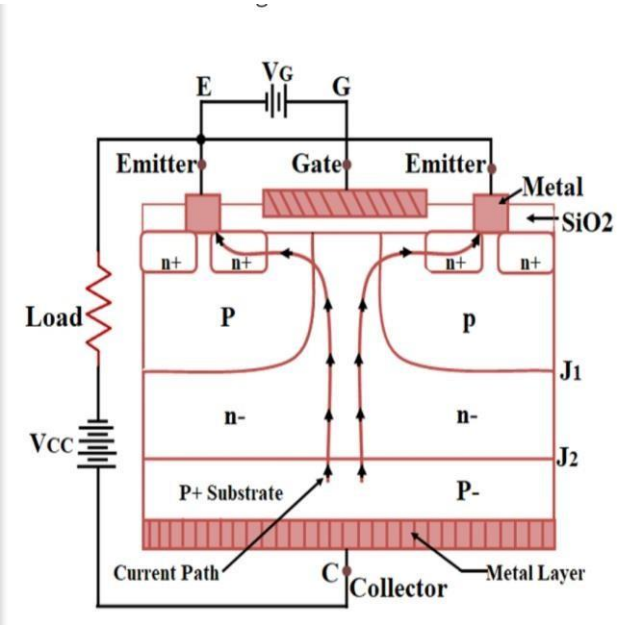
➢ The different names of IGBT are Insulated Gate Transistor (IGT), Metal Oxide Insulated Gate Transistor (MOSIGT), Gain Modulated Field Effect Transistor (GEMFET), Conductively Modulated Field Effect Transistor (COMFET).

Working of IGBT

➢ IGBT has three terminals attached to three different metal layers, the metal layer of the gate terminal is insulated from the semiconductors by a layer of silicon dioxide (SiO2).

➢ IGBT is constructed with 4 layers of semiconductor sandwiched together. The layer closer to the collector is the p+ substrate layer above that is the n- layer, another player is kept closer to the emitter and inside the player, we have the n+ layers.

➢ The junction between the p+ layer and n- layer is called the junction J2 and the junction between the n- layer and the p layer is called the junction J1. The structure of IGBT is shown in the figure below.



To understand the working of the IGBT, consider a voltage source VG connected positively to the Gate terminal with respect to the Emitter.

Consider other voltage source Vcc connected across The Emitter and the Collector, where Collector is kept positive with respect to the Emitter. Due to the voltage source Vcc the junction

J1 will be forward-biased whereas the junction J2 will be reverse biased. Since J2 is in reverse bias there will not be any current flow inside the IGBT(from collector to emitter).

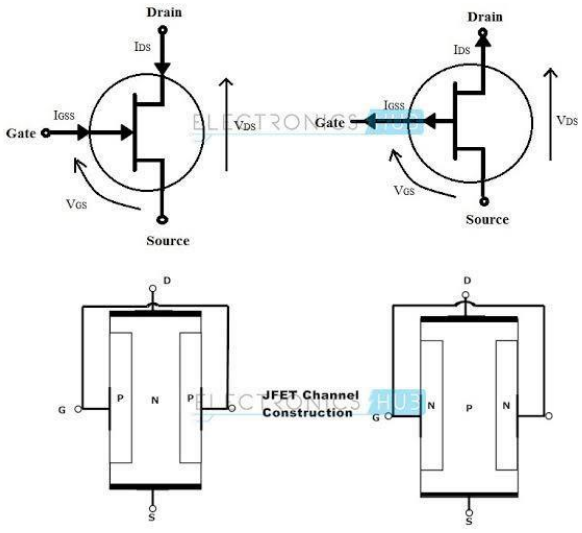
Initially, consider that there is no voltage applied to the Gate terminal, at this stage the IGBT will be in a non conductive state. Now if we increase the applied gate, due to the capacitance effect on the SiO2 layer the negative ions will get accumulated on the upper side of the layer and the positive ions will get accumulated on the lower side of the SiO2 layer.

This will cause the insertion of negative charge carriers in the p region, higher the applied voltage VG greater the insertion of negatively charged carriers. This will lead to a formation of the channel between the J2 junction which allows the flow of current from collector to emitter. The flow of current is represented as the current path in the picture, when the applied Gate voltage VG increases the amount of current flow from the collector to the emitter also increases.

4 A) Explain operation of JFET and its drain and transfer characteristics. (Nov 2015, April/May 2016, May 2017)

B) Explain n channel JFET and write its transfer characteristics (Nov/Dec 2017, April/May 2018, Nov/Dec 2018)

If the gate is an N-type material, the channel must be a P-type material.



Construction of N-Channel and P-Channell JFET

A piece of N- type material, referred to as channel has two smaller pieces of P-type material attached to its sides, forming PN junctions. The channel ends are designated as the drain and source. And the two pieces of P-type material are connected together and their terminal is called the gate. Since this channel is in the N-type bar, the FET is known as N-channel JFET.

Operation Of N-Channel JFET:

The overall operation of the JFET is based on varying the width of the channel to control the drain current. A piece of N type material referred to as the channel, has two smaller pieces of P type material attached to its sites, farming PN –Junctions. The channel's ends are designated the drain and the source. And the two pieces of P type material are connected together and their terminal is called the gate.

With the gate terminal not connected and the potential applied positive at the drain negative at the source a drain current Id flows. When the gate is biased negative with respective to the source the PN junctions are reverse biased and depletion regions are formed.

The channel is more lightly doped than the P type gate blocks, so the depletion regions penetrate deeply into the channel. Since depletion region is a region depleted of charge carriers it behaves as an Insulator. The result is that the channel is narrowed. Its resistance is increased and Id is reduced. When the negative gate bias voltage is further increased, the depletion regions meet at the center and Id is cut off completely.

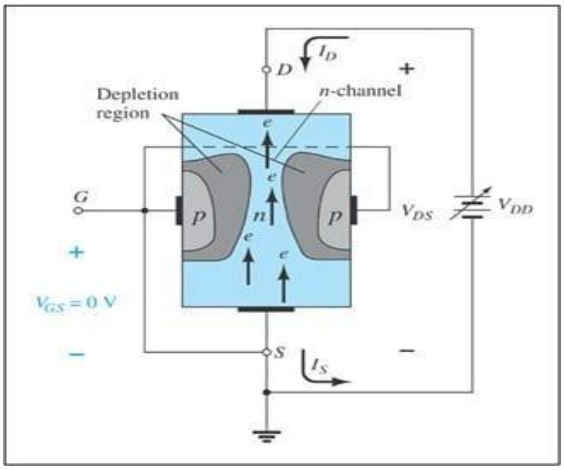
There are two ways to control the channel width

- By varying the value of Vgs
- And by Varying the value of Vds holding Vgs constant.

1. By varying the value of Vgs :-

We can vary the width of the channel and in turn vary the amount of drain current. This can be done by varying the value of Vgs. This point is illustrated in the fig below. Here we are dealing with N channel FET. So channel is of N type and gate is of P type that constitutes a PN junction. This PN junction is always reverse biased in JFET operation .The reverse bias is applied by a

battery voltage Vgs connected between the gate and the source terminal i.e positive terminal of the battery is connected to the source and negative terminal to gate.



1) When a PN junction is reverse biased the electrons and holes diffuse across junction by leaving immobile ions on the N and P sides, the region containing these immobile ions is known as depletion regions.

2) If both P and N regions are heavily doped then the depletion region extends symmetrically on both sides.

3) But in N channel FET P region is heavily doped than N type thus depletion region extends more in N region than P region.

4) So when no Vds is applied the depletion region is symmetrical and the conductivity becomes Zero. Since there are no mobile carriers in the junction

5) As the reverse bias voltage is increases the thickness of the depletion region also increases. i.e. the effective channel width decreases.

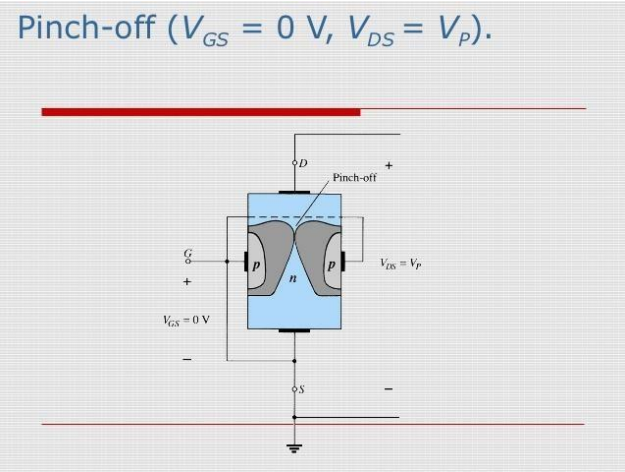
6) By varying the value of Vgs we can vary the width of the channel.

2. By Varying the value of Vds holding Vgs constant :

1) When no voltage is applied to the gate i.e. Vgs=0, Vds is applied between source and drain the electrons will flow from source to drain through the channel constituting drain current id.

2) With Vgs=0 for Id= 0 the channel between the gate junctions is entirely open In response to a small applied voltage Vds, the entire bar acts as a simple semi conductor resistor and the current Id increases linearly with Vds.

3) The channel resistances are represented as rd and rs as shown in the fig.



4) This increasing drain current Id produces a voltage drop across rd which reverse biases the gate to source junction (rd> rs). Thus the depletion region is formed which is not symmetrical

5) The depletion region i.e. developed penetrates deeper into the channel near drain and less towards source because Vrd >> Vrs. So reverse bias is higher near drain than at source.

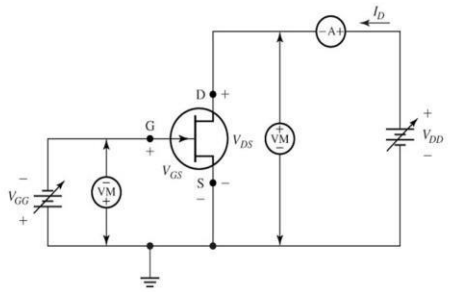
6) As a result growing depletion region reduces the effective width of the channel. Eventually a voltage Vds is reached at which the channel is pinched off.

Experimental Setup To Plot JFET:

This is the voltage where the current Id begins to level off and approach a constant value. So, by varying the value of Vds we can vary the width of the channel holding Vgs constant.

When both Vgs and Vds is applied:

Circuit that can be used to measure N-channel JFET characteristics.



It is of course in principle not possible for the channel to close Completely and there by reduce the current id to Zero for, if such indeed, could be the case the gate voltage Vgs is applied in the direction to provide additional reverse bias

1) When voltage is applied between the drain and source with a battery Vdd, the electrons flow from source to drain through the narrow channel existing between the depletion regions. This constitutes the drain current id, its conventional direction is from drain to source.

2) The value of drain current is maximum when no external voltage is applied between gate and source and is designated by Idss.

5. JFET has the following parameters: IDSS = 32 mA ; VGS (off) = – 8V ; VGS = – 4.5 V. Find the value of drain current.(Nov 2015)

$$I_D = I_{DSS}\left[1-\frac{V_{GS}}{V_{GS(off)}}\right]^2$$

$$= 32\left[1-\frac{(-4.5)}{-8}\right]^2 \text{ mA}$$

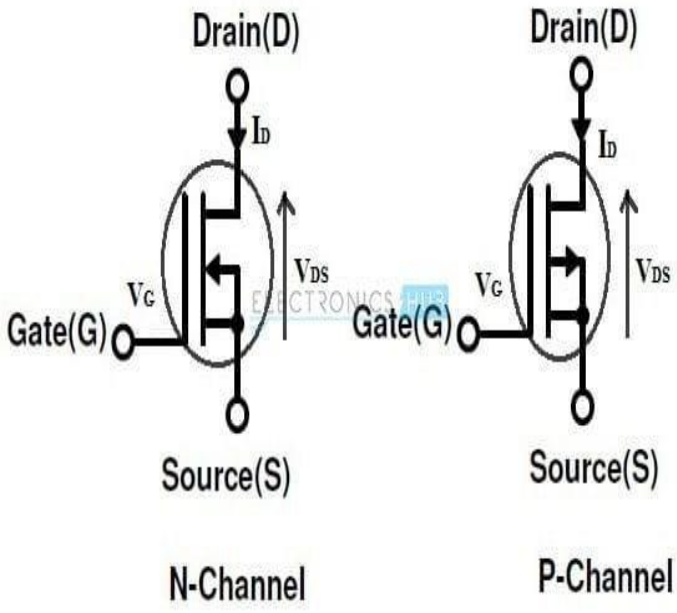
$$= 6.12 \text{ mA}$$

6. A) Explain working of MOSFET. (Nov 2015, Nov 2016)

B) Explain N-channel enhancement type of MOSFET. (April/May 2016, Nov/Dec 2017, May 2019)

MOSFET:

Most MOSFETS are triodes, with the substrate internally connected to the source. The circuit symbols used by several manufacturers are indicated in the Fig below.



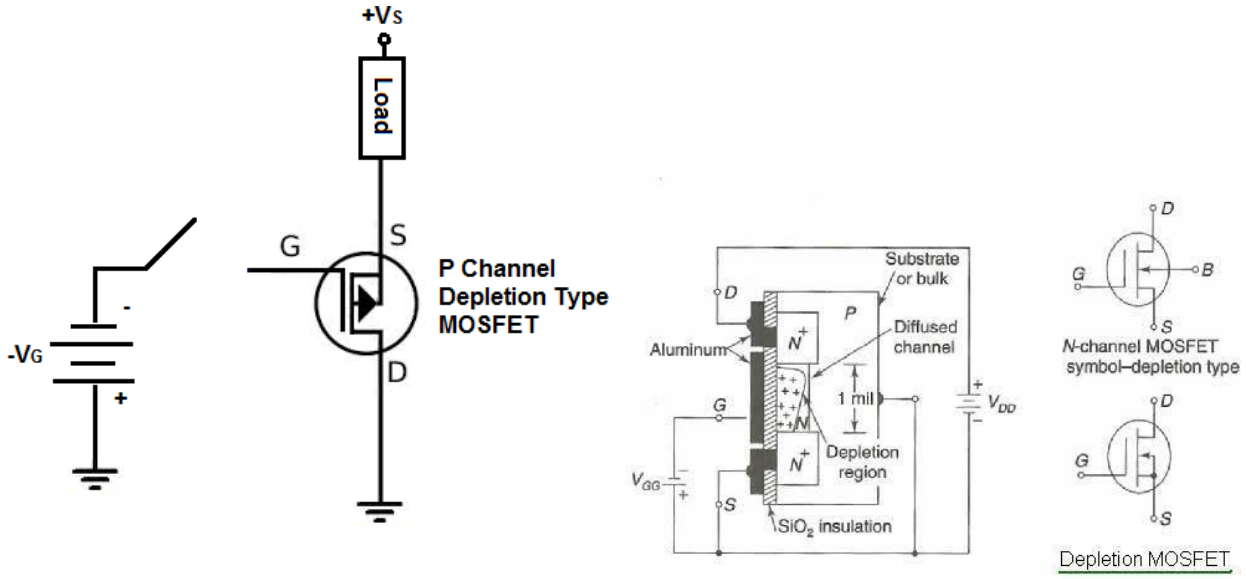
Here are two basic types of MOSFETS,

(1) Depletion type

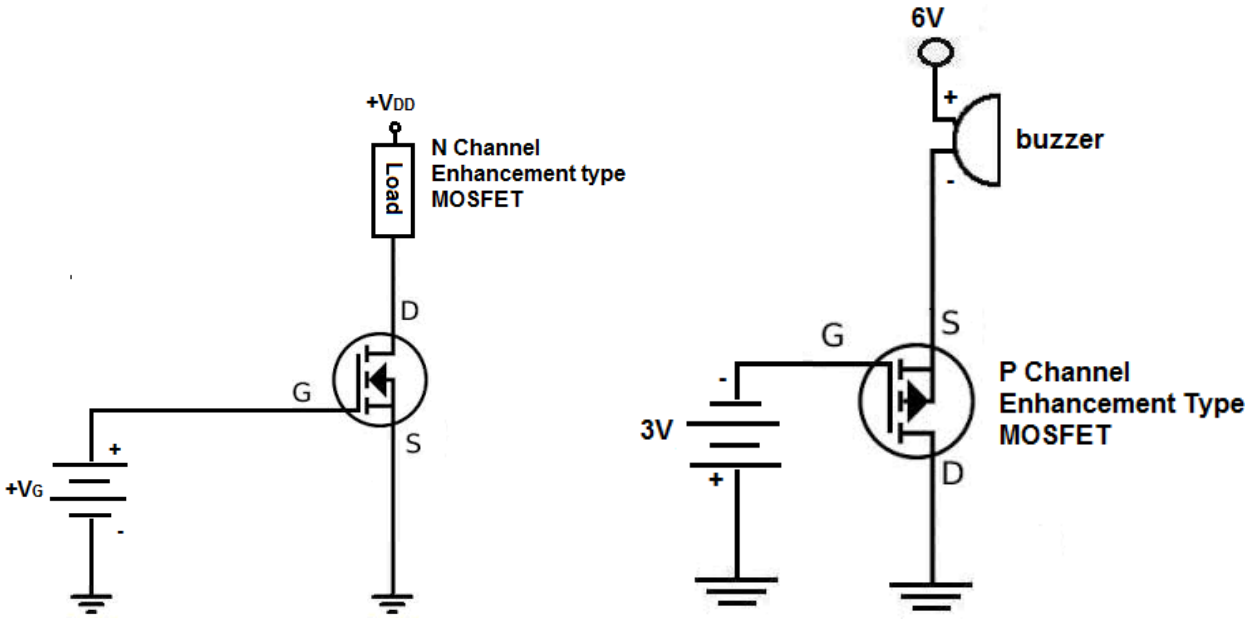
(2) Enhancement type MOSFET.

D-MOSFETS: D-MOSFETS can be operated in both the depletion mode and the enhancement mode. E MOSFETS are restricted to operate in enhancement mode. The primary difference between them is their physical construction.

The construction difference between the two is shown in the fig given below.



As we can see the D MOSFET have physical channel between the source and drain terminals(Shaded area)



The E MOSFET on the other hand has no such channel physically. It depends on the gate voltage to form a channel between the source and the drain terminals. Both MOSFETS have an insulating layer between the gate and the rest of the component. This insulating layer is made up of SIP, a glass like insulating material. The gate material is made up of metal conductor Thus going

from gate to substrate, we can have metal oxide semiconductor which is where the term MOSFET comes from,

In the symbol for the MOSFET, the arrow is placed on the substrate. As with JFET an arrow pointing represents an N-channel device, while an arrow pointing out represents p-channel device.

CONSTRUCTION OF AN N-CHANNEL MOSFET:

The N- channel MOSFET consists of a lightly doped p type substance into which two heavily doped n+ regions are diffused as shown in the Fig. These n+ sections, which will act as source and drain.

A thin layer of insulation silicon dioxide (SIO2) is grown over the surface of the structure, and holes are cut into oxide layer, allowing contact with the source and drain. Then the gate metal area is overlaid on the oxide, covering the entire channel region Metal contacts are made to drain and source and the contact to the metal over the channel area is the gate terminal.The metal area of the gate, in conjunction with the insulating dielectric oxide layer and the semiconductor channel, forms a parallel plate capacitor. The insulating layer of sio2

Is the reason why this device is called the insulated gate field effect transisto. This layer results in an extremely high input resistance (10 10 to 10power 15ohms) for MOSFET.

DEPLETION MOSFET

The basic structure of D-MOSFET is shown in the fig. An N-channel is diffused between source and drain with the device an appreciable drain current IDSS flows foe zero gate to source voltage, Vgs=0.

Depletion mode operation:

1) The above fig shows the D-MOSFET operating conditions with gate and source terminals shorted together(VGS=OV)

2) At this stage ID= IDSS where VGS=OV, with this voltage VDS, an appreciable drain current IDSS flows.

3) If the gate to source voltage is made negative i.e. VGs is negative .Positive charges are induced in the channel through the SI02 of the gate capacitor.

4) Since the current in a FET is due to majority carriers(electrons for an N-type material), the induced positive charges make the channel less conductive and the drain current drops as Vgs is made more negative.

5) The re distribution of charge in the channel causes an effective depletion of majority carriers, which accounts for the designation depletion MOSFET

6) That means biasing voltage Vgs depletes the channel of free carriers This effectively reduces the width of the channel, increasing its resistance.

7) Note that negative Vgs has the same effect on the MOSFET as it has on the JFET.

8) As shown in the fig above, the depletion layer generated by Vgs (represented by the white space between the insulating material and the channel) cuts into the channel, reducing its width. As a result,Id<ldss. The actual value of ID depends on the value of Idss,Vgs(off) and Vgs,

Enhancement mode operation:

1) This operating mode is a result of applying a positive gate to source voltage Vgs to the device.

2) When Vgs is positive the channel is effectively widened. This reduces the resistance of the channel allowing ID to exceed the value of IDSS

3) When Vgs is given positive the majority carriers in the p-type are holes. The holes in the p type substrate are repelled by the +ve gate voltage.

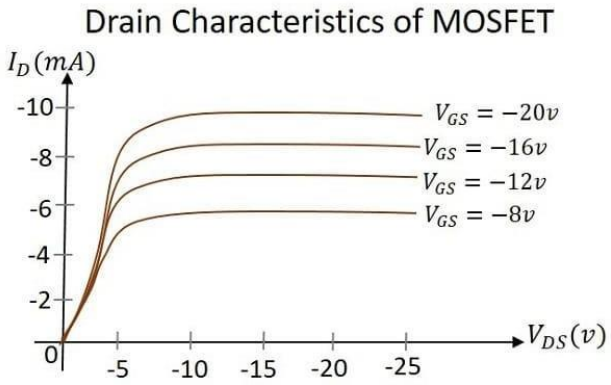
4) At the same time, the conduction band electrons (minority carriers) in the p type material are attracted towards the channel by the gate voltage

5) With the build up of electrons near the channel, the area to the right of the physical channel effectively becomes an N type material.

6) The extended n type channel now allows more current, Id> Idss.

Characteristics of MOSFET:

Drain characteristics:



1) The curves are plotted for both Vgs positive and Vgs negative voltages

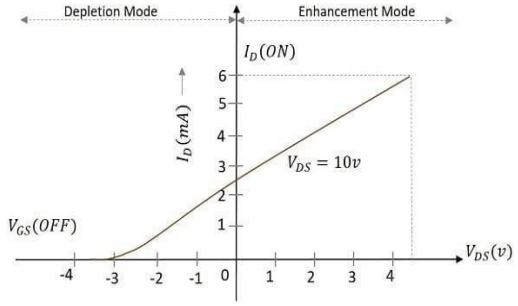
2) When Vgs=0 and negative the MOSFET operates in depletion mode when Vgs is positive the MOSFET operates in the enhancement mode.

3) The difference between JFET and D MOSFET is that JFET does not operate for positive values of Vgs.

4) When Vds=0, there is no conduction takes place between source to drain, if Vgs<0 and Vds>0 then Id increases linearly.

5) But as Vgs, induces positive charges holes in the channel, and controls the channel width. Thus the conduction between source to drain is maintained as constant, i.e. Id is constant.

6) If Vgs>0 the gate induces more electrons in channel side, it is added with the free electrons generated by source again the potential applied to gate determines the channel width and maintains constant current flow through it as shown in Figure.



Transfer Characteristics of a MOSFET

Transfer characteristics:

The combination of 3 operating states i.e. Vgs=OV, VGs<OV, Vgs>0V is represented by the D MOSFET transconductance curve.

1) Here in this curve it may be noted that the region AB of the characteristics similar to that of JFET

2) This curve extends for the positive values of Vgs

3) Note that id=idss for Vgs=0V when Vgs is negative, id loss when Vgs= Vgs(off) ,id is reduced to approximately omAWhere Vgs is positive Id>ldss.So obviously Idss is not the maximum possible value of Id for a MOSFET.

4) The curves are similar to JFET so thet the D MOSFET have the same transconductance equation.

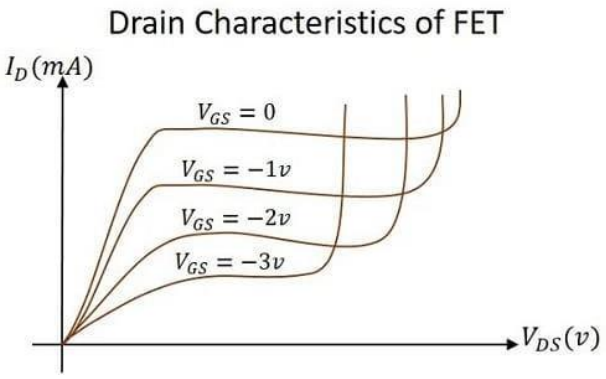
APPLICATION OF MOSFET

One of the primary contributions to electronics made by MOSFETS can be found in the area of digital computer electronics). The signals in digital circuits are made up of rapidly switching de levels. This signal is called as a rectangular wave made up of two dc levels (or logic levels). These logic levels are OV and +SV.

7. What are the application of FET as a voltage variable resistor? (Nov2015)

JFET AS A VVR OR VDR

Let us consider the drain characteristics of FET as shown in the fig.



In this characteristics we can see that in the region before pinch off voltage, drain characteristics are linear, i.e. FET operation is linear.

In this region the FET is useful as a voltage controlled resistor, i.e. the drain to source resistance is controlled by the bias voltage VGS. In this region only FET behaves like an ordinary resistor This resistances can be varied by VGS) .The operation of FET in the region is useful in most linear applications of FE in such an application the FET is also referred to as a voltage variable resistor (WVR) or voltage dependent resistor (VDR).

When the variation of the rd with VGS can be closely approximated by the expression,

gd=Id/Vds

gd=gd0(1-(Vgs/Vp)^1/2)

rd=(r0/1-KVgs)

Where ro = drain resistance at zero gate bias.K = a constant, dependent upon FET

Application of VVR :

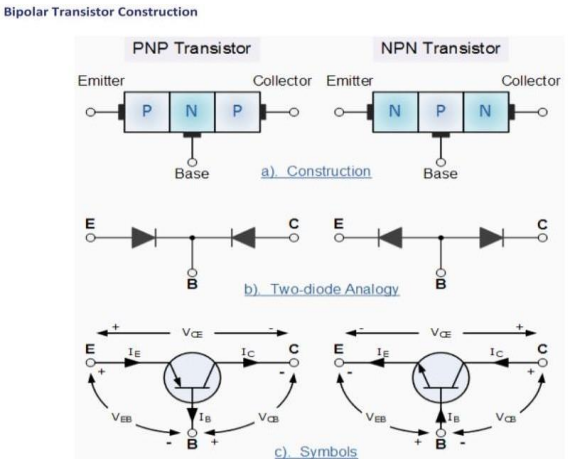
- The VVR property of FET can be used to vary the voltage gain of a multistage amplifier A, as the signal level is increased. This action is called AGC automatic gain control.
- When output signal level increases, the drain to source resistance rd increases, increasing effective RE. Increase in RE causes the gain of transistor Q1 to decrease, reducing the output signal. Exactly reverse process takes place when output signal level decreased.

- The output signal level is maintained constant. It is to be noted that the DC bias conditions of Q1 are not affected by JFET since FET is isolated from Q1 by capacitor C2..

8. Explain CC configuration of BJT with input and output characteristics (Nov/Dec 2017)

The Bipolar Transistor basic construction consists of two PN-junctions producing three connecting.terminals with each terminal being given a name to identify it from the other two. These three terminals are known and labelled as the Emitter (E), the Base (B) and the Collector (C) respectively. There are two basic types of bipolar transistor construction, PNP and NPN, which basically describes the physical arrangement of the P-type and N-type semiconductor materials from which they are made.

1. **Active Region** - the transistor operates as an amplifier and Ic = B.ib 2. Saturation - the transistor is "fully-ON" operating as a switch and Ic = (saturation) 3. Cut-off - the transistor is "fully-OFF" operating as a switch and fc = 0 Bipolar Transistors are current regulating devices that control the amount of current flowing through them in proportion to the amount of biasing voltage applied to their base terminal acting like a current-controlled switch. The principle of operation of the two transistor types PNP and NPN, is exactly the same the only difference being in their biasing and the polarity of the power supply for each type.

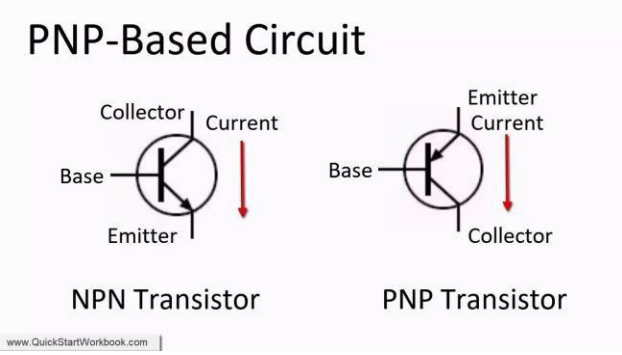


Bipolar Junction Transistor Symbol

The construction and circuit symbols for both the PNP and NPN bipolar transistor are given above with the arrow in the circuit symbol always showing the direction of "conventional current

flow" between the base terminal and its emitter terminal. The direction of the arrow always points from the positive P-type region to the negative N-type region for both transistor types, exactly the same as for the standard diode symbol.

Transistor current components

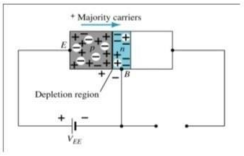


The above figure shows the various current components, which flow across the forward biased emitter junction and reverse-biased collector junction. The emitter current le consists of hole current les holes crossing from emitter into base) and electron current lof electrons crossing from base into emitter).

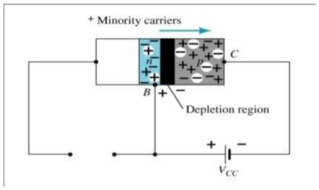
I= Ico loc

For a p-n-p transistor, it consists of holes moving across Je from left to right (base to collector) and electrons crossing lc in opposite direction. Assumed referenced direction for Ica i.e. from right to left, then for a p-n-p transistor, Icos negative. For an n-p-n transistor, lco is positive. The basic operation will be described using the pnp transistor. The operation of the pnp transistor is exactly the same the roles played by the electron and hole are interchanged.

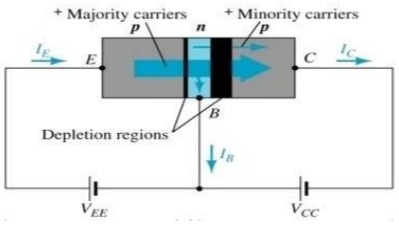
One p-n junction of a transistor is reverse-biased, whereas the other is forward-biased.



3.3a Forward-biased junction of a pnp transistor



3.3b Reverse-biased junction of a pnp transistor



Applying KCL to the transistor:

Ie = Ic + Ib

The comprises of two components - the majority and minority carriers

Ic = lc majority + lc minority

Ico - Ic current with emitter terminal open and is called leakage current.

Emitter Efficiency:

$$\gamma = \frac{currentofinjectedcarriersatJ_E}{totalemittercurrent}$$

$$\gamma = \frac{I_{PE}}{I_{pE} + I_{nE}} = \frac{I_{pE}}{I_{nE}}$$

Transport Factor:

$$\beta^* = \frac{injectedca\ rriercurrentreaching J_C}{injectedca\ rrierncurrentatJ_E}$$

$$\beta^* = \frac{I_{pC}}{I_{nE}}$$

Large signal current gain:

The ratio of the negative of collector current increment to the emitter current change from zero (cut off)to Ir the large signal current gain of a common base transistor

$$\alpha = \frac{-(I_C - I_{CO})}{I_E}$$

Since lc and le have opposite signs, then a, as defined, is always positive. Typically numerical values of a lies in the range of 0.90 to 0.995.

$$\alpha = \frac{I_{pC}}{I_E} = \frac{I_{pC}}{I_{nE}} * \frac{I_{pE}}{I_E} \qquad \alpha = \beta * \gamma$$

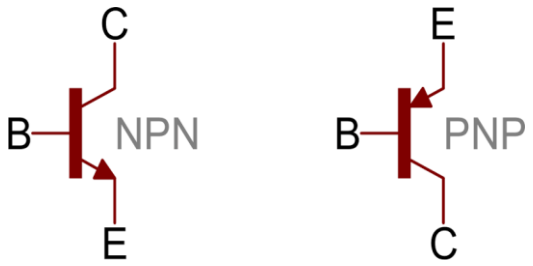
The transistor alpha is the product of the transport factor and the emitter efficiency. This statement assumes that the collector multiplication ratio a is unity is the ratio of total current crossing to hole arriving at the junction.junction

9. Explain NPN transistor working and its construction (Nov/Dec 2019)

Definition: The transistor in which one p-type material is placed between two n-type materials is known as NPN transistor. The NPN transistor amplifies the weak signal enter into the base and produces strong amplify signals at the collector end. In NPN transistor, the direction of movement of an electron is from the emitter to collector region due to which the current constitutes in the transistor. Such type of transistor is mostly used in the circuit because their majority charge carriers are electrons which have high mobility as compared to holes.

Construction of NPN Transistor

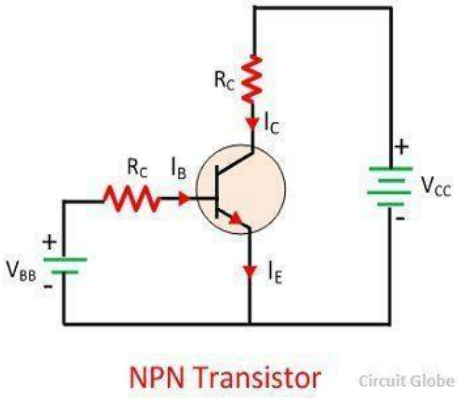
The NPN transistor has two diodes connected back to back. The diode on the left side is called an emitter-base diode, and the diodes on the left side are called collector-base diode. These names are given as per the name of the terminals.



The NPN transistor has three terminals, namely emitter, collector and base. The middle section of the NPN transistor is lightly doped, and it is the most important factor of the working of the transistor. The emitter is moderately doped, and the collector is heavily doped.

Circuit Diagram of NPN Transistor

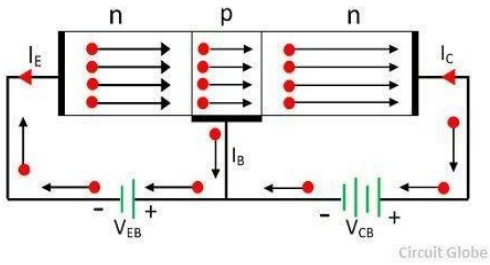
The circuit diagram of the NPN transistor is shown in the figure below. The collector and the base circuit is connected in reverse biased while the emitter and base circuit is connected in forward biased. The collector is always connected to the positive supply, and the base is in negative supply for controlling the ON/OFF states of the transistor.



Working of NPN Transistor

The circuit diagram of the NPN transistor is shown in the figure below. The forward biased is applied across the emitter-base junction, and the reversed biased is applied across the collector-

base junction. The forward biased voltage VEB is small as compared to the reverse bias voltage VCB.



The emitter of the NPN transistor is heavily doped. When the forward bias is applied across the emitter, the majority charge carriers move towards the base. This causes the emitter current IE. The electrons enter into the P-type material and combine with the holes.

The base of the NPN transistor is lightly doped. Due to which only a few electrons are combined and remaining constitutes the base current IB. This base current enters into the collector region. The reversed bias potential of the collector region applies the high attractive force on the electrons reaching collector junction. Thus attract or collect the electrons at the collector.

The whole of the emitter current is entered into the base. Thus, we can say that the emitter current is the sum of the collector or the base current.

10. Explain the Structure of Thyristor, operation and it's characteristics (Nov/Dec 2019)

The thyristor or silicon controlled rectifier, SCR has a structure that consists of four layers: it contains a PNPN sandwich.

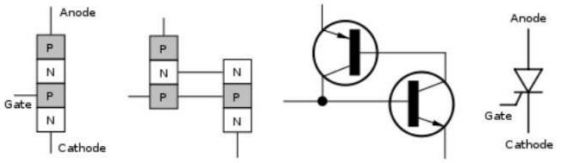
Construction of SCR Or Thyristor:

An SCR consists of four layers of alternating P and N type semiconductor materials. Silicon is used as the intrinsic semiconductor, to which the proper dopants are added. The junctions are either diffused or alloyed.

The planar construction is used for low power SCRs (and all the junctions are diffused). The mesa type construction is used for high power SCRs. In this case, junction J2 is obtained by the diffusion method and then the outer two layers are alloyed to it, since the PNPN pellet is

required to handle large currents. It is properly braced with tungsten or molybdenum plates to provide greater mechanical strength.

One of these plates is hard soldered to a copper stud, which is threaded for attachment of heat sink. The doping of PNPN will depend on the application of SCR, since its characteristics are similar to those of the thyratron. Today, the term thyristor applies to the larger family of multilayer devices that exhibit bistable state-change behavior that is, switching either ON or OFF.The operation of a SCR and other thyristors can be understood in terms of a pair of tightly coupled bipolar junction transistors, arranged to cause the self-latching action. The following figures are construction of SCR, its two transistor model and symbol respectively.



Construction, Two transistor model of SCR and symbol of SCR

SCR Working Principle:

The SCR is a four-layer, three-junction and a three-terminal device and is shown in fig. 1.24. The end P- region is the anode, the end N-region is the cathode and the inner P-region is the gate. The anode to cathode is connected in series with the load circuit. Essentially the device is a switch. The thyristor then switches on and current flows and continues to conduct without further gate signals. Ideally the thyristor has zero impedance in conduction state. For switching off or reverting to the blocking stat there must be no gate signal and the anode current must be reduced to zero. Current can flow only one direction

A voltage bias, as shown in figure, and an external circuit to carry current allow internal currents which Include the following terms:

- The current Ixis due to
- Majority carriers (holes) crossing junction J1
- Minority carriers crossing junction J1
- Holes injected at junction J2 diffusing through the N-region and crossing junction J1 and

- Minority carriers from junction J2 diffusing through the N-region and crossing junction J1

SCR Equivalent Circuit

The basic structure of SCR can be divided into 3-layer structure as shown in Fig. 17.5 (a). It may noted that the upper 3-layer structure is a PNP transistor w ereas the lower one is an NPN transistor Thus SCR can be represented by two transistors , le PNP) and (... NPN) interconnected a shown in Fig 175. Sometimes, this is also called as the two transistor analogy or an illegal latch of an SCR. triggering devices. Such devices are unijunction transistor, diac, silicon unilateral switch etc.

Turning ON (or Triggering) SCR

The SCR can be turned ON, from its OFF position, by several methods as discussed below:

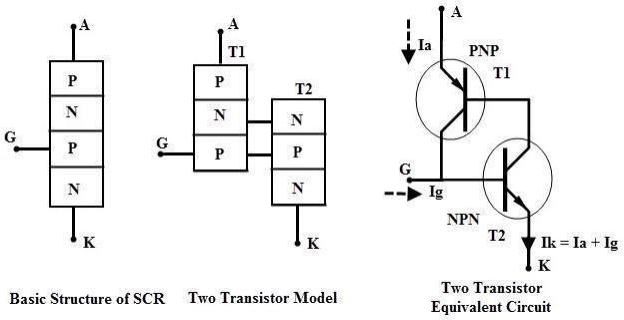
1. Forward breakover voltage: If the voltage across the SCR exceeds the rated forward breakover voltage, the SCR will start conducting due to avalanche breakdown.

2. Gate trigger. This is the most commonly used method to trigger the SCR. In this method, the SCR is operated with an anode voltage slightly less than the rated forward breakover voltage and is triggered into conduction by a low-power gate pulse. It may be noted that once the SCR is switched ON, the gate has no further control on the device current. The gate pulse signal can be supplied either from a d.c. source or an a.c. source.

Fig shows an SCR connected to the d.c. source through a load. In this case, the gale signal is generated by a push button switch (S). When the switch (S) is pressed, momentarily, a positive voltage is applied at the gate. As a result of this, the SCR is turned ON, and the current flows through the lond The SCR will remain in its ON position, until the supply voltage is removed reversed.

3. Rate-effect or dVd triggering: In this method, the SCR is turned ON by rapidly increasing the anode-to-cathode voltage. The ruptuly increasing anode-to-cathode voltage moduces a charging current, which triggers the SCR to conduction.

4 Light triggering: In this method, the SCR is triggered by irradiating it with light. When the light falls on the middle junction (J,) of the SCR, the device turns ON. Such a device is called Light. Activated Silicon Controlled Rectifier (LASCR).



Basic Structure of SCR Two Transistor Model Two Transistor Equivalent Circuit

Applications of SCR

The SCR has a number of applications, yet the following industrial applications are important from the subject point of view.

1. Motor speed control
2. Light-dimming control
3. Heater control

ELECTRONIC DEVICES AND CIRCUITS

UNIT V

2 MARKS

1. What is the advantages of Negative Feedback. (Nov 2014 , April/May 2016 , Nov/Dec 2019)

The negative feedback has less frequency distortion.

- It has highly stabilized gain.
- It can control step response of amplifier.
- It has less harmonic distortion.
- It has less amplitude distortion.

2. What are the conditions to be satisfied for sustained oscillations. (Nov 2014)

If the loop gain is equal to unity then sustained oscillations will be produced.

3. Negative feedback is preferred to other methods of modifying amplifier characteristics. Why? (April/May 2015)

The applied negative feedback can improve its performance (gain stability, linearity, frequency response, step response) and reduces sensitivity to parameter variations due to manufacturing or environment. Because of these advantages, many amplifiers and control systems use negative feedback.

4. State the Bharkausen's criterion for oscillation. (April/May 2015, 2016 , Nov/Dec 2018 , 2019)

Generally, the Barkhausen criteria has two conditions, first the closed-loop gain is equal to 1, second the closed-loop phase is equal to 0, with these conditions, the oscillator circuit would generate a sinusoidal signal.

5. Define pinch off voltage of JFET. (Nov 2015)

The Pinch-Off value of theJFET refers to the voltageapplied between Drain and Source (with the Gatevoltage at zero volts) at which maximum current flows. Operating with the

Drain/Source voltagebelow this value is classed is the "Ohmic Region" as the JFET will act rather like a resistor.

6. List the advantages of crystal oscillator. (Nov 2015, May 2017)

- Stability is one of the most important requirements of any oscillator.
- High Q. The Q factor or quality factor describes how 'underdamped' oscillators.
- Frequency Customization and Range.
- Low Phase Noise.
- A Crystal Oscillator Is Compact and Inexpensive

7. Specify the various types of power amplifier (Nov 2016)

- Power amplifiers designed to amplify analog signals come under A, B, AB or C category.
- Power amplifiers designed to amplify Pulse Width Modulated(PWM) digital signals come under D, E, F etc.

8. What are the essentials conditions for maintaining oscillation. (Nov 2016)

To ensure sustained oscillations, the loop gain must be slightly greater than one when circuit is turned on for the first time. For Wien bridge oscillator, the gain of the amplifier must be greater than three (A>3), which will ensure that sustained oscillations build up in the circuit

9. Name two high frequency ocsillators. (May 2017)

- Hartley Oscillator.
- Colpitt Oscillator.
- Hartley Oscillator

10. List out the four types of feedback topologies available for an amplifier. (Nov/Dec 2017)

- Voltage Series Feedback Amplifier
- Voltage Shunt Feedback Amplifier
- Current Series Feedback Amplifier
- Current Shunt Feedback Amplifier

11. Write down the expression of frequency of oscilaltion of colpitt's oscillation. (Nov/Dec 2017)

Frequency,

$$f = \frac{1}{2\pi\sqrt{LC}} \text{ where } C_s = \frac{C_1 C_2}{C_1 + C_2}$$

12. Write the effects of negative feedback on the various characteristics of amplifier. (May/April 2018)

Feedback reduces the overall gain of a system with the degree of reduction being related to the systems open-loop gain. Negative feedback also has effects of reducing distortion, noise, sensitivity to external changes as well as improving system bandwidth and input and output impedances.

13. What is the undamped oscillation. (May/April 2018)

The oscillations whose amplitude remains constant with time are called undamped oscillations. Systems which can generate such oscillations are called self-excited oscillating systems and they are maintained by an external energy source in a non-linear dissipative system.

14. Name the types feedback amplifier. (Nov/Dec 2018)

- Positive Feedback Amplifier
- Negative Feedback Amplifier

15. What are the feedback amplifier. (May 2019)

Feedback Amplifier is a device that is based on the principle of feedback. The process by which some part or fraction of output is combined with the input is known as feedback.

16. Give the classification of oscillators. (May 2019)

- **Sinusoidal or Hormonic oscillators**
    - Tuned circuit ocsillators
    - RC oscillators

- Crystal ocsillators
- Negative-resistance oscillators

- **Non-sinusoidal or Relaxation oscillators**

11 MARKS

1. **Draw and explain various feedback topologies. (Nov 2014)**

(or)

Explain voltage series and voltage shunt feedback connection of feedback amplifier. (April/May 2017, Nov/Dec 2019)

Feedback Amplifiers Topologies

In the feedback amplification of the signals, either the voltage or the current signals can be applied at the input of the amplifiers. Hence the topologies that are known for its series and the shunt characteristics are applied for both the voltage and the current signals. Hence the four topologies of these amplifiers are as follows:

Voltage Series

In this type of amplifier, the feedback in the circuit is designed in such a way that the output signal applied to input is in series connection. The feedback circuit to the output signal is in parallel so that there observed minimum output impedance. Whereas the feedback circuit is in series with the input signal so that impedance at this stage can be enlarged.

Voltage Shunt

In this type, the voltage signal generated at the output is fed back to the input through the feedback circuit. But in this case, the feedback circuit is connected in shunt with the input. In this case, both the input and the output are connected in shunt with the feedback circuit. Hence at both sides, the value of the impedance maintained is low.

Current Series

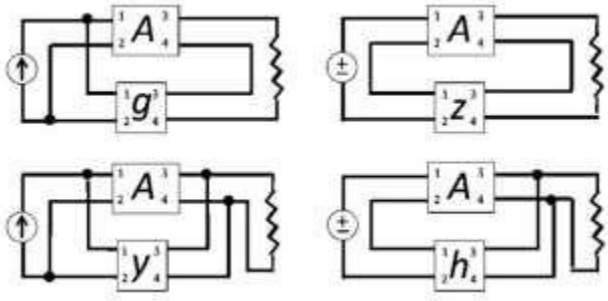
In this type of feedback amplification of the signals the part of the output signal that is fed back to the input signal is related in terms of series to the feedback circuit. Due to the series

connection established in the output and the input signals concerning the feedback circuit thee impedance value is high at both sides.

Current Shunt

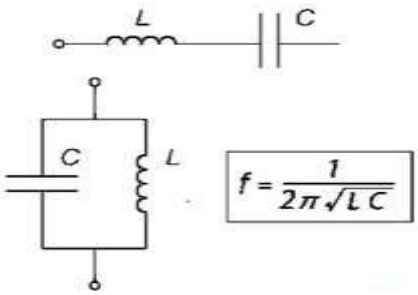
The feedback circuit connected in series for the output and parallel to the input signal is

known as a current shunt feedback amplifier. Due to the parallel connection with the input the value of impedance is low at this point. Whereas the output connected in terms of series makes the value of impedance high.



2. Derive the general conditions for oscillations for a LC oscillators. (Nov 2014)

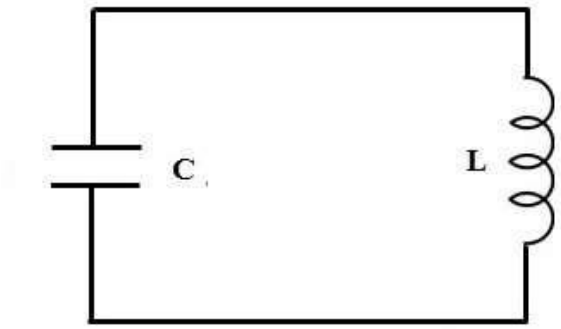
An oscillator is an electronic circuit used to change an input DC to an output AC. This can have an extensive range of waveforms with different frequencies based on the application. Oscillators are used in several applications like test equipment which generate any of these waveforms like a sinusoidal, sawtooth, square wave, triangular waveforms. LC Oscillator is usually used within RF circuits due to their high-quality phase noise characteristics as well as easy implementation. Basically, an oscillator is an amplifier that includes positive or negative feedback. In electronic circuit design, the main problem is to stop the amplifier from oscillating when trying to acquire oscillators to oscillate. This article discusses an overview of LC oscillator and circuit working.



This circuit is also called as LC tuned or LC resonant circuit. These oscillators can understand with the help of FET, BJT, Op-Amp, MOSFET, etc. The applications of LC oscillators mainly include frequency mixers, RF signal generators, tuners, RF modulators, sine wave generators, etc.

LC Oscillator Circuit Diagram

An LC circuit is an electric circuit that can be built with an inductor and capacitor where the inductor is denoted with 'L' and the capacitor is denoted with 'C' both allied within a single circuit. The circuit works like an electrical resonator which stores energy to oscillate at the resonant frequency of the circuit.



These circuits are used either to select a signal at the particular frequency through the compound signal otherwise generating signals at a particular frequency. These circuits work like major components within a variety of electronic devices such as radio apparatus, circuits such as filters, tuners, and oscillators. This circuit is a perfect model that imagines that the dissipation of energy doesn't happen because of resistance. The main function of this circuit is to oscillate through the least damping to make the resistance minimum possible.

LC Oscillator Derivation

The oscillations frequency can be produced from the tank circuit which completely relies upon the inductor, capacitor values & their condition of resonance. So it can be stated by using the following formula.

$XL = 2*\pi* f* L$

$XC = 1/ (2*\pi* f* C)$

We know that, at resonance, XL is equal to XC. So the equation will become like the following.

$2*\pi* f* L = 1/ (2*\pi* f* C)$

Once the equation can be shortened then the equation of LC oscillator frequency includes the following.

$f2 = 1/ ((2\pi) * 2 LC)$

$f = 1/ (2\pi \sqrt{} (LC))$

3. A) Draw and explain the operation of Hartley oscillator. (Nov 2015)

(or)

Draw the Hartley oscillator circuit and derive the condition for frequency of oscillations. (Nov 2016)

(or)

Explain the construction and working of Hartley oscillator with a circuit diagram. (April/May 2016)

(or)

Explain the Operation of Hartley oscillator. (April/May 2017)

B) With a neat diagram, Explain the working and construction of BJT RC phase shift oscillator. (Nov 2015)

(or)

With a neat diagram, explain the construction and working of RC phase shift oscillator. (April/May 2016)

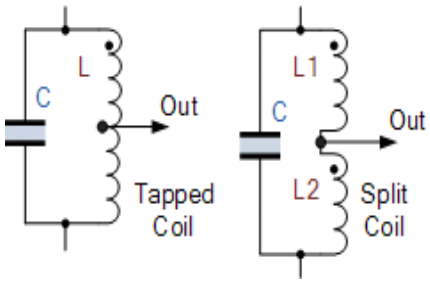
(or)

State the operation of an RC phase shift oscillator with a neat diagram and derive the condition for oscillation and resonant Frequency with BJT. (May 2017, Nov/Dec 2019)

C) Brief about any two high Frequency LC oscillations. (Nov/Dec 2018)

A) Hartley Oscillator:

The Hartley Oscillator design uses two inductive coils in series with a parallel capacitor to form its resonance tank circuit producing sinusoidal oscillations.



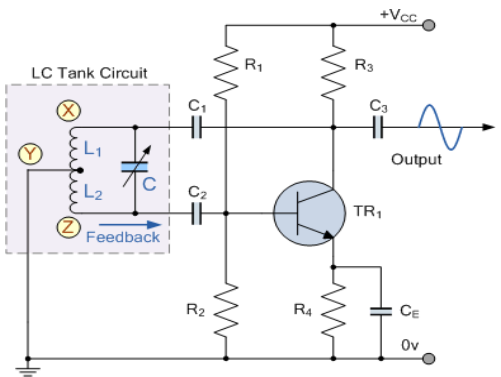
In the Hartley Oscillator the tuned LC circuit is connected between the collector and the base of a transistor amplifier. As far as the oscillatory voltage is concerned, the emitter is connected to a tapping point on the tuned circuit coil.

The feedback part of the tuned LC tank circuit is taken from the centre tap of the inductor coil or even two separate coils in series which are in parallel with a variable capacitor, C .

The Hartley circuit is often referred to as a split-inductance oscillator because coil L is centre-tapped. In effect, inductance L acts like two separate coils in very close proximity with the current flowing through coil section XY induces a signal into coil section YZ

An Hartley Oscillator circuit can be made from any configuration that uses either a single tapped coil (similar to an autotransformer) or a pair of series connected coils in parallel with a single capacitor.

Basic Hartley Oscillator Design:



When the circuit is oscillating, the voltage at point X (collector), relative to point Y (emitter), is 180o out-of-phase with the voltage at point Z (base) relative to point Y. At the frequency of oscillation, the impedance of the Collector load is resistive and an increase in Base voltage decrease in the Collector voltage.

Thus there is a 180o phase change in the voltage between the Base and Collector and this along with the original 180o phase shift in the feedback loop provides the correct phase relationship of positive feedback for oscillations to be maintained.

The amount of feedback depends upon the position of the "tapping point" of the inductor. If this is moved nearer to the collector the amount of feedback is increased, but the output taken between the Collector and earth is reduced and vice versa. Resistors, R1 and R2 provide the usual stabilizing DC bias for the transistor in the normal manner while the capacitors act as DC-blocking capacitors.

In this Hartley Oscillator circuit, the DC Collector current flows through part of the coil and for this reason the circuit is said to be "Series-fed" with the frequency of oscillation of the Hartley Oscillator.

$$f = \frac{1}{2\pi\sqrt{L_T C}}$$

$$\text{where: } L_T = L_1 + L_2 + 2M$$

The frequency of oscillations can be adjusted by varying the "tuning" capacitor, C or by varying the position of the iron-dust core inside the coil (inductive tuning) giving an output over a wide range of frequencies making it very easy to tune. Also the Hartley Oscillator produces an output amplitude which is constant over the entire frequency range.

B) The RC Oscillator Circuit

RC Oscillators use a combination of an amplifier and an RC feedback network to produce output oscillations due to the phase shift between the stages.

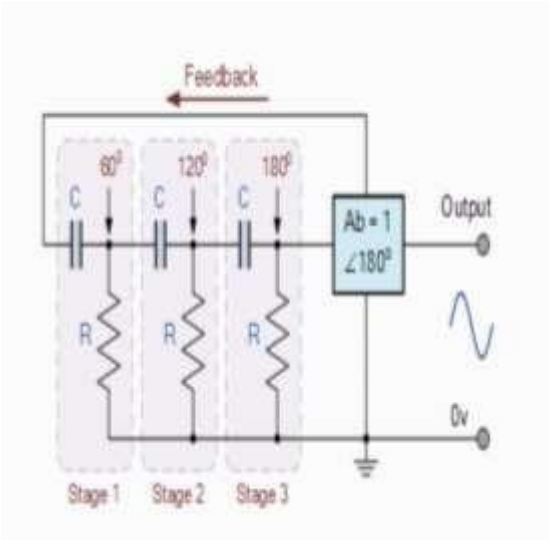
The basic RC Oscillator which is also known as a Phase-shift Oscillator, produces a sine wave output signal using regenerative feedback obtained from the resistor-capacitor (RC) ladder network. This regenerative feedback from the RC network is due to the ability of the

capacitor to store an electric charge, (similar to the LC tank circuit).

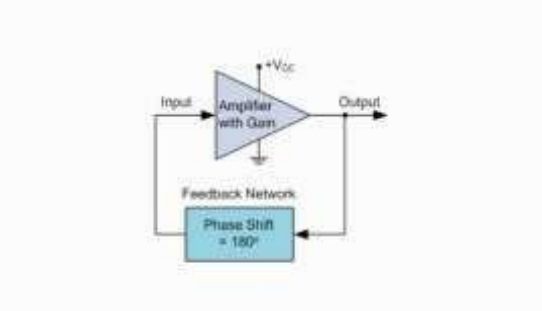
This resistor-capacitor feedback network can be connected as shown above to produce a leading phase shift (phase advance network) or interchanged to produce a lagging phase shift (phase retard network) the outcome is still the same as the sine wave oscillations only occur at the frequency at which the overall phase-shift is 360o.

By varying one or more of the resistors or capacitors in the phase-shift network, the frequency can be varied and generally this is done by keeping the resistors the same and using a 3-ganged variable capacitor because capacitive reactance (XC) changes with a change in frequency as capacitors are frequency-sensitive components. However, it may be required to re-adjust the voltage gain of the amplifier for the new frequency.

If the three resistors, R are equal in value, that is R1 = R2 = R3, and the capacitors, C in the phase shift network are also equal in value, C1 = C2 = C3, then the frequency of oscillations produced by the RC oscillator is simply given as:

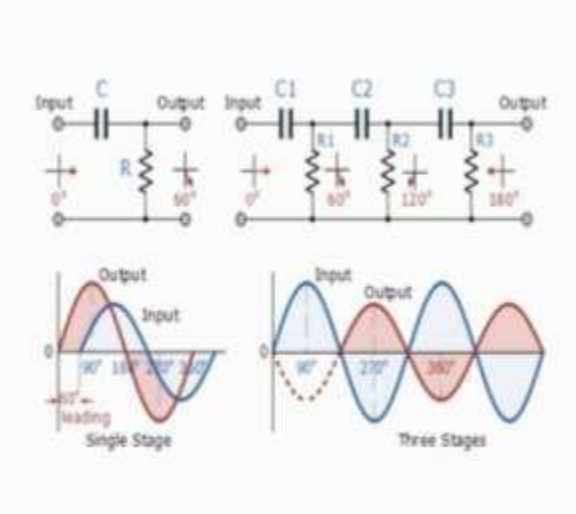


In an RC Oscillator circuit the input is shifted 180o through the feedback circuit returning the signal out-of-phase and 180o again through an inverting amplifier stage to produces the required positive feedback. This then gives us “180o + 180o = 360o” of phase shift which is effectively the same as 0o, thereby giving us the required positive feedback. In other words, the total phase shift of the feedback loop should be “0” or any multiple of 360o to obtain the same effect.



In a Resistance-Capacitance Oscillator or simply known as an RC Oscillator, we can make use of the fact that a phase shift occurs between the input to a RC network and the output from the same network by using interconnected RC elements in the feedback branch,

RC Phase-Shift Network:



The circuit on the left shows a single resistor-capacitor network whose output voltage "leads" the input voltage by some angle less than 90o. In a pure or ideal single-pole RC network. it would produce a maximum phase shift of exactly 90o, and because 180o of phase shift is required for oscillation, at least two single-poles networks must be used within an RC oscillator design.

Z = R – j

Z = Z ∠ – Φ Ohms Xc

However in reality it is difficult to obtain exactly 90o of phase shift for each RC stage so we must therefore use more RC stages cascaded together to obtain the required value at the

oscillation frequency. The amount of actual phase shift in the circuit depends upon the values of the resistor (R) and the capacitor (C), at the chosen frequency of oscillations with the phase angle (φ) .

RC Phase Angle

$$X_C = \frac{1}{2\pi fC} \qquad R = R,$$

$$Z = \sqrt{R^2 + (X_C)^2}$$

$$\therefore \quad \phi = \tan^{-1}\frac{X_C}{R}$$

Where: XC is the Capacitive Reactance of the capacitor, R is the Resistance of the resistor, and f is the Frequency.

In our simple example above, the values of R and C have been chosen so that at the required frequency the output voltage leads the input voltage by an angle of about 60o. Then the phase angle between each successive RC section increases by another 60o giving a phase difference between the input and output of 180o (3 x 60o).

By simplifying the circuit with equivalent AC circuit, we get

The frequency of oscillations,

f = 1/ (2

f= 1/ (2 π R C √ 6) π R C √ ((4Rc / R) + 6))

If Rc/R << 1, then

The condition of sustained oscillations,

hfe (min) = (4 Rc/ R) + 23 + (29 R/Rc)

Advantages of Phase Shift Oscillators

- Due to the absence of expensive and bulky high-value inductors, circuit is simple to design and well suited for frequencies below 10 KHz.

- These can produce pure sinusoidal waveform since only one frequency can fulfill the Barkhausen phase shift requirement.
- It is fixed to one frequency.

Disadvantages of Phase Shift Oscillators

- These oscillators produce 5% of distortion level in the output.
- This oscillator gives only a small output due to smaller feedback

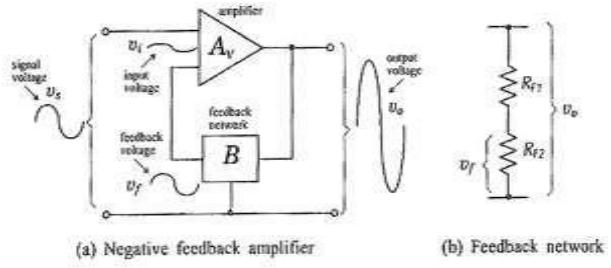
4. A) Differentiate Oscillators with amplifier.

PARAMETERS	AMPLIFIER	OSCILLATOR
Definition	An amplifier is a circuit which amplifies the weak signal and raises the amplitude of the signal**.**	An oscillator is a circuit which generates the AC waveforms of particular frequency for providing source to an electronic circuit.
Function	An amplifier is used repetitively in a circuit, because the signal loses its intensity after travelling to a long distance.	An Oscillator is used only in the initial stage when the circuit requires signal source
Feedback	It uses negative feedback	It uses positive feedback.
Requirement of Input	The input is required for its operation, it cannot operate without input.	It do not require any input to perform operation.
Type of Signal Generated	The Signal can be periodic or non-periodic.	The signal generated by it will be always periodic in nature.

B) Derive the equation for the voltage gain of an amplifier that uses series voltage negative feedback. (Nov 2015)

Voltage Series Negative Feedback Amplifier:

In a negative feedback amplifier, a small portion of the output voltage is fed back to the input. When the feedback voltage is applied in series with the signal voltage, the arrangement is Voltage Series Negative Feedback Amplifier. The instantaneous polarity of the feedback voltage is normally opposite to the signal voltage polarity, (they are in series-opposition). So, the feedback voltage is negative with respect to the signal voltage; hence the term negative feedback.



(a) Negative feedback amplifier (b) Feedback network

Figure 13-1
In a negative feedback amplifier a portion of the output is fed back to the input. The instantaneous polarity of the feedback voltage (v_f) is negative with respect to the signal voltage (v_s).

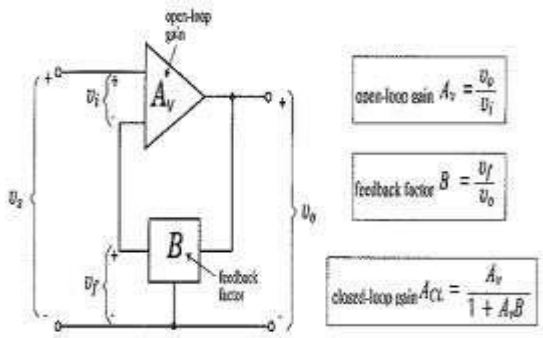
An amplifier with two input terminals and one output is shown (in triangular representation). The amplifier has a voltage gain (Av), and its output voltage (vo) is applied to a feedback network that reduces vo by a factor (B) to produce a feedback voltage (vf). The feedback network may be as simple as the resistive voltage divider. At the amplifier input, the instantaneous level of vf is applied negative with respect to vs, so that the amplifier input terminal voltage is,

$$v_i = v_s - v_f$$

Because the amplifier Input voltage is lower than the signal voltage, the output voltage is lower than that produced when negative feedback is not used. This means, of course, that the overall voltage gain (vo/vi) is reduced by negative feedback. However, as will be demonstrated, the stability of the voltage gain is greatly improved with Voltage Series Negative Feedback Amplifier.

Voltage Gain with Negative Feedback Amplifier:

Consider the feedback amplifier illustrated and recall that vi is amplified to produce vo, and that vo is divided by the feedback network to produce vf. Also, that vf is applied (along with vs) to the amplifier input. It is seen that there is a closed loop from the amplifier input to the output, and then back to the input. Because of this closed loop, the overall voltage gain with negative feedback is termed the closed-loop gain (ACL).



When the feedback network is disconnected, the loop is opened, and the gain without feedback is referred to as the open-loop gain (Av). Alternative symbols sometimes used for the open-loop gain are AOL and Av(OL).

The overall voltage gain (closed-loop gain) of the amplifier

$$A_{CL} = \frac{v_o}{v_s}$$

and the feedback factor is,

$$B = \frac{v_f}{v_o}$$

The input voltage is,

$$\begin{aligned} v_i &= v_s - v_f \\ v_i &= v_s - Bv_o \\ v_o &= A_v v_i = A_v(v_s - Bv_o) \\ &= A_v v_s - A_v B v_o \\ v_o(1 + A_v B) &= A_v v_s \\ \frac{v_o}{v_s} &= \frac{A_v}{1 + A_v B} \end{aligned}$$

So, the equation for overall voltage gain with negative feedback is,

$$A_{CL} = \frac{A_v}{1 + A_v B}$$

Series Voltage Negative Feedback Amplifier stabilizes amplifier voltage gain

$$A_{CL} \approx \frac{1}{B}$$

it is seen that to design a negative feedback amplifier with a particular closed-loop gain, it is only necessary to design the feedback network to give ACL ≈ 1/B. For example, for ACL = 100, B ≈ 1/100. It must be remembered that for Eq. 13-3 to be correct, AvB >> 1, or

$$A_v >> \frac{1}{B}$$

which means that,

$$A_v >> A_{CL}$$

Thus, for satisfactory operation of a negative feedback amplifier.

5. Describe the General Characteristics of negative feedback and positive feedback. (May 2018)

Basis for Comparison	Positive Feedback	Negative Feedback
Also called as	Regenerative feedback	Degenerative feedback
Relation between input and output	In phase	Out of phase

Basis for Comparison	Positive Feedback	Negative Feedback
Overall gain	Greater than the gain of the system where feedback is not present.	Smaller than the gain of the system where feedback is absent.
Effective input	Sum of applied input and fed back signal.	Difference of applied input and fed back signal
Transfer function of system with respective feedback	$\frac{G}{1-GH}$	$\frac{G}{1+GH}$
Stability	Less	Comparatively more
Phase shift	0° or 360°	180°
Feedback is taken from	Non-inverting terminal of op-amp	Inverting Terminal of op-amp
Sensitivity	Low	High
Use	In oscillators.	In amplifiers.

6. A) Explain the Operation of colpitt's oscillator. (April/May 2017)

(or)

Brief on Colpitt's oscillations. (May 2019, Nov 2016, May 2017)

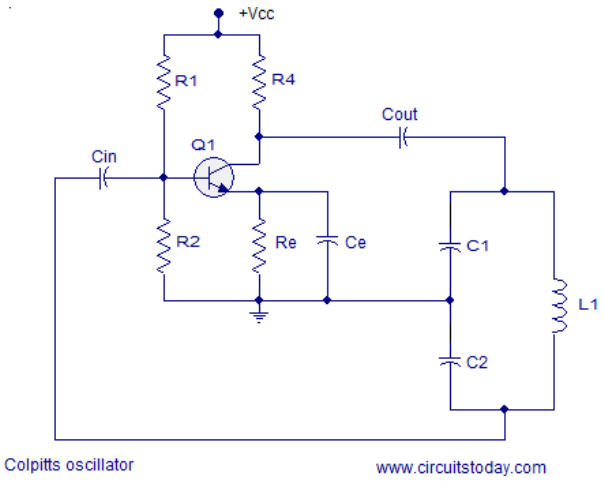
B) Explain the Operation of crystal oscillations. (May 2019, Nov 2016, May 2017)

A) COLPITT'S OSCILLATIONS:

An oscillator is used to produce electronic signal with oscillating periods. Eg: Sine wave, square wave etc.. Oscillators are broadly classified into two – linear oscillators and non-linear oscillators. As the name implies, linear oscillators are used to produce linear or sinusiodal waveforms. Whereas, non-linear oscillators are used to produce non-linear (non-sinusoidal output waveforms). All types of electronic oscillators use their input voltage to control the oscillation frequency.

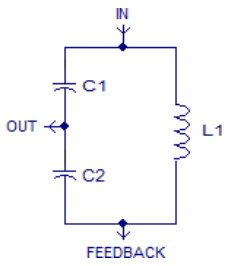
Colpitts Oscillator is an electronic oscillator which uses an inductor and capacitors to form an LC oscillator circuit.It is another type of sinusoidal LC oscillator and is basically a harmonic oscillator, which has a lot of applications. The Colpitts oscillator can be realized using valves, transistors, FETs or op-amp. It is much similar to the Hartley oscillator except the addition of tank circuit. In Colpitts oscillator the tank circuit consists of two capacitors in series and an inductor connected in parallel to the serial combination.

Colpitts oscillator is generally used in RF applications and the typical operating range is 20KHz to 300MHz. In Colpitts oscillator, the capacitive voltage divider setup in the tank circuit works as the feed back source and this arrangement gives better frequency stability when compared to the Hartley oscillator which uses an inductive voltage divider setup for feedback. The circuit diagram of a typical Colpitts oscillator using transistor.



In the circuit diagram resistors R1 and R2 gives a voltage divider biasing to the transistor. Resistor R4 limits the collector current of the transistor. Cin is the input DC decoupling capacitor while Cout is the output decoupling capacitor. Re is the emitter resistor and its meant for thermal stability. Ce is the emitter by-pass capacitor. Job of the emitter by-pass capacitor is to by-pass the amplified AC signals from dropping across Re. The the emitter by-pass capacitor is not there, the amplified AC signal will drop across Re and it will alter the DC biasing conditions of the transistor and the result will be reduced gain. Capacitors C1, C2 and inductor L1 forms the tank circuit. Feedback to the base of transistor is taken

from the junction of Capacitor C2 and inductor L1 in the tank circuit.



When power supply is switched ON, capacitors C1 and C2 starts charging. When they are fully charged they starts discharging through the inductor L1. When the capacitors are fully discharged, the electrostatic energy stored in the capacitors gets transferred to the inductor as magnetic flux. The the inductor starts discharging and capacitors gets charged again. This transfer of energy back and forth between capacitors and inductor is the basis of oscillation. Voltage across C2 is phase opposite to that of the voltage across the C1 and it is the voltage across C2 that is fed back to the transistor. The feedback signal at the base base of transistor appears in the amplified form across the collector and emitter of the transistor.

The energy lost in the tank circuit is compensated by the transistor and the oscillations are sustained. The tank circuit produces 180° phase shift and the transistor itself produces another 180° phase shift. That means the input and output are in phase and it is a necessary condition of positive feedback for maintaining sustained oscillations. The frequency of oscillations of the Colpitts oscillator can be determined,

$$F = \frac{1}{2\pi\sqrt{LC}}$$

Where L is the inductance of the inductor in the tank circuit and C is the effective capacitance of the capacitors in the tank circuit. If C1 and C2 are the individual capacitance, then the effective capacitance of the serial combination C= (C1C2)/(C1+C2). By using ganged variable capacitors in place of C1 and C2, the Colpitts oscillator can be made variable.

B) CRYSTALS OSCILLATIONS:

Whenever an oscillator is under continuous operation, its frequency stability gets affected.

There occur changes in its frequency. The main factors that affect the frequency of an oscillator are

- Power supply variations
- Changes in temperature
- Changes in load or output resistance

In RC and LC oscillators the values of resistance, capacitance and inductance vary with temperature and hence the frequency gets affected. In order to avoid this problem, the piezo electric crystals are being used in oscillators.

The use of piezo electric crystals in parallel resonant circuits provide high frequency stability in oscillators. Such oscillators are called as Crystal Oscillators.

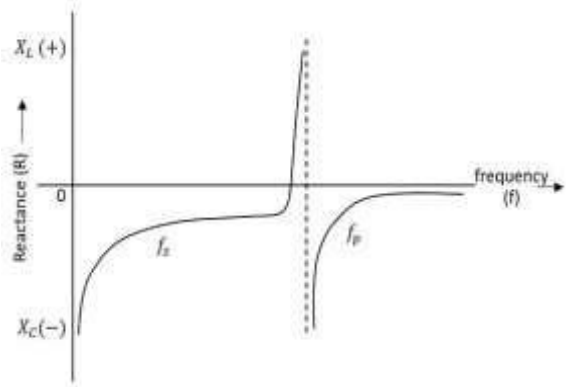
Crystal Oscillators

The principle of crystal oscillators depends upon the Piezo electric effect. The natural shape of a crystal is hexagonal. When a crystal wafer is cur perpendicular to X-axis, it is called as X-cut and when it is cut along Y-axis, it is called as Y-cut.

The crystal used in crystal oscillator exhibits a property called as Piezo electric property. So, let us have an idea on piezo electric effect.

Frequency response

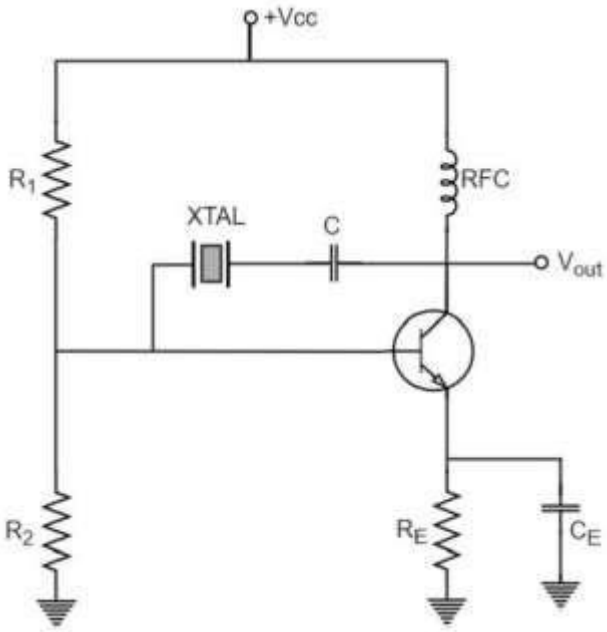
The frequency response of a crystal is as shown below. The graph shows the reactance (XL or XC) versus frequency (f). It is evident that the crystal has two closely spaced resonant frequencies.



Crystal Oscillator Circuit

A crystal oscillator circuit can be constructed in a number of ways like a Crystal controlled tuned collector oscillator, a Colpitts crystal oscillator, a Clap crystal oscillator etc. But the transistor pierce crystal oscillator is the most commonly used one. This is the circuit which is normally referred as a crystal oscillator circuit.

The following circuit diagram shows the arrangement of a transistor pierce crystal oscillator.



In this circuit, the crystal is connected as a series element in the feedback path from collector to the base. The resistors R1, R2 and RE provide a voltage-divider stabilized d.c. bias circuit. The capacitor CE provides a.c. bypass of the emitter resistor and RFC (radio frequency choke) coil provides for d.c. bias while decoupling any a.c. signal on the power lines from

affecting the output signal. The coupling capacitor C has negligible impedance at the circuit operating frequency. But it blocks any d.c. between collector and base.

The circuit frequency of oscillation is set by the series resonant frequency of the crystal and its value is given by the relation,

$$f_o = \frac{1}{2\pi\sqrt{L.C}}$$

It may be noted that the changes in supply voltage, transistor device parameters etc. have no effect on the circuit operating frequency, which is held stabilized by the crystal.

Advantages

- They have a high order of frequency stability.
- The quality factor (Q) of the crystal is very high.

Disadvantages

- They are fragile and can be used in low power circuits.
- The frequency of oscillations cannot be changed appreciably.