UNIT – I

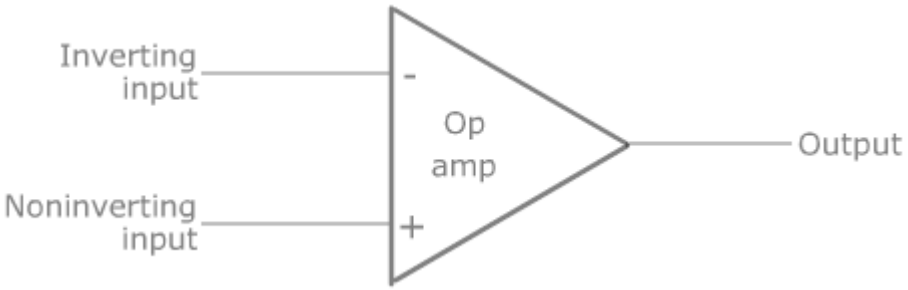
Operational Amplifiers

Linear IC- Operational amplifier: Introduction to linear ICs – Operational amplifierIC741 – Block diagram and characteristics – DC and AC performance – Open loopconfigurations – Feedback configurations – Inverting , Non inverting and Differentialamplifier – Summer, Subtractor, Integrator, Differentiator – Zero crossing detector – Schmitt trigger – Window detector – Astable and MonostableMultivibrators, V-I and IVConverters. Filter and its types – Instrumentation amplifier – Precision rectifiers -Logarithmic and antilog amplifiers – Multiplier.

Operational Amplifier:

The operational amplifier is a direct-coupled high gain amplifier. It is a versatile multi-terminal device that can be used to amplify dc as well as ac input signals. It was originally designed for performing mathematical operations such as addition, subtraction, multiplication and integration and is abbreviated as op-amp.

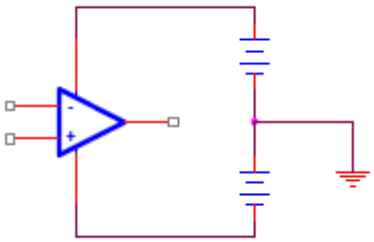
Circuit Symbol:



The circuit schematic of an op-amp is a triangle. It has two input terminals and one output terminal.

Op-amps have 5 basic terminals. 2 inputs 1 outputs and 2 power supply terminals. The signification of the other terminals varies with the type of op-amp.

Power supply connection:



V^+ and V^- power supply terminals are connected to two dc voltage sources. V^+ pin is connected to positive terminal of one source and $v^-$is connected to negative terminal of other source as shown in fig. The common terminal is connected to a reference point or ground.

The source is 15 V battery and it range from $\pm$5 V to $\pm$22 V.

Package Types:

Three popular packages available are

1. Dual in line package (DIP).
2. Metal can package (TO).
3. Flat package.

Op-amp packages may contain single, dual or quad op-amps. Typical packages have 8, 10 or 14 terminals.

The widely used very popular type µA741 is a single op-amp available as an 8 pin can, DIP or 10 pin flat pack.

Manufacturer's Designation for Linear IC's:

Each manufacturer uses a specific code and assigns a specific type number IC's e.g. 741 an internally compensated op-amp originally manufactured by fair child is sold as µA 741. Where µA represent the identifying initials.

Initials used by some well known manufacturers are

National Semiconductor	LM, LH, LF
Fair child	µA, µAF
Motorola	MC
Texas Instruments	SN

Ideal Op-amp:

An ideal op-amp exhibit the following characteristics,

Open loop voltage gain	$A_{OL} = \infty$
Input impedance	$R_i = \infty$
Output impedance	$R_0 = 0$
Bandwidth	$BW = \infty$
Zero offset i.e. $V_o = 0$	When $V_1 = V_2 = 0$

These properties cannot be realized in practice. However the use of ideal op-amp model simplifies the mathematics involved in op-amp circuits. Practical op-amp can be made to approximate some of these characteristics.

Equivalent circuit of an op-amp:

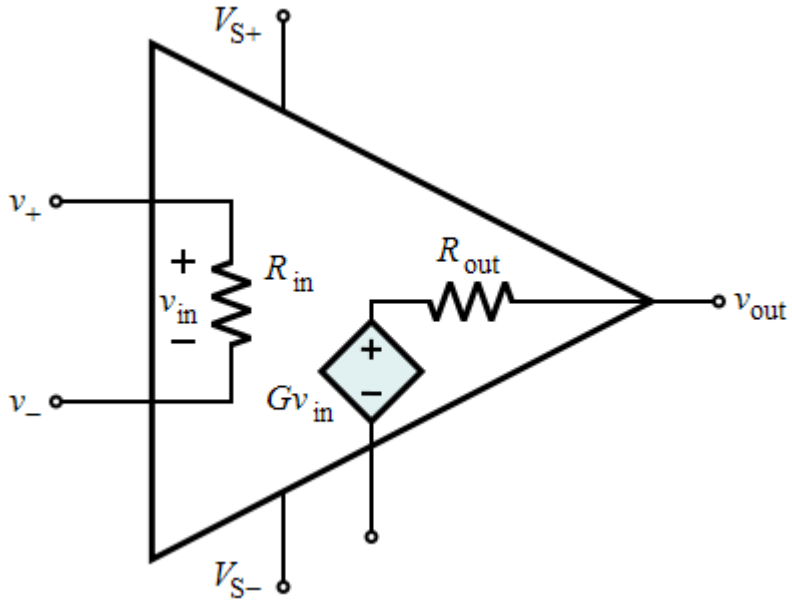


Fig. shows an equivalent circuit of an op-amp. Op-amp is a voltage controlled voltage source when $A_{oc}V_d$ is an equivalent Thevenin's voltage source and R_0 is the thevenin equivalent resistance looking back into the output terminal.

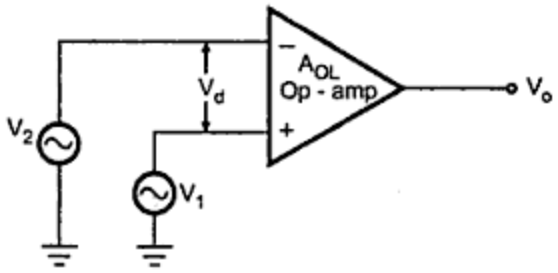
The equivalent circuit is useful in analyzing the basic operating principles of op-amp. From the circuit the output voltage

$$V_0 = A_{oL}\, V_d$$

$$= A_{OL}(V_1 - V_2)$$

i.e. the op-amp amplifies the difference between the two input voltages.

Open loop operation of op-amp:



The simplest way to use an op-amp is in the open loop mode as shown in fig. Since the gain is infinite, the output voltage V_0 is either at its $+V_{sat}$ (saturation voltage) or $-V_{sat}$ as $V_1>V_2$ or $V_2>V_1$ respectively. The output assumes one of the two possible output states and the amplifier acts as a switch only.

THE IDEAL OP-AMP CHARACTERISTICS:

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Ouput impedance,	R_0	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_0 = 0$ when $v_1 = v_2 = 0$.

It can be seen that

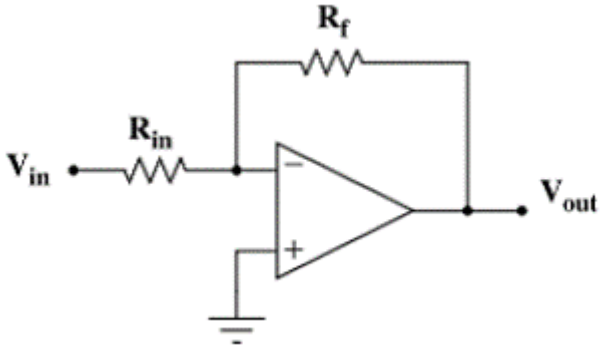
(1)An ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(2)Since gain is ∞ , the voltage between the inverting and non – inverting terminals, i.e., differential input voltage $v_d = (v_2 – v_1)$ is essentially zero for finite output voltage v_0.

(3)The output voltage v_0 is independent of the current drawn from the output as $R_0 =0$. The output thus can drive an infinite number of other devices.

GAIN FORMULA FOR INVERTING AMPLIFIER:

This is the most widely used of all the op-amp circuits. The circuit is shown in fig., The output voltage v_0 is fed back to the inverting input terminal through the R_f-R_1 network where R_f is the feedback resistor. Input signal v_i is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.



Assume an ideal op-amp as $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = v_i / R_1$$

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage,

$$v_0 = —i_1 R_f = — v_i R_f / R_1$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = v_0 / v_i = —R_f / R_1$$

Alternative the nodal equation at the node 'a'

$$v_a – v_i / R_1 + v_a – v_0 / R_f = 0$$

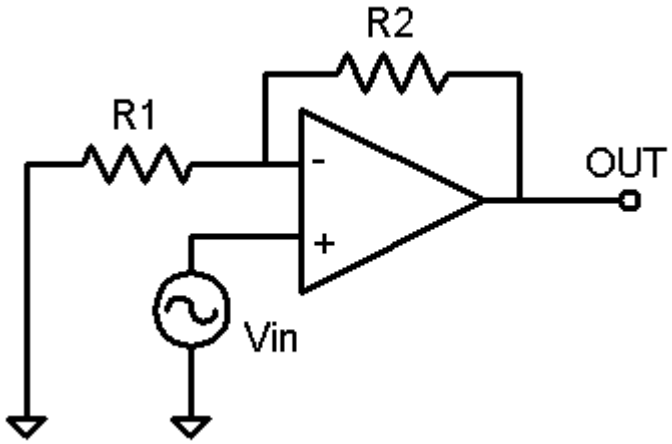
where v_a is the voltage at node 'a'. since node 'a' is at virtual ground $v_a = 0$. Therefore we get,

$$A_{CL} = v_0 / v_i = —R_f / R_1$$

The negative sign indicates a phase shift of 180° between v_i and v_0.

GAIN FORMULA FOR NON INVERTING AMPLIFIER:

If a signal is applied to the non-inverting input terminal and feed back is given as shown in fig., the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may also be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.



As the differential voltage vd at the input terminal of op-amp is zero, the voltage at node 'a'is v_i, same as the input voltage applied to non-inverting input terminal. Now RF and R1 forms a potential divider. Hence

$$v_i = v_0 R_1 / R_1 + R_f$$

As no current flows into the op-amp.

$$v_0 / v_i = (R_1 + R_f)/R_1 = 1 + R_f / R_1$$

Thus for non inverting amplifier the voltage gain,

$$A_{CL} = v_0 / v_i = 1 + R_f / R_1$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1.

electrical characteristics of op-amp. Give typical values.

The various electrical characteristics of op-amp are,

Input offset voltage:

It is the voltage that must be applied between the input terminals of an op-amp to nullify the output. Since this voltage could be positive or

negative its absolute value is listed on the data sheet. For 741C, the maximum value is 6 mV.

Input offset current:

The algebraic difference between the currents into the (-) input and (+) input is referred to as input offset current. It is 200nA maximum for 741C.

Input bias current:

The average of the currents entering into the (-) input and (+) input terminals of an op-amp is called as input bias current. Its value is 500nA for 741C.

Input resistance:

This is the differential input resistance as seen at the either of the input terminals with the other terminal connected to ground. For the 741C, the input resistance is 2MΩ.

Input capacitance:

It is the equivalent capacitance that can be measured at either of the input terminal with the other terminal connected ground. A typical value of C_1 is 1.4pF.

Offset voltage adjustment range:

A special feature of the 741 family op-amp is the provision of offset voltage null capability. For 741C offset voltage adjustment range is ± 15mV.

Input voltage range:

This is the common-mode voltage that can be applied to both input terminals without disturbing the performance of an op-amp. For the 741C, the range of the input common-mode voltage is ±13V. Common-mode configuration is used only for test purpose to determine the degree of matching between the inverting and non-inverting terminals.

Common-mode rejection ratio:

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio(CMRR) and gives the figure of merit ρ for the differential amplifier. So, CMRR is given by;

$$\rho = | A_{DM}/A_{CM} |$$

and is usually expressed in decibels(dB). For 741C, CMRR is typically 90dB. CMRR is usually measured under the test condition that the input source resistance $R_S \leq 10K\Omega$. The higher the value of CMRR, better is the matching between the two input terminals and smaller the output common-mode voltage.

Supply voltage rejection ratio:

The change in an op-amp's input offset voltage due to variations in supply voltage is called the supply voltage rejection ratio(SVRR). Some manufacturers use terms like power supply rejection ratio(PSRR) or power supply sensitivity(PSS). These terms are expressed in microvolts per volt or in decibels. For 741C, SVRR = 150μV/V. Obviously , lower the value of SVRR, better the op-amp.

Large signal voltage gain:

An op-amp amplifies the difference voltage between the two input terminals and, its voltage gain is defined as,

Voltage gain = output voltage / differential input voltage

Since the amplitude of the output signal is much larger than the input signal, the voltage gain is commonly referred as large signal voltage gain. For 741C, typical value is,2,00,000 under test conditions, $R_L \geq 2k\Omega$ and $V_0 = \pm 10V$.

Output voltage swing:

The output voltage swing indicates the value of positive and negative saturation voltages of an op-amp, and never exceeds the supply voltage V^+ and V^-. For 741C, the output voltage swing is guaranteed to be between +13V and —13V for $R_L \geq 2k\Omega$.

Output resistance:

Output resistance R_0 is the resistance measured between the output terminal of the op-amp and the ground. It is 75Ω for the 741C op-amp.

Output short circuit current:

This is the current thay may flow if an op-amp gets shorted accidentally and is generally high. The op-amp must be provided with short circuit protection. The short circuit current I_{sc} for 741C is 25mA. This means that the built-in short circuit protection is guaranteed to withstand 25mA of current.

Supply current:

Supply current I_s is the current drawn by the op-amp from the power supply. It is 2.8mA for 741C.

Power consumption:

This gives the amount of quiescent power(V_i = 0V) that must be consumed by the op-amp so as to operate properly. It is 85mW for 741C.

Transient response:

The rise time and overshoot are the two characteristics of the transient response of any circuit. Thes parameters are of importance whenever selecting an op-amp for ac applications. For 741C, rise time is 0.3μs and overshoot is 5%.

Slew rate:

This is another parameter of importance whenever selecting an op-amp for high frequency applications. Op-amp 741C has a low slew rate (0.5V/μs) and therefore cannot be used for high frequency applications.

AC and DC performance characteristics of op-amp in detail.

Dc characteristics:

An ideal op- amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non- ideal dc characteristics that add error components to the dc output voltage are:

1. Input bias current
2. Input offset current
3. Input offset voltage
4. Thermal drift

1. Input bias current:

It is defined as the average value of the base currents entering into the input terminals of an op-amp during the input bias current.

The op-amp input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into their linear region by supplying

currents into the bases by the external circuit. In an ideal op-amp we assume that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as IB^ (-) and IB^ (+) respectively. Even though both the transistors are identical, IB^ (-) and IB^ (+) are not exactly equal due to internal imbalances between the two inputs. IB= IB^ (+) + IB^ (-)/ 2 ,Where IB^ (+) – bias current at non- inverting terminal

IB (-) - bias current at inverting terminal

Input bias current compensation:

- IB for BJT is 500mA
- IB for FET is 50pA

By introducing compensation resistor at the non-inverting input terminal we can able to reduce the input bias current.

Rcomp=R1/ Rf= (R1* Rf) / (R1+Rf)

2. Input offset current:

Bias current compensation will work efficiently if both the bias currents IB^ (+) and IB^ (-) are equal. The input transistors cannot be made identical. Hence there will be difference in bias currents. This difference is called as input offset current Ios and can be written as

| Ios | = IB^ (+) – IB^ (-)

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Input offset current for BJT is 200nA.

Input offset current for FET is 10pA.

The effect of Ios can be minimized by having the feedback resistor value to be small.

3. Input offset voltage:

In spite of the use of the above compensation techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage Vios. This is the voltage required to be applied at the input for making output voltage to zero volts.

The voltage V_2 at negative terminal is

$V_2 = R_1.V_0/R_1+R_f$

Or $V_0 = (R_1 + R_f)V_2/R_1 = (1+ R_f/R_1)V_2$

Since $V_{OS} = |V_i – V_2|$ and $V_i = 0$

$V_{OS} = |0 – V_2| = V_2$

4. Thermal drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully mulled at 25 degree Celsius may not remain so when the temperature rises to 35 degree Celsius. This is called drift. Often, offset current drift is expressed in nA/0C and offset voltage drift in mV/0C. These indicate the change in offset for each degree Celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be equal be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Ac characteristics:

For small signal sinusoidal applications the a.c. characteristics are
1. Frequency response 2. Slew rate

1. Frequency response:

An ideal op-amp has infinite band width that is open loop gain is 90dB with d.c.signal and this gain should remain the same through audio and radio frequency.

But practically op-amp gain decreases at high frequency. This is due to a capacitive component in the equivalent circuit of op-amp.

Due to R0C, the gain decreases by 20 dB per decay and the frequency is said to be brake or corner frequency and is given by

$$f1 = 1/ (2*3.14*R0*C)$$

$$|A| = A0*L/ (1+ (f/f1) ^2)$$

2. Slew rate:

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. for e.g. A 1V/μs slew rate means that the output rises or falls by 1V in one 1μs.

The rate of change of output voltage due to the step input voltage and is usually specified as V/micro sec.

For example: 1V/micro sec. slew rate denotes the output rises or falls by 1 volts in 1 micro seconds.

The rate at which the voltage across the capacitor dVc/dt is given by

$$dVc/dt = I/C$$

Slew rate SR $dVc/dt|max = Imax/ C$
For IC741
Imax= 15 micro amps, C= 30 Pico farad
Slew rate = 0.5V/ micro sec.

Open loop op-amp configurations:

When connected in open loop mode op-amp simply functions as a high gain amplifier.
Three configurations are

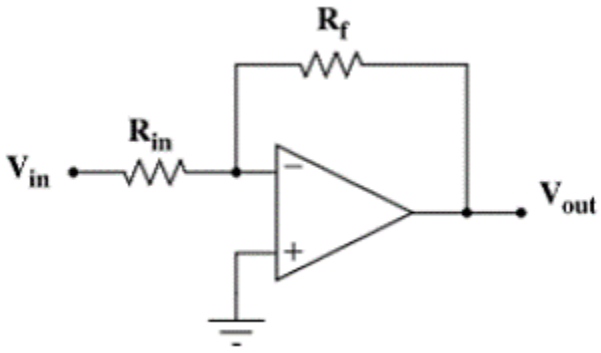
1. Differential Amplifier
2. Inverting Amplifier
3. Non inverting Amplifier

Feed back in op-amp:

The utility of an op-amp can be greatly increased by providing negative feedback. Here the output is not driven into saturation and the circuit behaves in a linear manner.

Inverting Amplifier:

This is the most widely used of all the op-amp circuits. The output voltage V_0 is feedback to the inverting input terminal through $R_f - R_1$ network where R_f is the feedback resistor. Input signal is applied to the inverting input through $R_1$and non-inverting input terminal is grounded.



Analysis:

For simplicity assume an ideal op-amp for analysis. As $V_d = 0$, node'a' is at ground potential an the current i_1 through R_1 is

$$i_1 = V_i / R_1$$

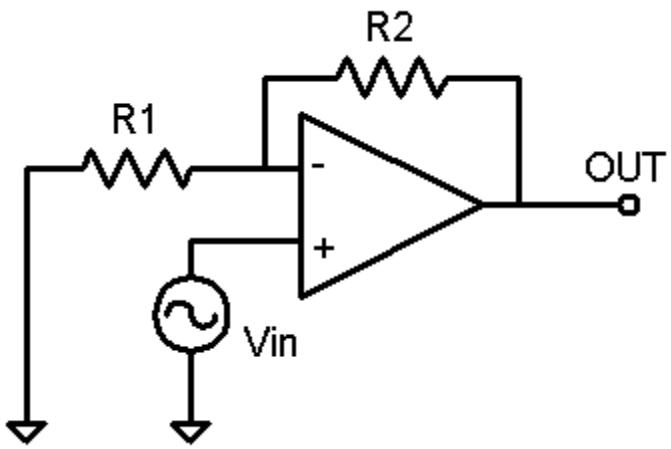
Since op-amp draws no current all the current flowing through R_1must flow through R_f. Therefore Output voltage ,

$V_0 = -i_1 R_f = -V_i R_f / R_1$

Gain $A_{CL} = V_0/V_i = -R_f/R_1$

Negative sign indicates a phase shift of 180^0 between V_i and V_0. R_1 should be kept fairly large to avoid loading effect.

Non-inverting Amplifier:



Here the signal is applied to the positive input terminal and feedback is given; the circuit amplifies without inverting the input signal hence it is called non-inverting amplifier.

The voltage at node 'a' is V_i.

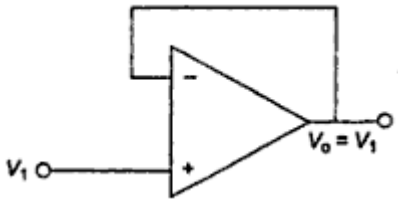
$$V_i = (V_0/R_1+R_f).R_1$$

$$V_0/V_i = (R_i+R_f)/R_1 = 1+R_f/R_1$$

i.e. $A_{CL} = 1+R_f/R_1$

The gain can be adjusted to unity or more by proper seletion of resistors R_f and R_1. Comparing with inverting amplifier the input resistance R_i is extremely large.

Voltage follower:



The output voltage follows the input voltage exactly hence the circuit is called a voltage follower. Voltage follower is obtained from the non-inverting amplifier if $R_f = 0$ and $R_1 = \infty$.

$$V_0 = V_i$$

Voltage follower is used as buffer for impedance matching. i.e. to connect a high impedance source to a low impedance load.

Op-amp Characteristics:

DC Characteristics:

Practical op-amp has some dc voltage at the output even with both the inputs are grounded. The non-ideal dc characteristics that add error components to the dc output voltage are

1. Input bias current
2. Input offset voltage
3. Input offset current
4. Thermal drift

Input bias current:

A practical op-amp conduct a small value of dc current to bias the input transistors. The base current entering into the inverting and non-inverting terminals are I_B^- and I_B^+ respectively. I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.

Input bias current I_B is defined as the average value of the base currents entering into the terminals of an op-amp.

(diagram)

i.e. $I_B = (I_B^+ + I_B^-)/2$

for 741 bipolar op-amp I_B is 500 nA and fet op-amp is 50 pA at room temperature.

Bias current compensation:

(diagram)

Input bias current can be compensated using resistor R_{comp} between the non-inverting input terminal and ground.

Current I_B^+ flowing through the resistor R_{comp} develops a voltage v_i across it.

By KVL,

$-V_1+0+V_2-V_0 = 0$

$V_0 = V_2 - V_1$

Selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and V_0 will be zero.

R_{comp} is derived as

$V_i = I_B^+ R_{comp}$

$I_B^+ = V_1/R_{comp}$

With $V_i = 0$, $I_1 = V_1/R_1$ and $I_2 = V_2/R_f$

For compensation V_0 should be zero for $V_i = 0$. i.e. $V_2 = V_1$. Therefore $I_2 = V_1/R_f$

KCL at node 'a' gives

$I_B^- = I_2 + I_1$

$= V_1/R_f + V_1/R_1$

$= V_1(R_1+R_f/R_1R_f)$

$= V_1/R_{comp}$

Or $R_{comp} = R_1R_f/R_1+R_f$ i.e. $R_1 = R_f$

Input offset current:

Bias current compensation will work id both bias currents I_B^+ I_B^- are equal. The input transistors cannot be made identical hence there will be some difference between I_B^+ and I_B^-. This difference is called offset current I_{OS}.

$|I_{OS}| = I_B^+ - I_B^-$

The absolute value indicates that there is no way to predict which of the current is larger.

I_{OS} for BJT op-amp is 200 nA and for FET is 10 pA.

Therefore $V_0 = R_fI_{OS}$

The effect of I_{OS} can be minimized by keeping feedback resistance small.

Input offset voltage:

The voltage which is required to be applied at the input for making the output voltage zero is called input offset voltage V_{OS}.

(diagram)

Equivalent circuit for $V_i = 0$:

(diagram)

The voltage V_2 at negative terminal is

$V_2 = R_1.V_0/R_1+R_f$

Or $V_0 = (R_1 +R_f)V_2/R_1 = (1+ R_f/R_1)V_2$

Since $V_{OS} = |V_i - V_2|$ and $V_i = 0$

$V_{OS} = |0 - V_2| = V_2$

Thermal drift:

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25^0 C may not remain so when the temperature rises. This is drift. Offset current drift is expressed in nA/^{0}C and offset voltage drift in mV/^{0}C.

AC Characteristics:

For small signal sinusoidal ac applications the ac characteristics such as frequency response and slew rate are to be considered.

Frequency Response:

An ideal op-amp have infinite bandwidth .i.e. if its open loop gain is 90dB. With dc signal its gain should remain the same 90dB through audio and onto high radio frequency. But practically op-amp gain decreases at high frequency. This is due to capacitive component in the equivalent circuit of op-amp. For an op-amp with only one break frequency all the capacitor effects can be represented by a single capacitor C as shown in fig.

(diagram)

There is one pole due to RC and obviously one -20dB/decade roll-off effect. The corner or break frequency is given by

$F_1 = 1/2\pi R_0 C$

$|A| = A_{OL}/(1+(f/f_1)^2)^{1/2}$

(diagram)

Slew rate:

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. for e.g. A 1V/μs slew rate means that the output rises or falls by 1V in one 1μs.

Ideal slew rate is infinite meaning that op-amp output voltage should change instantaneously in response to input step voltage. Practical op-amps have specified slew rates from 0.1V/μs to 100V/μs. Slew rate improves with higher closed loop gain and dc supply voltage.

There is usually a capacitor which prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor V_C increases is given by

$dV_C/dt = I/C$

slew rate, $SR = dV_c/dt|_{max} = I_{max}/C$

for 741 IC , $SR = I_{max}/C = 15\mu A/30pf = 0.5V/\mu s$

SR limits the response speed of all large signal wave shapes.

For e.g. consider a voltage follower whose input is large amplitude, high frequency sine wave.

(diagram)

If $V_S = V_m \sin\omega t$

Then $V_0 = V_m \sin\omega t$

The rate of change of output is given by $dV_0/dt = V_m \omega \cos\omega t$

The maximum rate of change of output occurs when $\cos\omega t = 1$.

i.e. $SR = dV_0/dt|_{max} = V_m \omega$

therefore, $SR = 2\pi f V_m$ V/s $= 2\pi f V_m/10^6$ V/μs

Summer or Adder Amplifier:

Op-amp may be designed to sum several input signals either at inverting or non-inverting input terminal. Such a circuit is called Summer or Summing amplifier.

(diagram)

A typical summing amplifier with three input voltage V_1, V_2 and V_3, three resistors R_1, R_2 and R_3 and a R_f as shown in fig.

Analysis:

Since the input bias current is assumed to be zero, there is no voltage drop across R_{comp} hence positive input terminal is at ground potential and voltage at node 'a' is zero.

By KCL the nodal equation is,

$V_1/R_1 + V_2/R_2 + V_3/R_3 + V_0/R_f = 0$

$V_0 = -\{R_f V_1/R_1 + R_f V_2/R_2 + R_f V_3/R_3\}$

Thus the output is an inverted weighted sum of inputs

If $R_1 = R_2 = R_3 = R_f$ then $V_0 = -(V_1+V_2+V_3)$

Subtractor:

(diagram)

A basic differential amplifier can be used as a subtractor as shown in fig. If all the resistors are equal in value then the output voltage can be derived using superposition principle.

To find output V_{01} due to v_1 alone put $V_2 = 0$ then the circuit becomes a non-inverting amplifier having input voltage $V_1/2$ at the positive terminal and the output becomes,

$V_{01} = V_1(1+R/R)/2 = V_1$

Similarly output due to V_2 alone is $V_{02} = -V_2$

Thus the output voltage due to both inputs can be written as

$V_0 = V_{01}+V_{02}$

$V_0= V_1 – V_2$

Differentiator:

Op-amp circuit that contains capacitor at the input is the differentiating amplifier or differentiator. The output of the differentiator is the derivative of the input.

(diagram)

Analysis:

The node N is a virtual ground potential i.e. $V_N =0$. The current through the capacitor is

$I_C = C\, d(V_i-V_N)/dt$

$= C\, dV_i/dt$

Current $i_f = V_0/R_f$

Nodal equation at node N is $C\, dV_i/dt + V_0/R_f =0$

Therefore, $V_0 = - R_f C\, dV_i/dt$

Thus the output voltage V_0 is constant ($- R_f C$) times the derivative of the input voltage V_i and the circuit is a differentiator.

Integrator:

An op-amp circuit with capacitor as the feed back element is an integrator circuit. The output waveform is the integration of the input waveform.

(diagram)

The nodal equation at node N is $V_i/R_1 + C_f\, dV_0/dt = 0$

$dV_0/dt = - V_i /R_1C_f$

integrating on both sides,

${}_0\int^t dV_0 = -1/R_1C_f\ {}_0\int^t V_i\, dt$

$V_0(t) = -1/R_1C_f\ {}_0\int^t V_i\, dt + V_0(0)$

Where $V_0(0)$ is the intial output voltage.

Comparator:

Op-amp in the open loop configuration operates in a non linear manner. Application of op-amp in this mode are comparator, detector, converters etc.

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open loop op-amp with output $\pm V_{sat}$ ($=v_{CC}$).

(diagram)

Types of comparator:

1. Non-inverting comparator
2. Inverting comparator

(diagram)

Here the output voltage is at $-V_{sat}$ for $V_i<V_{ref}$ and V_0 goes to $+V_{sat}$ for $V_i>V_{ref}$

(diagram)

In a practical circuit V_{ref} is obtained by using 10KΩ potentiometer which form a voltage divider with supply voltage V^+ and V^- with the wiper connected to negative input terminal. Thus a V_{ref} of desired amplitude and polarity can be obtained by adjusting the potentiometer.

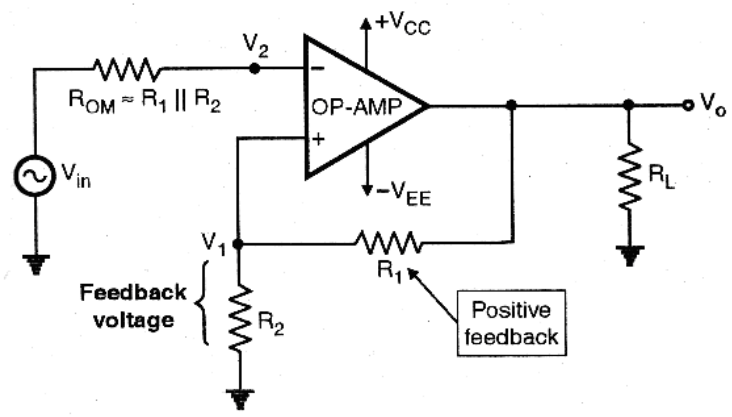
Applications of Comparator:

1. Zero crossing detector
2. Window detector
3. Time market generator
4. Phase meter

Schmitt Trigger- Regenerative Comparator:

If positive feedback is added to the comparator, gain can be increased greatly, consequently the transfer curve becomes more close to ideal curve. For practical circuits it is not possible to maintain loop gain exactly equal to unity , due to power supply & temperature variations.

Schmitt Trigger is a circuit which converts sine wave to a square wave and saw-tooth waves and saw-tooth wave into a pulse. This is also called regenerative comparator. The input voltage V_{IN} triggers (changes the state of) the output V_O every time it exceeds certain voltage levels called upper threshold voltage V_{UT} and lower threshold voltage V_{LT}.

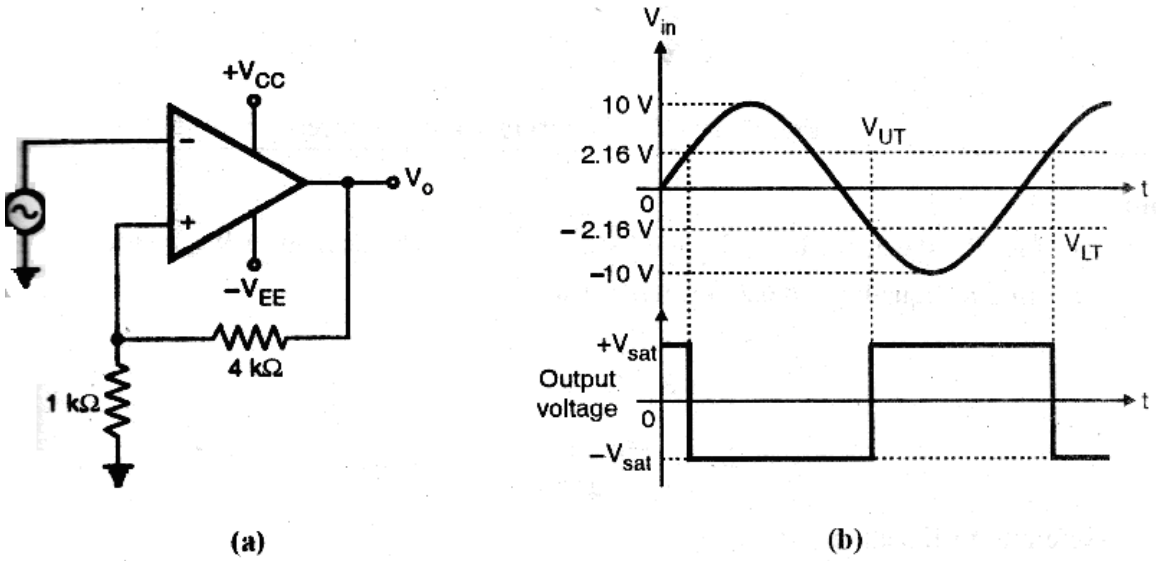


Inverting schmitt trigger using OP-AMP

5.

The threshold voltages are obtained by using the voltage divider R_1~R_2, where the voltage across R_2 is feedback to positive input.

When $V_O = +V_{SAT}$, the voltages across R_1 is called upper threshold voltage, V_{UT}. $V_{IN}>V_{SAT}$ to cause V_O to switch from $+V_{SAT}$ to $-V_{SAT}$.



6.
7.

Using voltage divider rule

$$V_{UT} = \frac{R_1}{R_1+R_2} * V_{SAT}$$

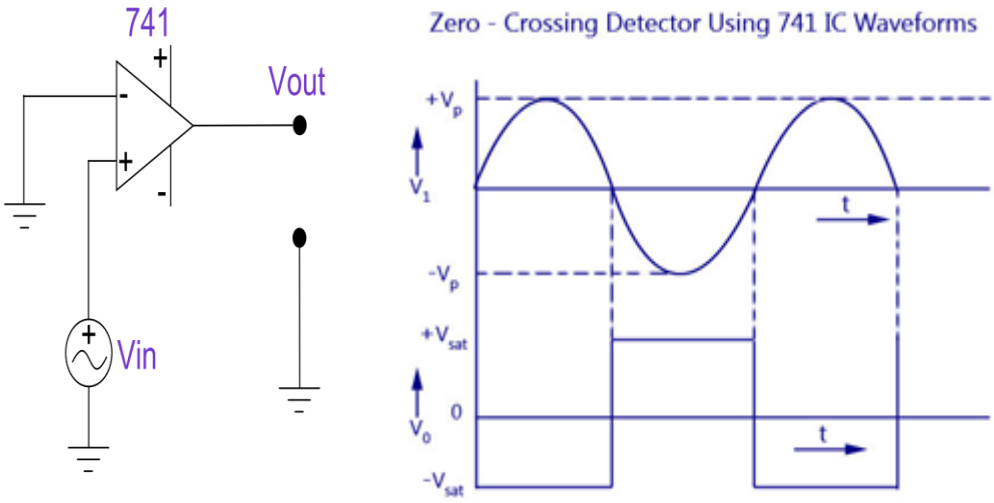
If $V_O = -V_{SAT}$, voltage across R_1 is called lower threshold voltage V_{LT}. V_{IN} must be slightly more negative than V_{LT} in order to cause V_O to switch from $-V_{SAT}$ + $+V_{SAT}$

$$V_{LT} = \frac{R_1}{R_1 + R_2} * (-V_{SAT})$$

The positive feedback because of its regenerative action will make V_O switch faster between $+V_{SAT}$ and $-V_{SAT}$. The resistance R_3 is used to minimize the offset problem.

operation of zero crossing detector and window detector circuits using op-amp.

The zero crossing detector circuit is an important application of the op-amp comparator circuit. It can also be called as the sine to square wave converter. Anyone of the inverting or non-inverting comparators can be used as a zero-crossing detector. The only change to be brought in is the reference voltage with which the input voltage is to be compared, must be made zero (Vref = 0V). An input sine wave is given as Vin. These are shown in the circuit diagram and input and output waveforms of an inverting comparator with a 0V reference voltage.



As shown in the waveform, for a reference voltage 0V, when the input sine wave passes through zero and goes in positive direction, the output voltage Vout is driven into negative saturation. Similarly, when the input voltage passes through zero and goes in the negative direction, the output voltage is driven to positive saturation. The diodes D1 and D2 are also called clamp diodes. They are used to protect the op-amp from damage due to increase in input voltage. They clamp the differential input voltages to either +0.7V or -0.7V.

In certain applications, the input voltage may be a low frequency waveform. This means that the waveform only changes slowly. This causes a delay in time for the input voltage to cross the zero-level. This causes further delay for the output voltage to switch between the upper and lower saturation levels. At the same time, the input noises in the op-amp may cause the output voltage to switch between the saturation levels. Thus zero crossing is detected for noise voltages in addition to the input voltage. These difficulties can be removed by using a regenerative feedback circuit with a positive feedback that causes the output voltage to change faster thereby eliminating the possibility of any false zero crossing due to noise voltages at the op-amp input.

8.

Window Detector

A window detector circuit or dual edge limit detector circuits is used to determine whether an unknown input is between two precise reference threshold voltages. It employs comparators to detect over-voltage or under-voltage.

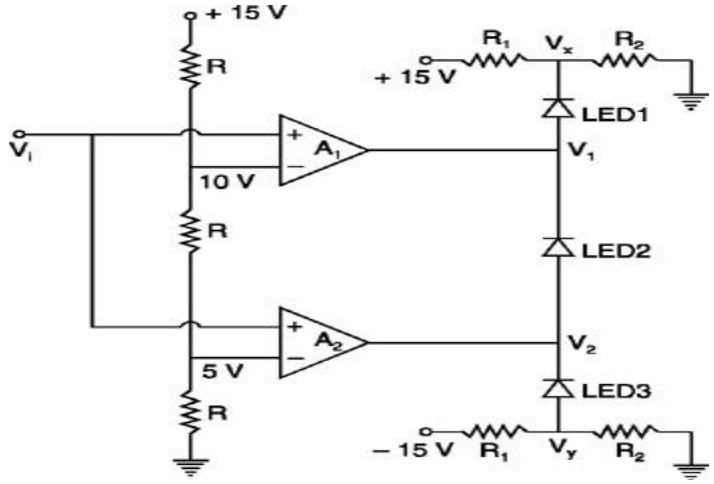
Using a single comparator, one could only have one voltage reference value: if we want to have two voltage reference values, where we could set the upper and lower voltage level limit value to determine the output, we can use the window comparator circuit.

If Vin is greater than V1 and V2 (V_{in} > 2/3 V_{cc}) then the comparator CMP1 output will swing to the logical low and make the TR2 to turn OFF (LED2 OFF), while the comparator CMP2 output will swing to the logical high, this will power the TR1 base make the TR1 to turn ON (LED1 ON).

When the Vin is less than V1 but greater than V2 ($1/3\ V_{cc} < Vin < 2/3\ V_{cc}$) then the comparator CMP1 output will swing to logical high and make the TR2 to turn ON (LED2 ON). The comparator CMP2 output also will swing to the logical high, this will provide the necessary voltage input on the TR1 base to make it ON (LED1 ON).

The last when the Vin voltage goes bellow the V1 and V2 ($Vin < 1/3\ V_{cc}$) then the comparator CMP1 output will swing to logical high and make the TR2 to turn ON (LED2 ON), while the comparator CMP2 output will swing to the logical low and make the TR1 to turn OFF (LED1 OFF).

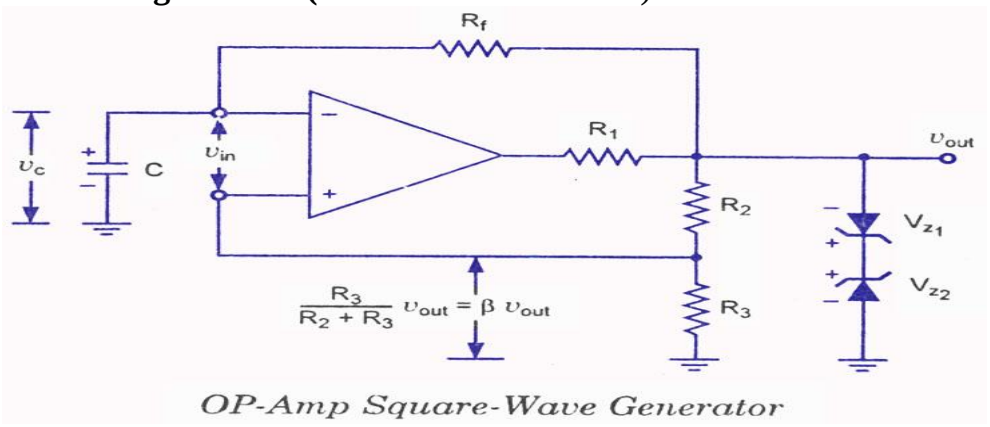
9.



10. **window detector**

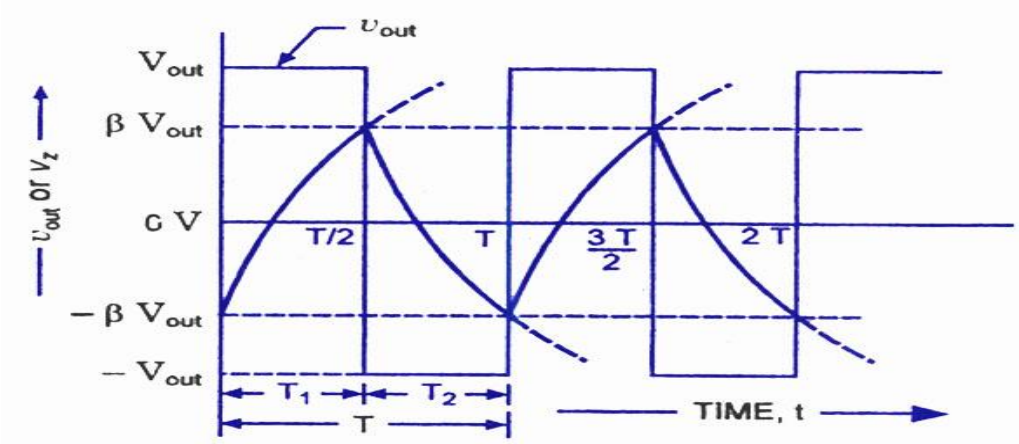
Multivibrator Circuits:

Square wave generator (Astable multivibrator)



OP-Amp Square-Wave Generator

A simple op-amp square wave generator is also called a free running oscillator. The principle of generation of square wave output is to force an op-amp to operate in the saturation region. Fraction $\beta = R2/(R1+R2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage Vref is βV_0 and may take values as $+\beta V_{sat}$ or $-\beta V_{sat}$.The output is also fed back to the (-) input terminal after integrating by means of a low pass RC combination. Whenever input at the (-) input terminal just exceeds Vref switching takes place resulting in a square wave output .In astable multivibrator, both the states are quasi stable.



Output and Capacitor Voltage Waveforms

Consider an instant of time when the output is at Vsat.The capacitor now starts charging towards +Vsat through resistance R.The voltage at the (+) input terminal is held at +βVsat by R1 and R2 combination. This condition continues as the charge on C rises until it has just exceeded +βVsat, the reference voltage .When the voltage at the (-) input terminal becomes greater than this reference volt, the output is driven to –Vsat.At this instant, the voltage on the capacitor is +βVsat.It begins to discharge through R, that is, charges more and more negatively until voltage just exceeds –βVsat .The output switches back to +Vsat.

The frequency is determined by the time it takes the capacitor to charge from –βVsat to + βVsat and vice versa.The voltage across the capacitor as a function of time is given by

$Vc(t)=Vf+(Vi-Vf)\ e^{-t/R_fC}$

Vf -final value =+Vsat

Vi-Initial value= -βVsat

$Vc(t)=Vsat+(-\beta Vsat-Vsat)\ e^{-t/R_fC}$ ---------- (1)

$Vc(t)=Vsat-Vsat(\beta+1)\ e^{-t/R_fC}$

$= Vsat(1+\beta\ e^{-t/R_fC} + e^{-t/R_fC})$

$Vc(t)=Vsc=-Vsat(1+\beta)\ e^{-t/R_fC}$ ---------- (2)

Time t= T1

Voltage across capacitor reaches + βVsat and switching takes place

$Vc(T1)=\beta Vsat$ ---------- (3)

Equating (2) & (3)

$Vsat-Vsat(1+\beta)\ e^{-t/R_fC}=\beta Vsat$

$Vsat[1-(1+\beta)\ e^{-t/R_fC}]=\beta Vsat$

$[1-(1+\beta)\ e^{-t/R_fC}]=\beta$

$[1-(1+\beta)\ e^{-T1/R_fC}]=\beta$

$(1-\beta)/(1+\beta)=e^{-T1/R_fC}$

$Ln[(1-\beta)/(1+\beta)]=T1/R_fC$

$T1=-Ln[(1-\beta)/(1+\beta)]\ R_fC$

Total time period $T=2t1=2\ R_fC\ Ln[(1-\beta)/(1+\beta)]$

R1=R2; β=0.5

$T=2\ R_fC\ ln(1.5/0.5)$

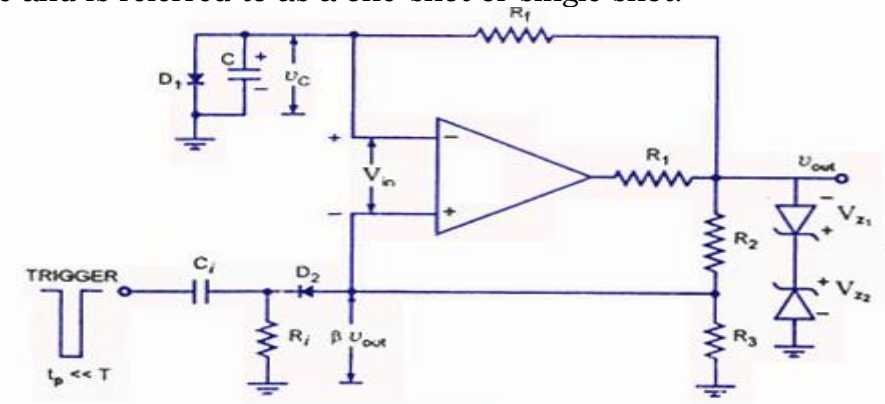
$T=2\ R_fC\ ln(3)$

If R1=1.16R2 then $T=2\ R_fC$

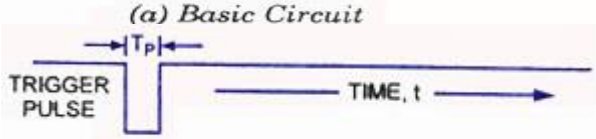
and frequency $f=1/2\ R_fC$

MONOSTABLE MULTIVIBRATOR

A **monostable multivibrator** (MMV) has one stable state and one quasi-stable state. The circuit remains in its stable state till an external triggering pulse causes a transition to the quasi-stable state. The circuit comes back to its stable state after a time period T. Thus it generates a single output pulse in response to an input pulse and is referred to as a one-shot or single shot.

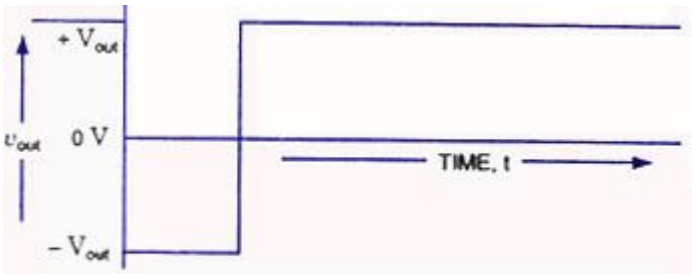


(a) Basic Circuit



(b) Negative Trigger Pulse

11.



(d) Output Waveform

Pulse Generator

Monostable multivibrator circuit illustrated in figure is obtained by modifying the astable multivibrator circuit by connecting a diode D_1 across capacitor C so as to clamp v_c at v_d during positive excursion.

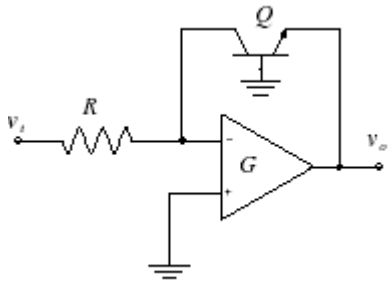
Under steady-state condition, this circuit will remain in its stable state with the output $V_{OUT} = +V_{OUT}$ or $+V_z$ and the capacitor C is clamped at the voltage V_D (on-voltage of diode $V_D = 0.7$ V). The voltage V_D must be less than βV_{OUT} for $v_{in} < 0$. The circuit can be switched to the other state by applying a negative pulse with amplitude greater than $\beta V_{OUT} - V_D$ to the non-inverting (+) input terminal.

When a trigger pulse with amplitude greater than $\beta V_{OUT} - V_D$ is applied, v_{in} goes positive causing a transition in the state of the circuit to $-V_{out}$. The capacitor C now charges exponentially with a time constant $\tau = R_fC$ toward — V_{OUT} (diode D_1 being reverse-biased). When capacitor voltage v_c becomes more negative than $-\beta V_{OUT}$,

v_{in} becomes negative and, therefore, output swings back to + V_{OUT} (steady- state output). The capacitor now charges towards + V_{OUT} till v_c attain V_D and capacitor C becomes clamped at V_D. The trigger pulse, capacitor voltage waveform and output voltage waveform are shown in figures respectively.

The width of the trigger pulse T must be much smaller than the duration of the output pulse generated i.e. T_P « T. For reliable operation the circuit should not be triggered again before T.
During the quasi-stable state, the capacitor voltage is given as
$\mathbf{v_c = -V_{OUT} + (V_{OUT} + V_D)e^{-t/\tau}}$
At instant t = T, $v_c = -\beta V_{OUT}$
So $\mathbf{-\beta V_{OUT} = -V_{OUT} + (V_{OUT} + v_D) e^{-T/\tau}}$ **or**
$\mathbf{T = R_fC \log_e (1 + V_D/V_{OUT})/ 1- \beta}$
Usually $V_D << V_{OUT}$ and if R2 = R3 so that if β = R3/(R2+R3) = ½ then,
$\mathbf{T = R_fC \log_e 2 = 0.693 R_f C}$

Logarithmic Amplifier:

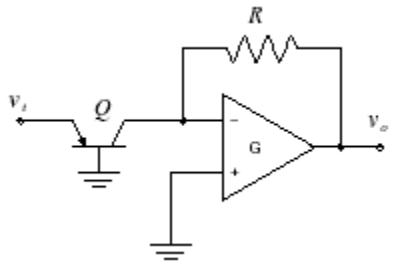


The fundamental log-amp circuit is shown in the fig.where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by
$I_E = I_S (e^{qVe/kT} - 1)$
Since $I_C = I_E$ for a grounded base transistor
$I_C = I_S (e^{qVe/kT} - 1)$
I_S = emitter saturation current = 10^{-13} A
k = Boltzman's constant
T= absolute temperature(in ^{o}K)
$I_C / I_S = e^{qVe/kT} - 1$
$e^{qVe/kT} = (I_C / I_S) + 1 \sim (I_C / I_S)$
Taking natural log on both sides
$V_E = kT / q \ln (I_C / I_S)$
also $I_C = V_i / R1$
$V_E = -V_O$
$V_O = \ln (V_i / V_{ref})$
thus output voltage is proportional to the logarithm of input voltage.
$\text{Log}_{10} X = 0.4343 \ln X$

The drawback of this circuit is I_S varies from transistor to transistor and with temperature, hence a stable reference voltage V_{Ref} can't be obtained. This be eliminated by applying reference voltage to another amplifier.

The input is applied to one log-amp while a reference voltage is applied to another log-amp. The 2 transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

Antilog Amplifier:



The input V_i is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. the output V_O of the anti-log amplifier is fed back to the inverting input of A_1 through resistor R_1. V_{BE} of transistor Q_1 and Q_2 can be given by

$V_{Q1BE} = kt/q \ln(V_O / R_1 I_S)$ and

$V_{Q2BE} = Kt/q \ln(V_{ref} / R_1 I_S)$

since the base is tied to ground

$V_A = -V_{Q1} = — Kt/q \ln(V_O / R_1 I_S)$

base voltage of Q_2

$$V_B = \frac{R_{TC}}{R_2 + R_{TC}} V_i$$

Emitter Voltage

$V_E = V_B + V_{Q2}$

But the emitter voltage of Q_2 is V_A

Ie $V_A = V_E$

$$\frac{-kT}{q} \ln (V_O / R_1 I_S) = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln(V_{ref} / R_1 I_S)$$

(or)

$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = \frac{-kT}{q} \left(\ln \frac{V_O}{R_1 I_S} - \ln \frac{V_{ref}}{R_1 I_S} \right)$$

$V_O = V_{ref} 10^{-kVi}$

Thus an increase of input by one volt causes the output to decrease by a decade.

Instrumentation Amplifiers

1. Instrumentation Amplifier constructed using three Op-Amps as shown in Fig 5.1
2. Op-Amps A_1 and A_2 are connected basically, in noninverting amplifier configuration.
3. The only change is that instead of grounding inverting terminals of both Op-Amps as in noninverting configuration), they are connected to resistor R_G
4. Effectively, the inverting terminals of Op-Amp A_1 is fed a voltage V_I through R_G and the inverting terminal of Op-Amp A_2 is fed by a voltage V_2 through R_G. This is obvious by virtual ground concept.

Fig 5.1. Basic instrumentation amplifier with three Op-Amps.

Derivation for Output Voltage

As per the superposition theorem, the output of A_1 (Vo′)and A_2 (Vo′′) is given below

$$V_O' = \left(1 + \frac{R_2}{R_G}\right) V_1 - \frac{R_2}{R_G} V_2 \qquad \ldots (5.1)$$

$$V_O'' = \left(1 + \frac{R_2}{R_G}\right) V_2 - \frac{R_2}{R_G} V_1 \qquad \ldots (5.2)$$

The output of two op-amps (A_1 and A_2) are applied to the input of differential amplifier. Therefore, the final output of the instrumentation amplifier is written as follows

Output $V_O = \frac{R_f}{R_1}(V_O'' - V_O')$ . . . (5.3)

Substituting the equations (5.2) and (5.1) in equation (5.3)

$$V_o = \frac{R_f}{R_1}\left(\left(\left(1+\frac{R_2}{R_G}\right)V_2 - \frac{R_2}{R_G}V_1\right) - \left(1+\frac{R_2}{R_G}\right)V_1 + \frac{R_2}{R_G}V_2\right)$$

$$= \frac{R_f}{R_1}\left(\left(\left(1+\frac{R_2}{R_G}\right)(V_2 - V_1) + \frac{R_2}{R_G}(V_2 - V_1)\right)\right)$$

$$= \frac{R_f}{R_1}(V_2 - V_1)\left(\left(1+\frac{R_2}{R_G}\right) + \frac{R_2}{R_G}\right)$$

$$\boxed{V_O = \frac{R_f}{R_1}(V_2 - V_1)\left(\left(1+\frac{2R_2}{R_G}\right)\right)}$$ . . . (5.4)

The gain may be adjusted by varying resistance R_G

Features of Instrumentation Amplifier

1. High gain accuracy

2. High CMRR
3. High gain stability with low temperature coefficient
4. Low DC offset
5. Low output impedance

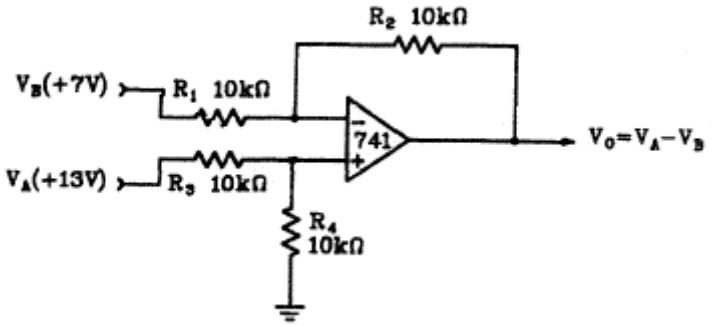
Applications of Instrumentation Amplifier

1) Data acquisition from low output transducers;
2) Medical instrumentation;
3) current/voltage monitoring;
4) Audio applications involving weak audio signals or noisy environments;
5) High-speed signal conditioning for video data acquisition and imaging

8. Explain with circuit and relevant equations the following op-amp applications.

a) Subtractor b) Differentiator c) Non-inverting amplifier.

Subtractor:



A basic differential amplifier can be used as a subtractor as shown in fig. If all the resistors are equal in value then the output voltage can be derived using superposition principle.

To find output V_{01} due to v_1 alone put $V_2 = 0$ then the circuit becomes a non-inverting amplifier having input voltage $V_1/2$ at the positive terminal and the output becomes,

$V_{01} = V_1(1+R/R)/2 = V_1$

Similarly output due to V_2 alone is $V_{02} = -V_2$

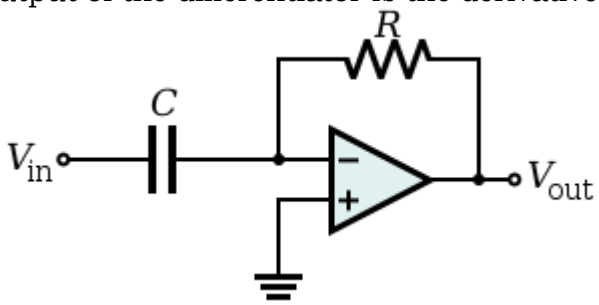
Thus the output voltage due to both inputs can be written as

$V_0 = V_{01}+V_{02}$

$V_0 = V_1 - V_2$

b)Differentiator:

Op-amp circuit that contains capacitor at the input is the differentiating amplifier or differentiator. The output of the differentiator is the derivative of the input.



Analysis:

The node N is a virtual ground potential i.e. V_N =0. The current through the capacitor is

$I_C = C\, d(V_i - V_N)/dt$

$= C\, dV_i/dt$

Current $i_f = V_0/R_f$

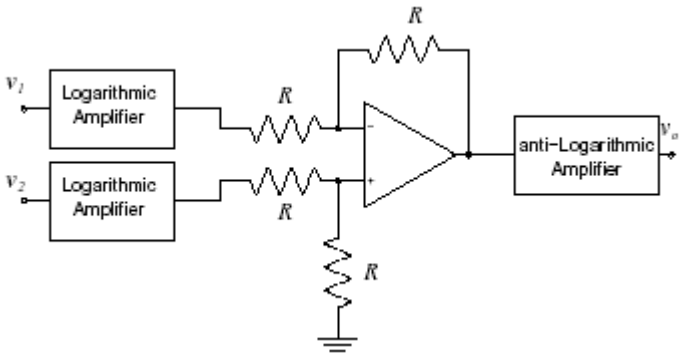
Nodal equation at node N is $C\, dV_i/dt + V_0/R_f = 0$

Therefore, $V_0 = - R_f\, C\, dV_i/dt$

Thus the output voltage V_0 is constant (- R_f C) times the derivative of the input voltage V_i and the circuit is a differentiator.

Multiplier:

A basic multiplier with 2 input signals V_x and V_y is shown below. The output is the product of 2 inputs divided by a reference voltage $V_{ref.}$



ie $V_O = V_xV_y / V_{ref}$

V_{ref} = 10 volts hence $V_O = V_xV_y / 10$

As long as $V_x < V_{ref}$ and $V_y < V_{ref}$ then the output of the multiplier will not saturate.

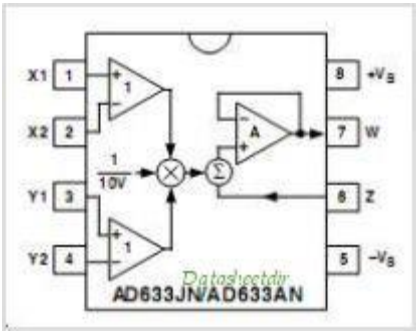
If both inputs are positive, IC is said to be 1 quadrant multiplier. 2 quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative then IC is a 4 quadrant multiplier.

One commonly used technique to make multiplier circuit is log-antilog method. The log-antilog method relies on the mathematical relationship that the sum of 2 numbers equals the log of product of those numbers.

$(\ln V_x + \ln V_y) = \ln(V_xV_y)$

Four-Quadrant Analog Multiplier

The **AD633** is a functionally complete, four-quadrant, Analog Multiplier It includes high impedance, differential X and Y inputs and a high impedance summing input (Z). The low impedance output voltage is a nominal 10 V full scale provided by a buried Zener. The **AD633** is the first product to offer these features in modestly priced 8-lead plastic DIP and SOIC packages
The **AD633** is laser calibrated to a guaranteed total accuracy of 2% of full scale. Nonlinearity for the Y-input is typically less than 0.1% and noise referred to the output is typically less than 100 V rms in a 10 Hz to 10 kHz bandwidth. A 1 MHz band-10V width, 20 V/s slew rate, and the ability to drive capacitive loads make the **AD633** useful in a wide variety of applications where simplicity and cost are key concerns.
The **AD633** 's versatility is not compromised by its simplicity. The Z-input provides access to the output Buffer Amplifier abling the user to sum the outputs of two or more multipliers, the multiplier gain, convert the output voltage to a rent, and configure a variety of applications.
AD633 is available in an 8-pin plastic mini-DIP package (N) and 8-pin SOIC (R) and is specified to operate over the 0C to +70C commercial temperature range.



Applications of multiplier:

The AD633 is well suited for such applications as modulation and demodulation, automatic gain control, power measurement, voltage-controlled amplifiers, and frequency doublers.

Multiplier connections

Figure 11 shows the basic connections for multiplication. The X and Y inputs normally have their negative nodes grounded, but they are fully differential, and in many applications, the grounded inputs may be reversed (to facilitate interfacing with signals of a particular polarity while achieving some desired output polarity), or both may be driven.

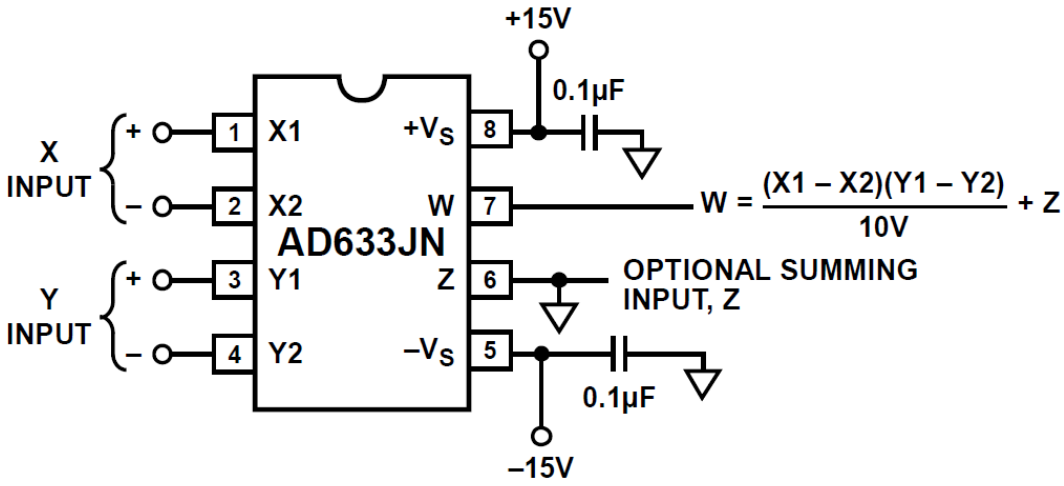


Figure 11. Basic Multiplier Connections

Squaring and frequency doubling

As shown in Figure 12, squaring of an input signal E is achieved simply by connecting the X and Y inputs in parallel to produce an output of $E^2/10$ V. The input can have either polarity, but the output is positive. However, the output polarity can be reversed by interchanging the X or Y inputs. The Z input can be used to add a further signal to the output.

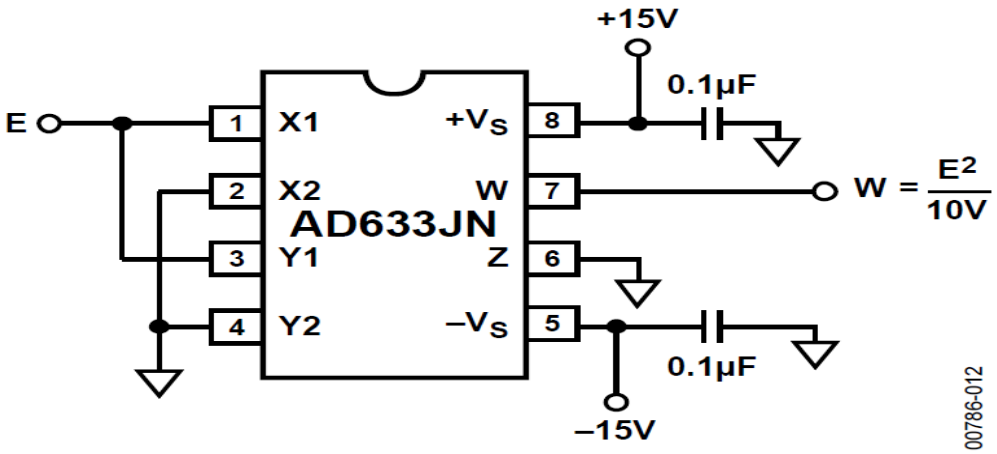


Figure 12. Connections for Squaring

When the input is a sine wave E sin ωt, this squarer behaves as a frequency doubler, because

$$\frac{(E \sin \omega t)^2}{10\ V} = \frac{E^2}{20\ V}(1 - \cos 2\,\omega t) \qquad (2)$$

Equation 2 shows a dc term at the output that varies strongly with the amplitude of the input, E. This can be avoided using the connections shown in Figure 13, where an RC network is used to generate two signals whose product has no dc term. It uses the identity

$$\cos\theta \sin\theta = \frac{1}{2}(\sin 2\theta) \qquad (3)$$

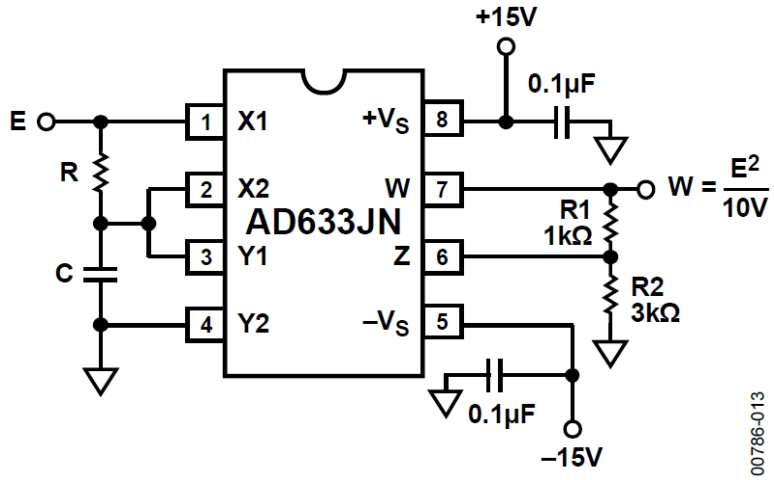


Figure 13. Bounceless Frequency Doubler

At ωo = 1/CR, the X input leads the input signal by 45° (and is attenuated by √2), and the Y input lags the X input by 45° (and is also attenuated by √2). Becausee the X and Y inputs are 90° out of phase, the response of the circuit is (satisfying Equation 3)

$$W = \frac{1}{(10\,V)}\frac{E}{\sqrt{2}}\left(\sin \omega_0 t + 45°\right)\frac{E}{\sqrt{2}}\left(\sin \omega_0 t + 45°\right)$$

$$= \frac{E^2}{(40\,V)}\left(\sin 2\,\omega_0 t\right) \qquad (4)$$

which has no dc component. Resistors R1 and R2 are included to restore the output amplitude to 10 V for an input amplitude of 10 V.
The amplitude of the output is only a weak function of frequency; the output amplitude is 0.5% too low at ω = 0.9 ω0 and ω0 = 1.1 ω0.

Generating inverse functions

Inverse functions of multiplication, such as division and square rooting, can be implemented by placing a multiplier in the feedback loop of an op amp. Figure 14 shows how to implement square rooting with the transfer function for the condition E < 0.

$$W = \sqrt{-(10E)V} \qquad (5)$$

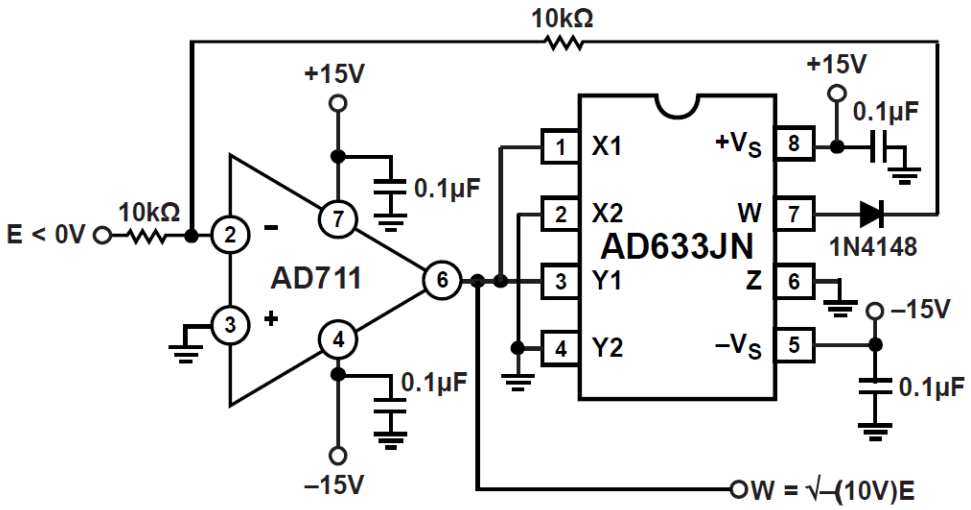


Figure 14. Connections for Square Rooting

Likewise, Figure 15 shows how to implement a divider using a multiplier in a feedback loop. The transfer function for the divider is

$$W' = -(10\ V)\frac{E}{E_X} \qquad (6)$$

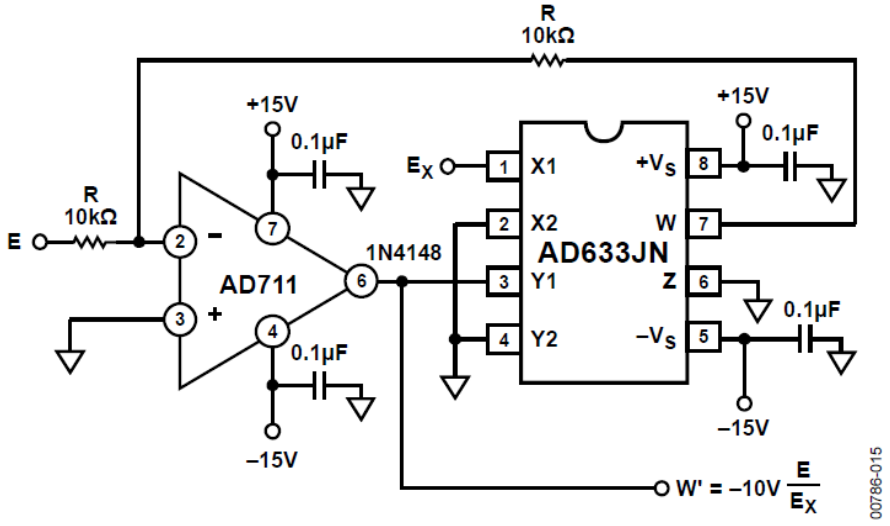


Figure 15. Connections for Division

UNITII

Other LICs and Data Converters

Other LICs and Data Converters: 555 timer – Block diagram and features – Astable Multivibrator – Applications - Square wave oscillator, Ramp generator, Triangular waveform generator and Voltage to frequency converter – Monostable Multivibrator – applications - Frequency divider.
PLL565, Principle, Building blocks – Applications – Frequency multiplication, Frequency translation, AM and FM detection.
Data converters – DAC characteristics – Binary weighted DAC, R-2R DAC, Monolithic DAC-08– ADC characteristics–Flash ADC, Successive Approximation ADC, Dual slope integrating type ADC.

555 TIMER

- The 555 timer is a highly stable device for generating accurate time delay or oscillation
- A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

Pin diagram

- It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply voltage, the 555 timer is versatile (can be used AC as well as DC) and easy to use in various applications.
- Fig.1 shows the 8 Pin package

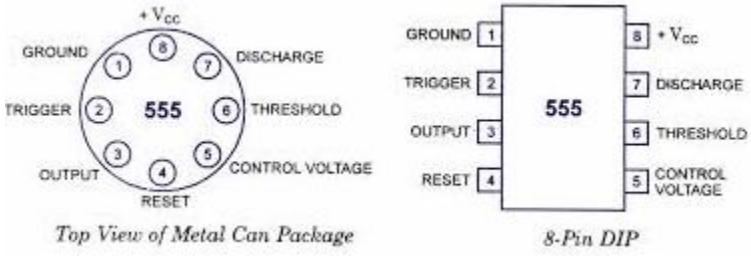


Fig 1 IC 555 pin package

Applications of IC 555

Various applications include

1. Oscillator,
2. Pulse generator,
3. Ramp and Square Wave Generator',
4. Mono-shot multivibrator,
5. Burglar alarm, Traffic light control and
6. Voltage monitor etc.

Functional Diagram of IC 555

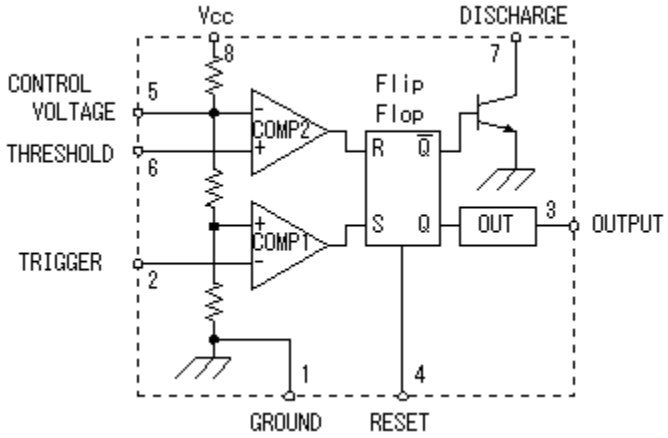


Fig 2. The functional diagram for 555 IC timer.

- The figure 2 The functional diagram for 555 IC timer consist of 3hree 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) VCC to the upper comparator (UC) and (1/3) VCC to the lower comparator (LC), where V, is the supply voltage.
- Since these two voltages fix the threshold voltage for each comparator and these voltages are also determining the timing interval.
- It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5).
- In applications where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 pF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

Operation of IC 555

- In the stable state, the output Q of the flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter.
- If negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. VCC / 3), now the trigger passes through (VCC / 3), the output of the lower comparator goes HIGH and sets the FF (Q = 1, = 0).
- when the threshold voltage at pin 6 passes through (2/3) VCC , the output of the upper comparator goes HIGH and resets the FF (Q = 0, =1).
- The reset input (pin 4) is used to reset the FF and the flip flop output becomes HIGH and the output of IC 555 becomes LOW because the output of FF is 1.

MONOSTABLE MULTIVIBRATOR:

- Monostable Multivibrator is also known as One Short Multivibrator.
- As its name indicates it has one stable state and it switches to unstable state for a predetermined time period T when it is triggered.

- The time period T is determined by the RC time constant in the circuit.
- Monostable mode of 555 Timer is commonly used for generating Pulse Width Modulated

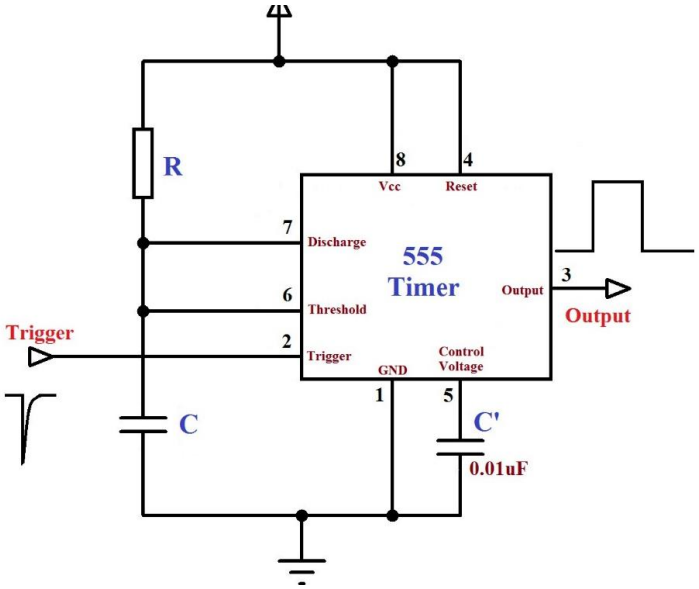


Fig 3. Monostable Multivibrator using 555 Timer

- This is the circuit diagram of 555 Timer shown in figure 3 wired in Monostable mode.
- 8^{th} pin and 1^{st} pin of the 555 timer are used to given power Vcc and Ground respectively.
- 4^{th} pin is the Reset pin of 555 Timer, which is active low so it is connected to Vcc to avoid accidental resets.
- 5^{th} pin is the Control Voltage pin used to provide external reference voltage to internal comparators.
- Since it is not used here, it is grounded via a capacitor C' (0.01μF) to avoid high frequency noises.
- When a negative trigger is applied on the Trigger input of 555, output goes high and capacitor starts charging through resistor R.
- When the capacitor voltage becomes greater than 2/3 Vcc, ouput goes low and capacitor starts discharging through the Discharge pin of 555 Timer.
- Time period of the unstable state is given the tye expression, T = 1.1RC.

Working

- The Internal Block Diagram of IC555 shown in figure 4
- The Monostable Multivibrator will be in its stable state (Output LOW) until it is triggered.
- When a negative trigger is applied to the Trigger pin of 555 Timer, output of lower comparator will become HIGH and output of upper comparator will be LOW, since the capacitor voltage is zero. This makes the output HIGH.
- The Discharge transistor turns OFF and the capacitor starts charges through resistor R to Vcc.
- After the negative trigger, output of lower comparator becomes LOW and that of upper

comparator remains LOW. Since both inputs of the SR Flip Flop are LOW, output will not change, so the output is HIGH.

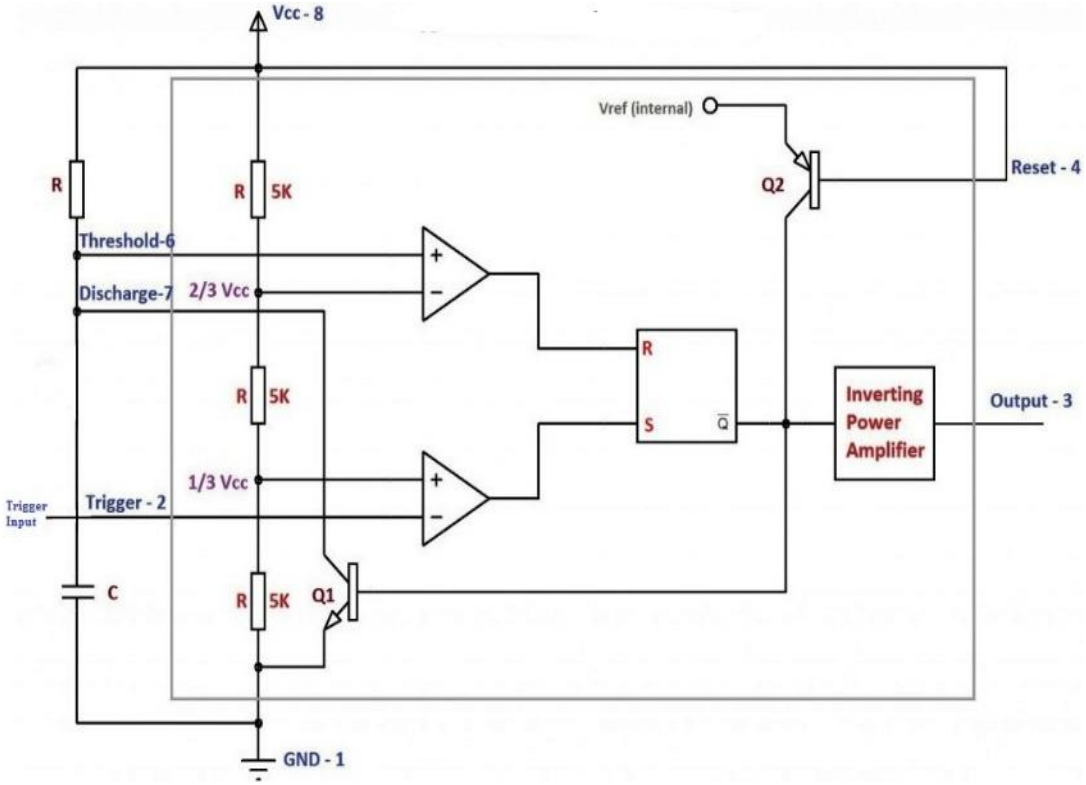


Fig 4: Internal diagram of IC 555

- When the capacitor voltage will become greater than 2/3 Vcc, output of upper comparator becomes HIGH and that of lower comparator remains LOW, so the output
- becomes LOW.
- This turns ON the discharge transistor and the capacitor discharges.
- The circuit remains in its stable state (Output LOW) until next trigger occurs.

Design

- Time Period, T = 1.1RC

Frequency Divider

- Fig 5 shows a monostable multivibrator circuit which is used as frequency divider by continuously triggered.
- This trigger signal is the input of the circuit, this signal frequency is divided based the time period of the circuit. In general, time period of the circuit is adjusted to be longer (time period is longer means, frequency is less (f = 1/T)).

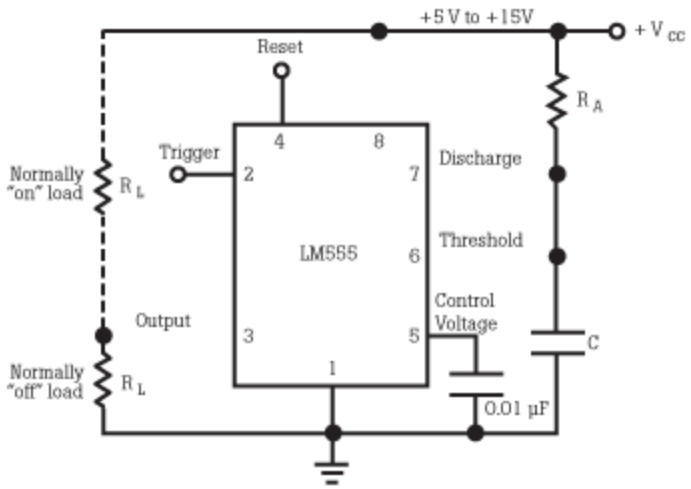


Fig 5 monostable Multivibrator used as frequency divider

- The monostable multivibrator will be triggered by the first negative going edge of the square wave input as shown in Fig 6 but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in **Fig. 10**.
- The mono-shot *w*ill however be triggered on the third negative going input, depending on the choice of the time delay, the output can be made fractions of the frequency of the input triggering square wave.

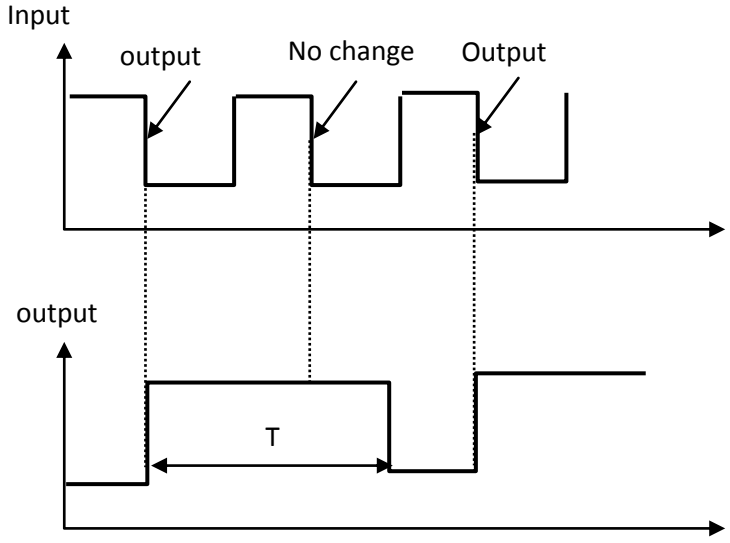


Fig 6 Input and output waveform of frequency division

Pulse Width Modulation

The circuit for pulse width modulation is shown in Fig. 7.

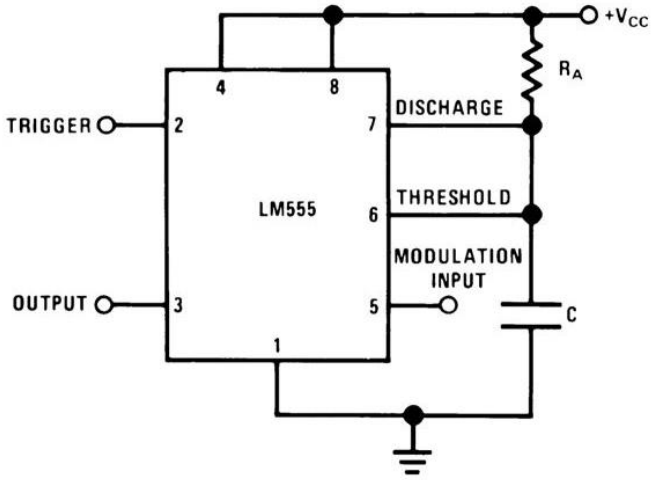


Fig 7 Pulse width modulator circuit

- This is basically a monostable multivibrator with a modulating input signal applied at pin-5.
- By applying of continuous trigger at pin-2, a series of output pulses are obtained at the pin 3, the duration of which depends on the modulating input at pin-5.
- The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V,. at the inverting input terminal of UC.
- This in turn changes the threshold level of the UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig 8

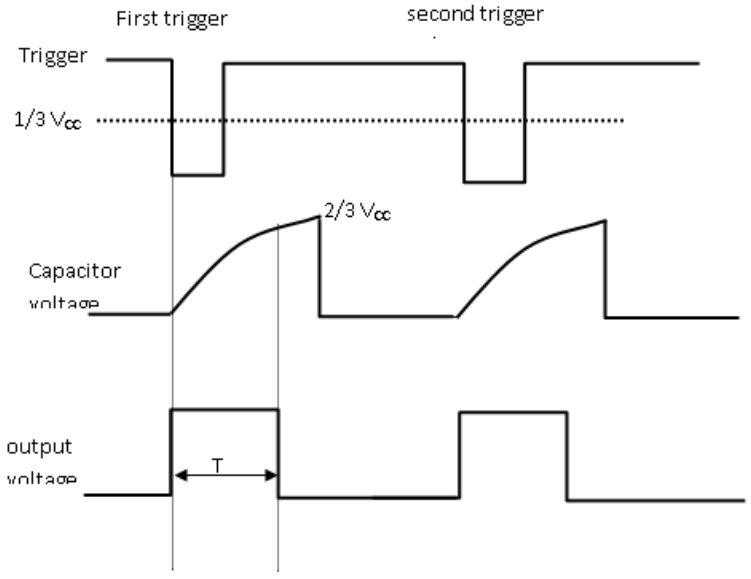


Fig 8. Output waveform of PWM

ASTABLE MULTIVIBRATOR

The astable multivibrator circuit using timer IC is shown in the fig 9

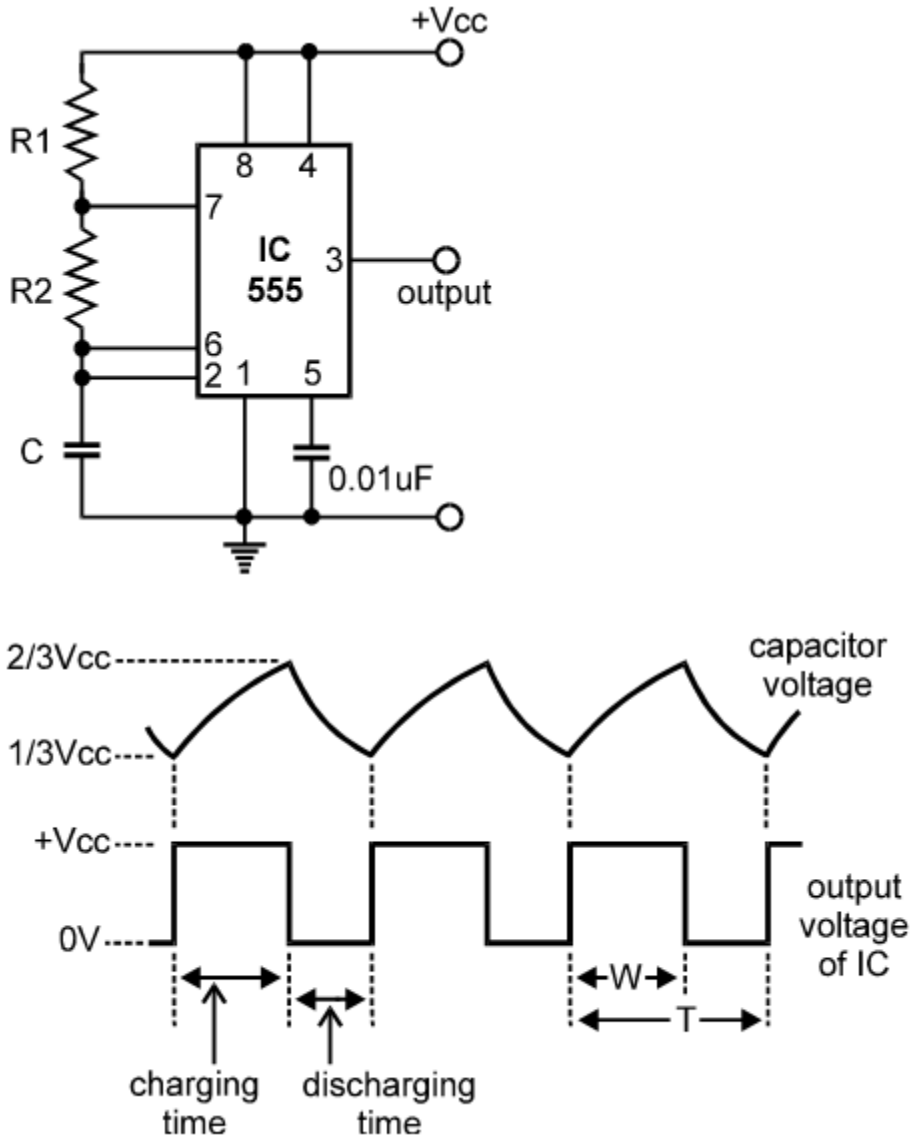
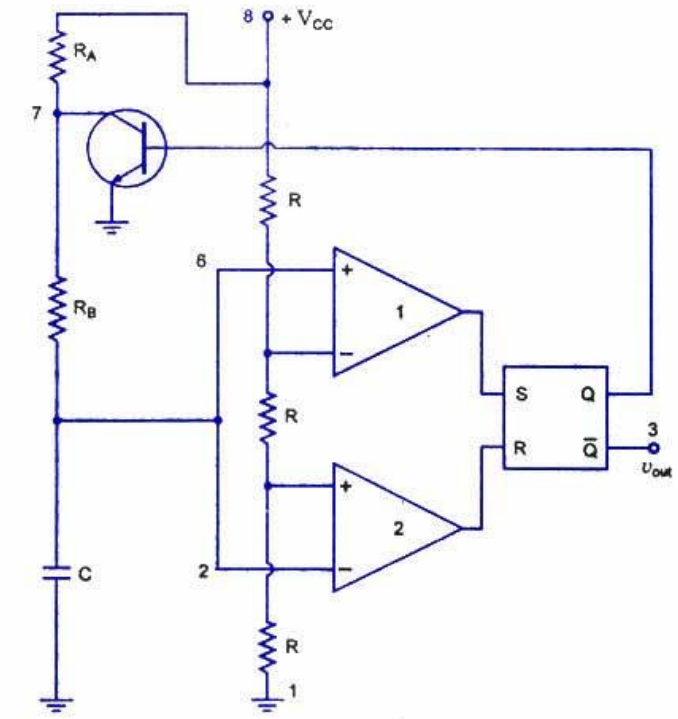


Fig. 9.Astable multivibrator using 555 timer

Astablemultivibrator using IC 555

- The Fig 10.shows the Functional diagram of astable multivibrator using 555 timer
- Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q, is connected to the Junction of R_A and R_B.



Internal Circuitry With External Connections

Fig 10 Functional diagram of astablemultivibrator using 555 timer

- When the power supply V_{CC} connected, the external timing capacitor C charges towards V_{CC} at time constant $(R_A + R_B)$ C.
- During this time, output (pin 3) is high (equals V_{CC}) as Reset R = 0, Set S =1 and this combination makes Q = 0 which has unclamped the timing capacitor C.
- When the capacitor voltage equals and is just greater than (2/3)V_{CC} the upper comparator triggers the flip-flop with the input condition R=1 and S=0, so the output of FF is Q=0 and $\overline{Q}$ =1.
- This $\overline{Q}$ = 1, is given to the input of transistor and make the transistor Q_1 on and capacitor C starts discharging towards ground through R_B and transistor Q_I with a time constant R_BC (neglecting the forward resistance of Q_1).
- Current also flows into transistor Q_I through R_A. Resistors $R_A$and $R_B$must be large enough to limit this current and prevent damage to the discharge transistor Q_I.
- During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) V_{CC}/3, the lower comparator is triggered

- Now the lower comparator makes *S = 1, R = 0,* which turns Q = 0. Now Q = 0 unclamps the external timing capacitor C, The capacitor C is thus periodically charged and discharged between (2/3)V_{CC} and (1/3)V_{CC} respectively.

Output Waveform

- Figure 11 shows the timing sequence and capacitor voltage wave form.
- The length of time that the output remains HIGH is the time for the capacitor to charge from (1 / 3) V_{CC} to (2 / 3) V_{CC}.

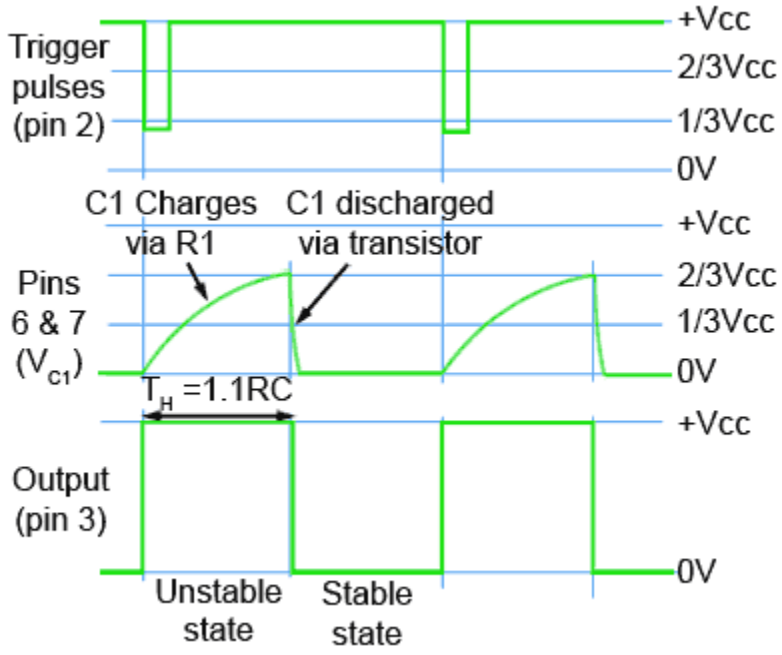


Fig 11.Timing sequence of astablemultivibrator

Derivation for frequency of Oscillation

<u>At time t_1</u>

The capacitor voltage for a *RC* circuit subjected to a step input of V_{CC} volts is given by

$$V_c = V(1 - e^{-t/RC})$$

The time t_l taken by the circuit to charge from 0 to (2/3) V_{CC} is,

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-t_1/RC})$$

$$\frac{2}{3} = (1 - e^{-t_1/RC})$$

Take ln on both sides

$$t_1 = RC \ln\left(\frac{2}{3}\right)$$

$$t_1 = 1.09RC$$

At time t_2

During the time t_2 , the circuit to charge from 0 to (2/3) V_{CC} is,

$$\frac{1}{3}V_{CC} = V_{CC}(1-e^{-t_2/RC})$$

$$\frac{1}{3} = (1-e^{-t2/RC})$$

Taking ln on both sides

$$t_2 = RC\ln\left(\frac{1}{3}\right)$$

$$t_1 = 0.405RC \qquad \ldots (2.3)$$

So the time to charge from (1/3) V_{CC} to (2/3) V_{CC} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09RC - 0.405RC = 0.69RC$$

so the given circuit, the capacitor is charged through R_A and R_B

$$t_{HIGH} = 0.69(R_A+R_B)C$$

The output is low while the capacitor discharges from (2/3) V_{CC} to (1/3) V_{CC} and the voltage across the capacitor is given by

$$\frac{1}{3}V_{CC} = \frac{2}{3}V_{CC}(1-e^{-t/RC})$$

Solving the above equation, we get

$$t = 0.69RC$$

For the given circuit, $t_{LOW} = 0.69RC$ . . . (2.4)

The resistor R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore the total time period

$$T = t_{HIGH} + t_{LOW}$$

$$T = 0.69(R_A + R_B)c + 0.69R_BC$$

$$= 0.69R_AC + 0.69R_Bc + 0.69R_BC$$

$$= 0.69(R_A + 2R_B)C$$

Frequency of oscillation $f = \frac{1}{T}$

$$f = \frac{1}{0.69(R_A + 2R_B)C}$$

$$f = \frac{1.45}{(R_A + 2R_B)C}$$

Applications Astable Mode

1. FSK generator
2. Pulse-position Modulator

PHASE LOCKED LOOP IC 565

Block diagram of IC 765

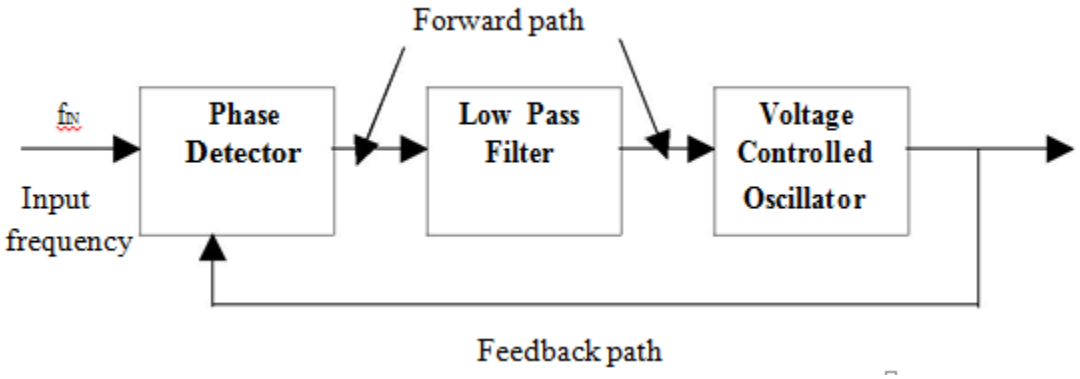


Fig 12 IC 565 Block diagram

Phase locked loop construction and operation:

- The block diagram of PLL IC 765 shown in figure 12 consists of i) Phase detector ii) LPF iii) VCO. The phase detector or comparator compares the input frequency fIN with feedback frequency f_{OUT}.
- The output of the phase detector is proportional to the phase difference between f_{IN}&f_{OUT}. The output of the phase detector is a dc voltage & therefore is often referred to as the error voltage.
- The output of the phase detector is then applied to the LPF, which removes the high frequency noise and produces a dc level. This dc level in turn, is input to the VCO.
- The output frequency of VCO is directly proportional to the dc level. The VCO frequency is compared with input frequency and adjusted until it is equal to the input frequencies.
- PLL goes through 3 states, i) free running ii) Capture iii) Phase lock.
- Before the input is applied, the PLL is in free running state. Once the input frequency is applied the VCO frequency starts to change and PLL is said to be in the capture mode. The VCO frequency continuous to change until it equals the input frequency and the PLL is in phase lock mode.
- When Phase locked, the loop tracks any change in the input frequency through its

repetitive action. If an input signal vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output vo of the VCO.

- If the two signals differ in frequency of the incoming signal to that of the output vo of the VCO. If the two signals differ in frequency and/or phase, an error voltage ve is generated.
- The phase detector is basically a multiplier and produces the sum (fs + fo) and difference (fs - fo) components at its output
- . The high frequency component (fs + fo) is removed by the low pass filter and the difference frequency component is amplified then applied as control voltage vc to VCO.
- The signal vc shifts the VCO frequency in a direction to reduce the frequency difference between fs and fo.
- Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency.
- The circuit is then said to be locked. Once locked, the output frequency fo of VCO is identical to fs except for a finite phase difference φ.
- This phase difference φ generates a corrective control voltage vc to shift the VCO frequency from f0 to fs and thereby maintain the lock.
- Once locked, PLL tracks the frequency changes of the input signal.
- Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Capture range: the range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of fo.
Pull-in time: the total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

(a) Phase Detector:

- Phase detector compares the input frequency and VCO frequency and generates DC voltage i.e., proportional to the phase difference between the two frequencies.
- Depending on whether the analog/digital phase detector is used, the PLL is called either an analog/digital type respectively.
- Even though most monolithic PLL integrated circuits use analog phase detectors.

- Ex for Analog: Double-balanced mixer
- Ex for Digital: Ex-OR, Edge trigger, monolithic Phase detector.

Ex-OR Phase Detector:

- This uses an exclusive OR gate. The output of the Ex-OR gate is high only when fIN or fOUT is high.The DC output voltage of the Ex-OR phase detector is a function of the phase difference between its two outputs.
- The maximum dc output voltage occurs when the phase difference is Π radians or180 degrees. The slope of the curve between 0 or Π radians is the conversion gain kp of the phase detector for eg; if the Ex-OR gate uses a supply voltage Vcc = 5V, the conversion gain Kp is K_p = 5V/Π = 1.59V / RAD

Edge Triggered Phase Detector:

- Advantages of Edge Triggered Phase Detector over Ex-OR are

i) The dc output voltage is linear over 2Π radians or 360 degrees, but in Ex-OR it is Π radians or 180 degrees.

ii) Better Capture, tracking & locking characteristics.

- Edge triggered type of phase detector using RS Flip – Flop. It is formed from a pair of cross coupled NOR gates.
- RS FF is triggered, i.e, the output of the detector changes its logic state on the positive edge of the inputs fIN &fOUT

b) Low pass filter

- The function of the LPF is to remove the high frequency components in the output of the phase detector and to remove the high frequency noise.
- LPF controls the characteristics of the phase locked loop. i.e, capture range, lock ranges, bandwidth

Lock range(Tracking range):

- The lock range is defined as the range of frequencies over which the PLL system follows the changes in the input frequency fIN.

Capture range:

- Capture range is the frequency range in which the PLL acquires phase lock. Capture range is always smaller than the lock range.

Filter Bandwidth:

- Filter Bandwidth is reduced, its response time increases. However reduced Bandwidth reduces the capture range of the PLL. Reduced Bandwidth helps to keep the loop in lock through momentary losses of signal and also minimizes noise.

c) Voltage Controlled Oscillator (VCO):

- The third section of PLL is the VCO shown in figure 13; it generates an output frequency that is directly proportional to its input voltage. The maximum output frequency of NE/SE 566 is 500 Khz

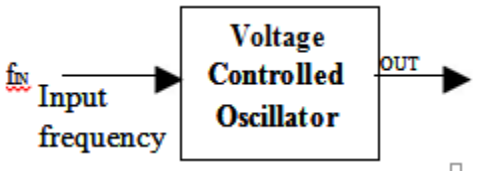


Figure 13 VCO

Feedback path and optional divider:

- Most PLLs also include a divider between the oscillator and the feedback input to the phase detector to produce a frequency synthesizer.
- A programmable divider is particularly useful in radiotransmitter applications, since a large number of transmit frequencies can be produced from a single stable, accurate, but expensive, quartz crystal–controlled reference oscillator.

- Some PLLs also include a divider between the reference clock and the reference input to the phase detector.

- If this divider divides by M, it allows the VCO to multiply the reference frequency byN / M. It might seem simpler to just feed the PLL a lower frequency, but in some cases the reference frequency may be constrained by other issues, and then the reference divider is useful.

- Frequency multiplication in a sense can also be attained by locking the PLL to the 'N'th harmonic of the signal.

- The equations governing a phase-locked loop with an analog multiplier as the phase detector may be derived as follows.

- Let the input to the phase detector be *xc*(*t*) and the output of the voltage-controlled oscillator (VCO) is *xr*(*t*) with frequency ω*r*(*t*), then the output of the phase detector *xm*(*t*)is given by

$$x_m(t) = x_c(t) \cdot x_r(t)$$

the VCO frequency may be written as a function of the VCO input *y*(*t*) as

$$\omega_r(t) = \omega_f + g_v y(t)$$

where*gv* is the *sensitivity* of the VCO and is expressed in Hz / V.

Hence the VCO output takes the form

$$x_r(t) = A_r \cos\left(\int_0^t \omega_r(\tau)\, d\tau\right) = A_r \cos(\omega_f t + \varphi(t))$$

$$\varphi(t) = \int_0^t g_v y(\tau)\, d\tau$$

The loop filter receives this signal as input and produces an output

$xf(t) = F\text{filter}(xm(t))$

where*F*Filter is the operator representing the loop filter transformation.

When the loop is closed, the output from the loop filter becomes the input to the VCO thus

$y(t) = xf(t) = F\text{filter}(xm(t))$

We can deduce how the PLL reacts to a sinusoidal input signal:

$xc(t) = Ac\sin(\omega ct)$.

The output of the phase detector then is:

$$x_m(t) = A_c \sin(\omega_c t) A_r \cos(\omega_f t + \varphi(t)).$$

This can be rewritten into sum and difference components using trigonometric identities:

$$x_m(t) = \frac{A_c A_f}{2} \sin(\omega_c t - \omega_f t - \varphi(t)) + \frac{A_c A_f}{2} \sin(\omega_c t + \omega_f t + \varphi(t))$$

As an approximation to the behaviour of the loop filter we may consider only the difference frequency being passed with no phase change, which enables us to derive a small-signal model ofthe phase-locked loop. If we can make $\omega_f \approx \omega_c$, then the $\sin(\cdot)$can be approximated by its argument resulting in: $y(t) = x_f(t) \simeq -A_c A_f \varphi(t)/2$. The phase-locked loop is said to be *locked* if this is the case.

FREQUENCY MULTIPLIER:

- Frequency divider is inserted between the VCO & phase comparator. Since the output of the divider is locked to the f_{IN}, VCO is actually running at a multiple of the input frequency.
- The desired amount of multiplication can be obtained by selecting a proper divide-by-N network, where N is an integer shown in figure 14

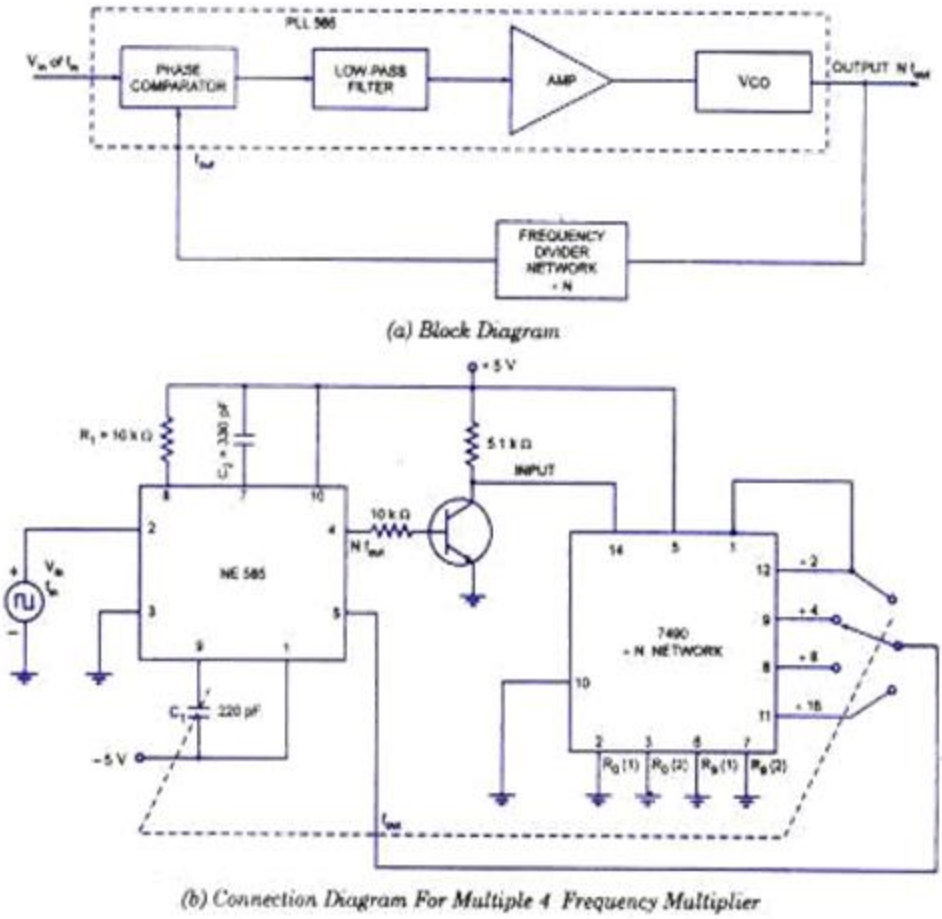


Figure 14. FM generation

AM DEMODULATION:

- A PLL may be used to demodulate AM signals as shown in the figure 15. The PLL is locked to the carrier frequency of the incoming AM signal.
- The output of VCO which has the same frequency as the carrier, but un modulated is fed to the multiplier.
- Since VCO output is always 90^0 before being fed to the multiplier. This makes both the signals applied to the multiplier and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF.
- Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

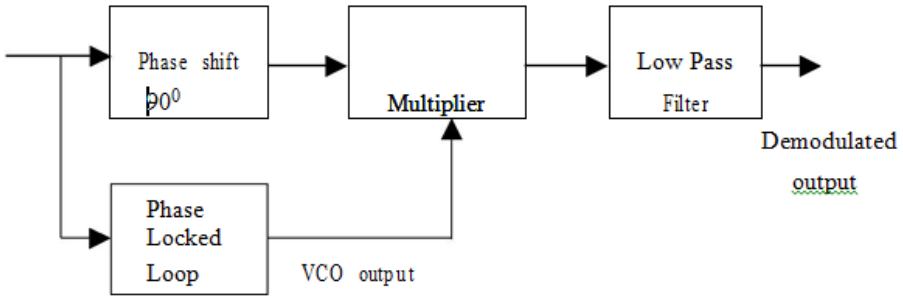


Figure 15 AM demodulation

FM DEMODULATION

- If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output.
- The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

DATA CONVERTERS

- Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form.
- Analog signals are difficult to process, store and transmit without introducing error. Therefore for processing, transmission and storage purpose, it is often convenient to express these variable in digital form.
- It gives better accuracy and reduces noise. The operation of any digital communication is based upon analog to digital converters and digital to analog D/A converters are available with wide range of specifications specified by manufacturer.
- Some of the important specifications of data converter are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

Resolution:

- Resolution is defined as the number of different analog output voltage levels that can be provided by a DAC. Or alternatively resolution is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input. Simply, resolution is the value of LSB.

Resolution (Volts) = $Vo_{FS} / (2^n - 1) = 1$ LSB increment Where 'n' is the number of input bits

'Vo_{FS}' is the full scale output voltage.

Eg:

Resolution for an 8 – bit DAC for example is said to have

→8 – bit resolution

→A resolution of 0.392 of full-Scale (1/255)

→A resolution of 1 part in 255.

Thus resolution can be defined in many different ways.

The following table shows the resolution for 6 to 16 bit DACs

S.No.	Bits	Intervals	LSB size (% of full-scale)	LSB size (For a 10 V full-scale)
1.	6	63	1.588	158.8 mV
2.	8	255	0.392	39.2 mV
3.	10	1023	0.0978	9.78 mV
4.	12	4095	0.0244	2.44 mV
5.	14	16383	0.0061	0.61 mV
6.	16	65535	0.0015	0.15 mV

Accuracy:

- Absolute accuracy is the maximum deviation between the actual converter output and the ideal converter output.
- The ideal converter is the one which does not suffer from any problem.
- Whereas, the actual converter output deviates due to the drift in component values, mismatches, aging, noise and other sources of errors.

- The relative accuracy is the maximum deviation after the gain and offset errors have been removed.

- Accuracy is also given in terms of LSB increments or percentage of full-scale voltage. Normally, the data sheet of a D/A converter specifies the relative accuracy rather than absolute accuracy.

Linearity:

- Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale.
- The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output. An ideal D/A converter produces equal increments or step sizes at output for every change in equal increments of binary input.

Monotonicity:

- A Digital to Analog converter is said to be monotonic if the analog output increases for an increase in the digital input.
- A monotonic characteristics is essential in control applications. Otherwise it would lead to oscillations. If a DAC has to be monotonic, the error should be less than ± (1/2) LSB at each output level. Hence all the D/A converters are designed such that the linearity error satisfies the above condition.

- When a D/A Converter doesn't satisfy the condition described above, then, the output voltage may decrease for an increase in the binary input.

Conversion Time:

- It is the time taken for the D/A converter to produce the analog output for the given binary input signal.
- It depends on the response time of switches and the output of the Amplifier. D/A converters speed can be defined by this parameter. It is also called as setting time.

Settling time:

- It is one of the important dynamic parameter. It represents the time it takes for the output to settle within a specified band ± (1/2) LSB of its final value following a code change at the input (Usually a full-scale change).
- It depends on the switching time of the logic circuitry due to internal parasitic capacitances and inductances.
- A typical settling time ranges from 100 ns to 10 μs depending on the word length and type of circuit used.

Stability:

- The ability of a DAC to produce a stable output all the time is called as Stability.
- The performance of a converter changes with drift in temperature, aging and power supply variations.
- So all the parameters such as offset, gain, linearity error & monotonicity may change from the values specified in the datasheet.
- Temperature sensitivity defines the stability of a D/A converter.

DIGITAL TO ANALOG CONVERSION

- A DAC converts an abstract finite-precision number (usually a fixed-point binary number) into a concrete physical quantity (e.g., a voltage or a pressure).
- In particular, DACs are often used to convert finite-precision time series data to a continually-varying physical signal.
- A typical DAC converts the abstract numbers into a concrete sequence of impulses that are then processed by a reconstruction filter using some form of interpolation to fill in data between the impulses.
- Other DAC methods (e.g., methods based on Delta-sigma modulation) produce a pulse-density modulated signal that can then be filtered in a similar way to produce a smoothly-varying signal.
- By the Nyquist–Shannon sampling theorem, sampled data can be reconstructed perfectly provided that its bandwidth meets certain requirements (e.g., a baseband signal with bandwidth less than the Nyquist frequency).
- However, even with an ideal reconstruction filter, digital sampling introduces quantization that makes perfect reconstruction practically impossible.
- Increasing the digital resolution (i.e., increasing the number of bits used in each sample) or

introducing sampling dither can reduce this error.

- DACs are at the beginning of the analog signal chain, which makes them very important to system performance. The most important characteristics of these devices are:

- **Resolution**: This is the number of possible output levels the DAC is designed to reproduce. This isusually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 (2^1) levels while an 8 bit DAC is designed for 256 (2^8) levels.
- Resolution is related to the **effective number of bits**(ENOB) which is a measurement of the actual resolution attained by the DAC.

- **Maximum sampling frequency**:This is a measurement of the maximum speed at which theDACs circuitry can operate and still produce the correct output.

- As stated in the Nyquist–Shannon sampling theorem, a signal must be sampled at over twice the frequency of the desired signal.

- For instance, to reproduce signals in all the audible spectrum, which includes frequencies of up to 20 kHz, it is necessary to use DACs that operate at over 40 kHz. The CD standard samples audio at 44.1 kHz, thus DACs of this frequency are often used.

- A common frequency in cheap computer sound cards is 48 kHz—many work at only this frequency, offering the use of other sample rates only through (often poor) internal resampling.

- **Monotonicity**:This refers to the ability of a DAC's analog output to move only in the directionthat the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

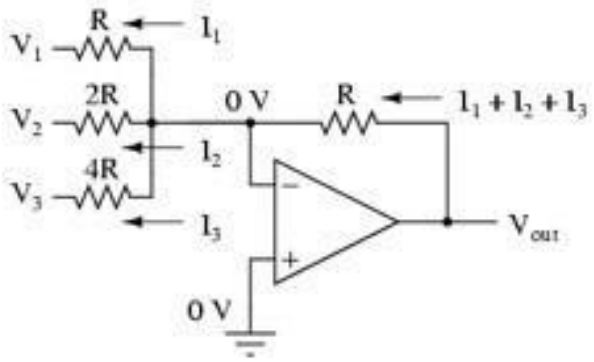
- **THD+N**: This is a measurement of the distortion and noise introduced to the signal by the DAC. Itis expressed as a percentage of the total power of unwanted harmonic HYPERLINK "http://en.wikipedia.org/wiki/Distortion" distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

- **Dynamic range**:This is a measurement of the difference between the largest and smallest signalsthe DAC can reproduce expressed in decibels. This is usually related to DAC resolution and noisefloor.

- Other measurements, such as phase distortion and sampling period instability, can also be very important for some applications.

BINARY-WEIGHTED RESISTOR DAC

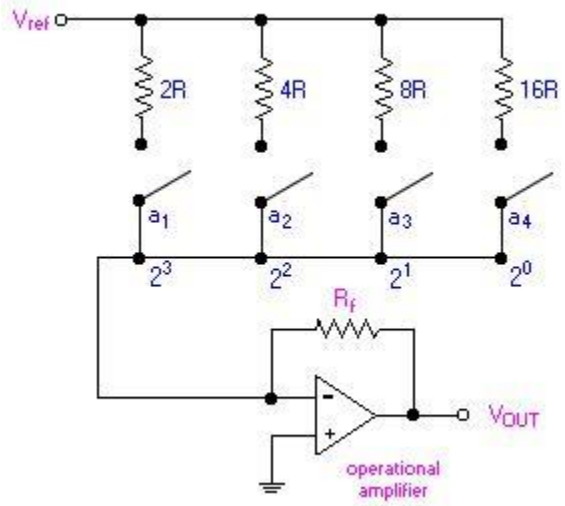
- The binary-weighted-resistor DAC employs the characteristics of the inverting summer Op Amp circuit.
- In this type of DAC, the output voltage is the inverted sum of all the input voltages. If the input resistor values are set to multiples of two: 1R, 2R and 4R, the output voltage would be equal to the sum of V1, V2/2 and V3/4. V1 corresponds to the most significant bit (MSB) while V3 corresponds to the least significant bit (LSB).



$$V_{out} = -(V_1 + \frac{V_2}{2} + \frac{V_3}{4})$$

Figure 16. Binary-Weighted Resistor Dac

The circuit for a 4-bit DAC using binary weighted resistor network is shown below:



- The binary inputs, ai (where i = 1, 2, 3 and 4) have values of either 0 or 1. The value, 0, represents an open switch while 1 represents a closed switch.

- The operational amplifieris used as a summing amplifier, which gives a weighted sum of the binary input based on the voltage, Vref.

- For a 4-bit DAC, the relationship between Vout and the binary input is as follows:

$$
\begin{aligned}
V_{OUT} &= -iR_f \\
&= -\left[V_{ref}\left(\frac{a_1}{2R}+\frac{a_2}{4R}+\frac{a_3}{8R}+\frac{a_4}{16R}\right)\right]R_f \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2}+\frac{a_2}{4}+\frac{a_3}{8}+\frac{a_4}{16}\right) \\
&= -\frac{V_{ref}R_f}{R}\left(\frac{a_1}{2^1}+\frac{a_2}{2^2}+\frac{a_3}{2^3}+\frac{a_4}{2^4}\right)
\end{aligned}
$$

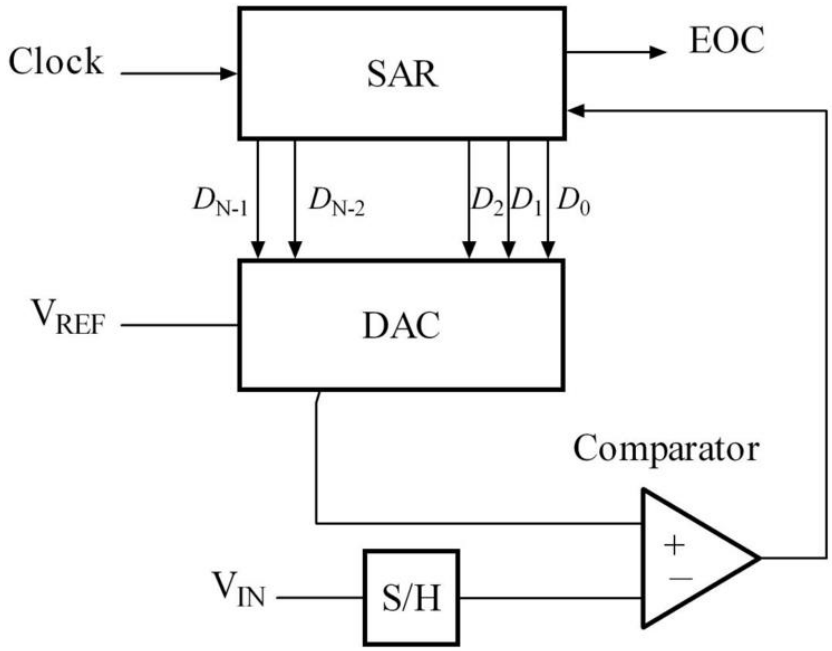
- The negative sign associated with the analog output is due to the connection to a summing amplifier, which is a polarity-inverting amplifier. When a signal is applied to the latter type of amplifier, the polarity of the signal is reversed (i.e. a + input becomes -, or vice versa).
- For a n-bit DAC, the relationship between Vout and the binary input is as follows:

$$V_{OUT} = -\frac{V_{ref}R_f}{R}\sum_{i=1}^{n}\frac{a_i}{2^i}$$

Successive Approximation Converter

The successive approximation Analog to digital converter circuit typically consists of four sub-circuits:

1. A sample and hold circuit to acquire the input voltage (V_{in}).
2. An analog voltage comparator that compares V_{in} to the output of the internal DAC and outputs the result of the comparison to the successive approximation register (SAR).
3. A successive approximation register subcircuit designed to supply an approximate digital code of V_{in} to the internal DAC.
4. An internal reference DAC that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with V_{in}.



Circuit Operation

- The successive approximation register is initialized so that the most significant bit (MSB) is set to binary bit - 1.
- This code is fed into the DAC which then supplies the analog equivalent of this digital code ($V_{ref}/2$) into the comparator circuit for comparison with the sampled input voltage.
- If this analog voltage exceeds V_{in} the comparator causes the SAR to reset this bit and set the next bit to a digital 1.
- If it is lower then the bit is left a 1 and the next bit is set to 1. This binary search continues until every bit in the SAR has been tested.

- The resulting code is the digital approximation of the sampled input voltage and is finally output by the ADC at the end of the conversion (EOC).

Successive approximation conversion sequence for typical analog input

Correct digital representation ,	*Successive approximation register output Vd at different stages in the conversion*	*Comparator output*
11010100	*10000000*	*1 (initial output)*
	11000000	*1*
	11100000	*0*
	11010000	*1*
	11011000	*0*
	11010100'	*1*
	11010110	*0*
	11010101	*0*
	1 1 0 1 0 1 0 0	

2.5.5 THE PARALLEL COMPARATOR OR FLASH ADC

- This is the possible A/D convertor. It is at the same time, the fastest and most expensive technique. Figure 2.19 shows the 3-bit A/D convertor.
- The circuit consists of a resistive divider network, 8 op-amp comparators and a 8-line encoder(3-bit priority encoder) The comparator and its ruth table is shown in figure 2.20, at each node of the resistive divider network, a comparison voltage is available.
- Since all the resistors are of equal value, the voltage levels available at the nodes are equally divided between refernce voltage V_r and the ground.
- The purpose of the circuit is to compare the analog input voltage Va with each of the node voltages. The truth table for flash type AD converter is shown in figure 2.1.
- The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially.
- Typical conversion time is 100 ns or less. Conversion time is limited only by the speed of the comparator and of the priority encoder. By using an Advanced Micro AMD 686A comparator and a T1147 priority encoder, conversion delays of the order of 20ns can be obtained.
- This type of ADC has the disadvantage that the number of comparators required is almost doubles for each added bit.
- A 2-bit ADC requires a 3 comparators , 3-bit ADC needs 7,whereas 4-bit requires 15 comparators.
- In general,the number of comparators required are 2^n-1 where n is the desired number of bits.
- Hence the number of comparators approximately doubles for each added bit. Also the larger

the value of n, the more complex is the priority encoder.

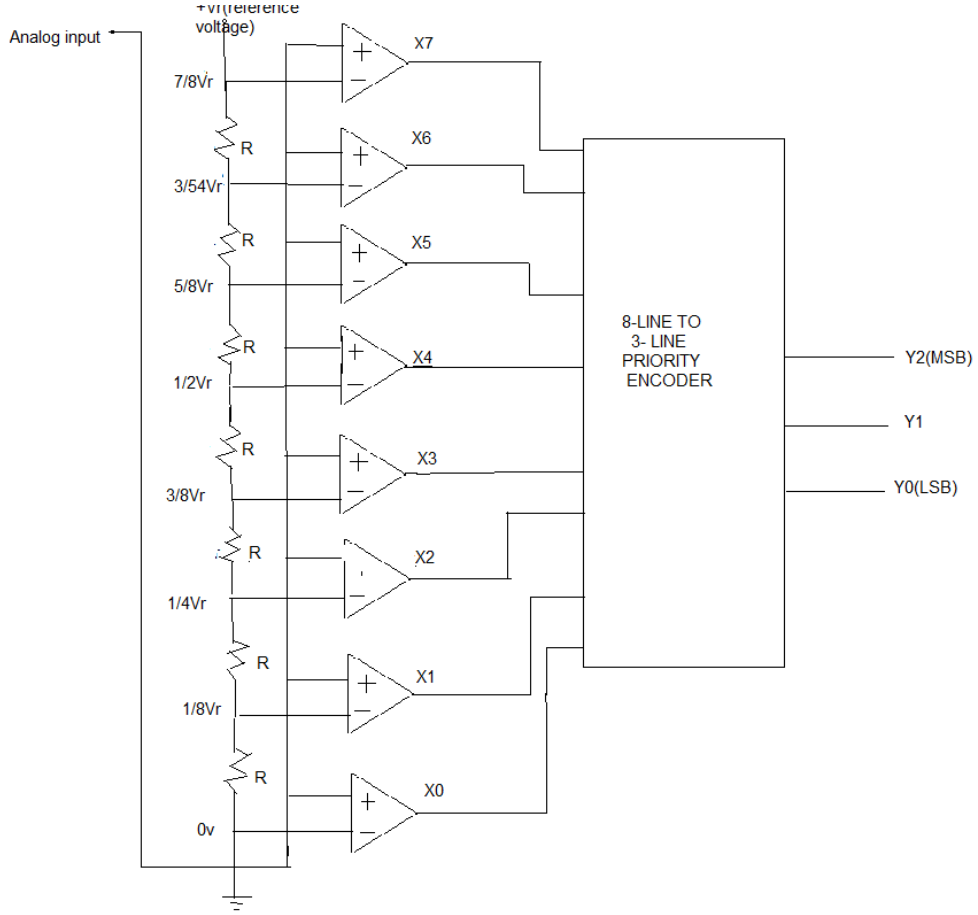
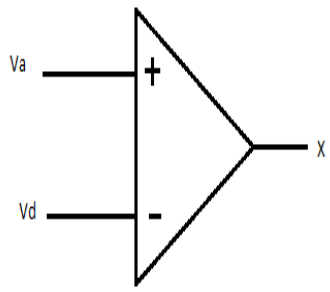


Fig 2.19 Basic circuit of flash type ADC



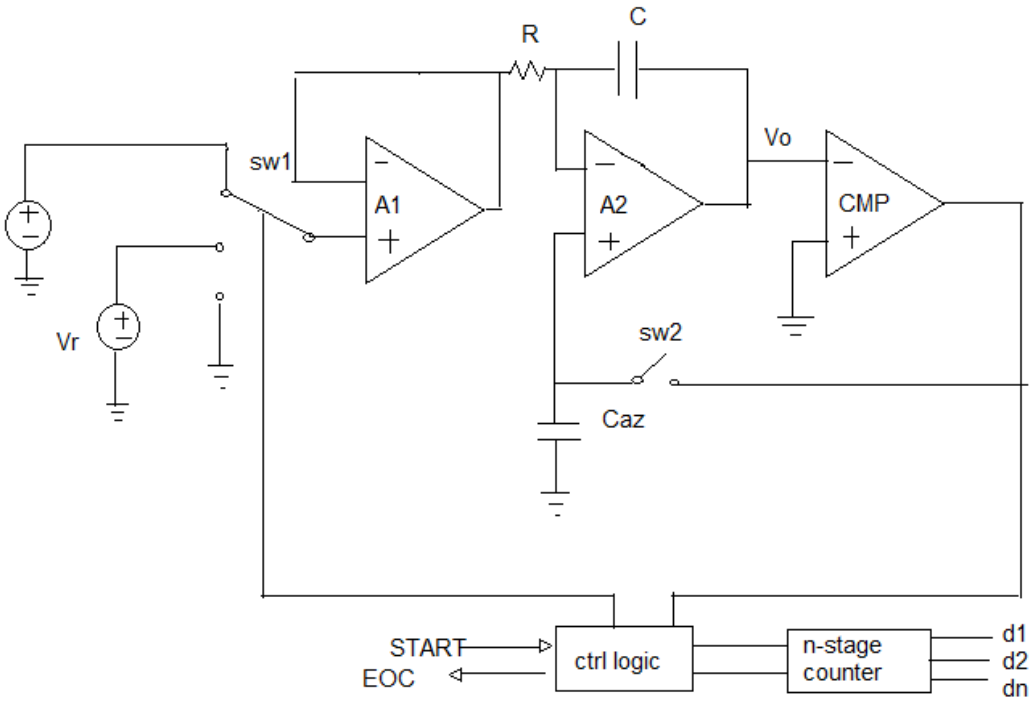
Voltage input	Logic input X
Va>Vd	X=1
Va<Vd	X=0
Va=Vd	Previous value

Fig 2.20 Comparator and its truth table

Table 2.1 Truth table for a flash type ADC

Input Voltage Va	X7	X6	X5	X4	X3	X2	X1	X0	Y2	Y1	Y0
0 to Vr/8	0	0	0	0	0	0	0	1	0	0	0
Vr/8 to Vr/4	0	0	0	0	0	0	1	1	0	0	1
Vr/4 to 3Vr/8	0	0	0	0	0	1	1	1	0	1	0
3Vr/8 to Vr/2	0	0	0	0	1	1	1	1	0	1	1
Vr/2 to 5Vr/8	0	0	0	1	1	1	1	1	1	0	0
5Vr/8 to 3Vr/4	0	0	1	1	1	1	1	1	1	0	1
3Vr/4 to 7Vr/8	0	1	1	1	1	1	1	1	1	1	0
7Vr/8 to vr	1	1	1	1	1	1	1	1	1	1	1

DUAL SLOPE ADC



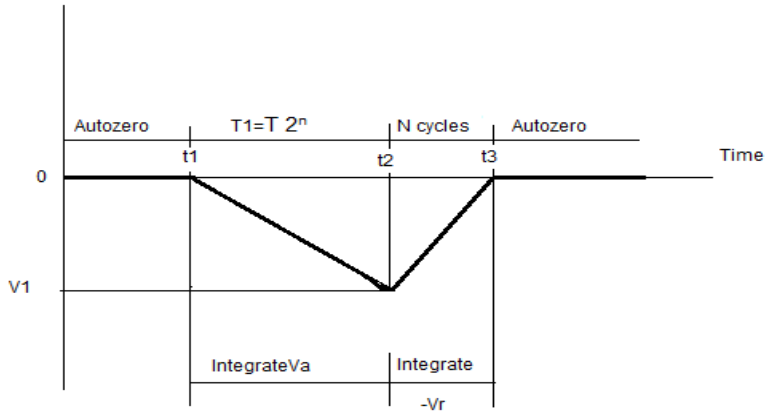


Fig 2.21(a) funtional diagram of Dual slope ADC b) Integrated ouput waveform for the dual slope ADC

- Figure 2.21 shows the functional diagram of the dual slope or dual ramp converter. The analog part of the circuit consists of the high input impedance
- The converter first integrates the analog input signal Va for a fixed duration of 2^n clock periods as shown in figure 2.21. Then it integrates an internal reference voltage V of opposite polarity until the integrator output is zero.
- The number N of clock cycles required to return the integrator to zero is proportional to h value of Va averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows,
- Before the START command arrives, the switch is connectd to ground and S_{W2} is closed. Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across capacitor c_{az} till the threshold of the comparator is acheived.
- The capacitor C_{az} thus provides the automatic compensation for the input offset voltages of all the three amplifiers. Later when S_{w2} opens, C_{az} acts as a memory to hold th voltage required to keep the offset nulled.
- At the arrival of the START command at $t=t_1$, the control logic opens S_{w2} and connects s to Va and enables starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulse place for a time $T_1 = 2^n \times T$ and the output is a ramp going downloads as shown in 2.21.
- The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage ($-V_R$). The output voltage v_o will now have a positive slope. As long as v_o is negative, the output of the comparator is positive and the control logic allows the clock pulse to be counted. However, when v_o becomes just zero at time $t=t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog input voltage V_a.

In fig 2.21

$T_1=t_2-t_1=(2^n$ counts)/clock rate

$t_2-t_1=$ digital count N/clock rate

For an integrator,

$$\Delta v_o=(-1/RC)\, V(\Delta t)$$

The voltage v_o will be equal to v_1 at the instant t_2 and can be written as

$$v_1=(-1/RC)V_a(t_2-t_1)$$

The voltage v_1 is also given by

$$v_1=(-1/RC)(-V_R)(t_2-t_3)$$

so, $v_a(t_2-t_1)=V_R(t_3-t_2)$

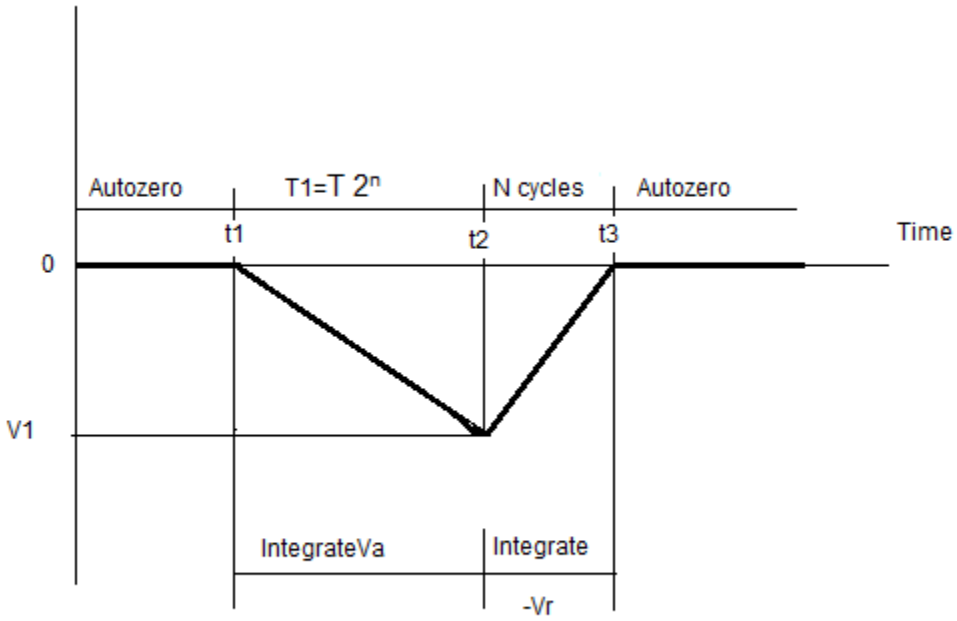
putting the values of $(t_2-t_1)=2^n$ and $(t_3-t_2)=N$,we get

$$V_a(2^n)=(V_R)N$$

$$V_a=(V_R)(N/2^n)$$

The following important observations can be made as,

- Since V_a and n are constant, the analog voltage Va is proportional to the count reading N and is indeoendent of R, c and T.
- The dual slope ADC integrates the input signal for a fixed time, hence it provides excellent noise rejection of ac signals whose periods are integral multiples of the integration time T_1. Thus ac noise superimposed on the input signal such as 50 Hz power line pick-up will be average during the input integration time. So choose clock period T, so that 2^nT is an exact integral multiple of the line period (1/50)second=20ms.
- The main disadvantage of the dual slope ADC is the long conversion time. For instance, if 2^n-T=1/50 is used to reject ling pick-up, the conversion time will be 20ms.
- Dual slope comverters are particularly suitable for accurate measurement of slowly varying signals, such as thermocouples and weighing scales. Dual slope ADCs also form the basis of digital panel meters and multimeters.
- Dual slope converters are available in monolithic form and are available both in microprocessor compatible and in oriented versions. The former provide the digital code in binary form whereas the display oriented versions present the output code in a format suitable for the direct drive of LED displays. The Datel intersil ICL7109 is a monolithoc 12-bit dual slope ADC with microprocessor compatibility.


Autozero
T1=T 2n
N cycles
Autozero
t1
t2
t3
Time
0
V1
IntegrateVa
Integrate
-Vr

Unit-III

Digital integrated circuits

Digital Integrated Circuits: Digital IC characteristics, Digital IC families -RTLand DTL, TL, I2L, TTL, ECL, MOS and CMOS logic circuits, Comparison of digital IC families

INTRODUCTION

An Integrated Circuit (IC) is fabricated on a die of a silicon semiconductor crystal, called a chip, containing the electronic components for constructing digital gate. The various gates are interconnected inside the chip to form the required circuit. The chip is mounted in a ceramic or plastic container, and connections are welded to external pins to form the integrated circuit. The number of pins may range from 14 on a small IC package to several thousand on a larger package. Each IC has a numeric designation printed on the surface of the package for identification. Vendors provide data books, catalogs, and Internet websites that contain descriptions and information about the ICs that they manufacture.

Digital ICs are categorized based on

i) Level of integration-
ii) Logic families

1. LEVEL OF INTEGRATION

Digital ICs are often categorized according to the complexity of their circuits, as measured by the number of logic gates in a single package. They are

Small-scale integration (SSI)

- SSI devices contain several independent gates in a single package.
- The inputs and outputs of the gates are connected directly to the pins in the package.
- The number of gates is usually fewer than 10 and is limited by the number of pins available in the IC.

Medium-scale integration (MSI)

- MSI devices have a complexity of approximately 10 to 1,000 gates in a single package.
- They usually perform specific elementary digital operations.
- MSI digital functions aredecoders, adders, and multiplexers, registers and counters.

Large-scale integration (LSI)

- LSI devices contain thousands of gates in a single package.
- They include digital systems such as processors, memory chips, and programmable logicdevices.

Very large-scale integration (VLSI)

- VLSI devices now contain millions of gates within a single package.
- Examples are large memory arrays and complex microcomputer chips.

2. LOGIC FAMILIES

The digital IC arealso classified based on specific circuit technology. The circuit technology referred logic families. Each logic family has its own basic electronic circuit upon which more complex digital circuits and components are developed. The basic circuit in each technology is a NAND, NOR, or inverter gate. The logic families of digital integrated circuits are

RTL- Resistor Transistor Logic-

- In RTL (resistor transistor logic), all the logic are implemented using resistors and transistors.
- One basic thing about the transistor (NPN), is that HIGH at input causes output to be LOW (i.e. like a inverter).
- In the case of PNP transistor, the LOW at input causes output to be HIGH.

DTL- Digital Transistor Logic-

- In DTL (Diode transistor logic), all the logic is implemented using diodes and transistors.
- Propagation Delay is Larger

I2L- Integrated injection logic-

It Consist of npn and pnp transistor

TTL transistor–transistor logic-

- In Transistor Transistor logic or just TTL, logic gates are built only around transistors.
- TTL Logic has the following sub-families:

✓ Standard TTL.
✓ High Speed TTL
✓ Low Power TTL.
✓ Schhottky TTL.
✓ Low Power Schottky TTL
✓ Advanced Schottky TTL
✓ Advanced Low Power Schottky TTL
✓ Fast Schottky

ECL Emitter-coupled logic-

- The main specialty of ECL is that it is operating in Active Region than the Saturation Region. That is the reason for its high speed operation.
- **Disadvantage**: 1) Large Silicon Area
  2)Large Power Consumption

MOS metal-oxide semiconductor

CMOS complementary metal-oxide semiconductor.

DIGITAL IC CHARACTERISTICS

The characteristics of IC digital logic families are usually compared by analyzing the circuit of the basic gate in each family. The important parameters are

- **fan-out ,**
- **power dissipation,**
- **propagation delay, and**
- **noise margin**

1. FAN OUT or LOADING

- The fan-out of a gate specifies the number of standard loads that can be connected to the outputof the gate without degrading its normal operation
- The fan-out really depends on the amount of electric current a gate can source or sink while driving other gates.
- Consider the connections shown in Fig. 1 the output of one gate is connected to one or more inputs of other.
- The output of the gateis in the high-voltage level(Logic 1) in Fig. 1(a). It provides a current source I_{OH} to all thegate inputsconnected to it.
- Each gate input requires a current I_{IN} for proper operation.
- Similarly, theoutput of the gate is in the low -voltage level (logic 0) in Fig. 1 (b). It provides a current sink I_{OL} forall the gate inputs connected to it. Each gate input supplies a current,I_{IL}
- The fan-out of the gate is $\frac{I_{OH}}{I_{IH}}$ or $\frac{I_{OL}}{I_{IL}}$

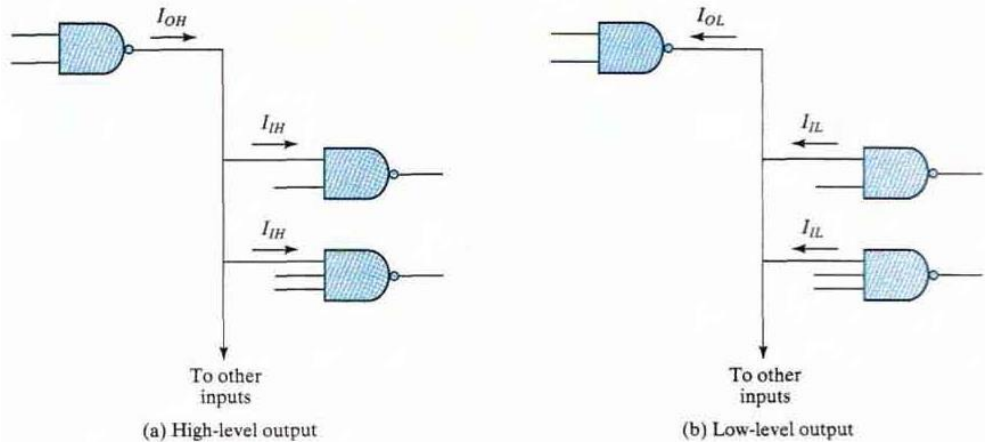


Fig 1. Fan out computation

For example, the standard TTL gates have the following values for the currents
I_{OH} = 400 p.A

I_{IH} = 40 p.A
I_{OL} = 16 mA
I_n = I.6 mA

$$Fanout = \frac{I_{OH}}{I_{IH}} = \frac{I_{OL}}{I_{IL}} = \frac{400\mu A}{40pA} = \frac{16\mu A}{1.6pA} = 10$$

2. POWER DISSIPIATION

- It represents the amount of power needed by thegate.
- It represents the power delivered to the gate from the power supply. It does not include thepower delivered from anothergate
- The amount of power that is dissipated in a gate is calculated from the **supply voltage V_{CC}** and **the current I_{CC} that is drawn by the circuit**.the current drawn from the supply depend on the logic state of the gate

If **I_{CCH}** - The current drawnfrom the power supply when the output of the gate is in the high-voltage level
I_{CCL} - The current drawn from the power supply when the output of the gate is in the low-voltage level

$$I_{CC(avg)} = \frac{I_{CCH} + I_{CCL}}{2}$$

The average power dissipiation is

$$P_{D(avg)} = I_{CC(avg)} \times V_{CC}$$

For example, a standard TTL NAND gate uses a supply voltage Vcc of 5 V and has currentdrains I_{CCH} = I mA and ICCL = 3 mA. The average current is (3 + l)/2 = 2 mA. The averagepower dissipation is 5 x 2 = 10 mW. An IC that has four NAND gates dissipates atotal of 10 x 4 = 40 mW.

3. PROPAGATION DELAY

- The propagation delay of a gate is the average transition-delay time for the signal to propagatefrom input to output when the binary input signal changes in value.
- Propagation delay is measured in nanoseconds(ns); 1 ns is equal to 10^{-9} second.
- If there are many gates, then total propagation delay of digital circuit is the sum of the propagation delays through the gates
- Two propagation delays associated with a logic gates are shown in fig 2

✓ **t_{PHL} :** The time between a specified reference point on the input pulse and a corresponding reference point on the output pulse, with the output changing from the High level to the Low level.

✓ **t_{PLH} :** The time between specified reference point on the input pulse and a corresponding reference point on the output pulse, with the output changing from the Low level to the High level.

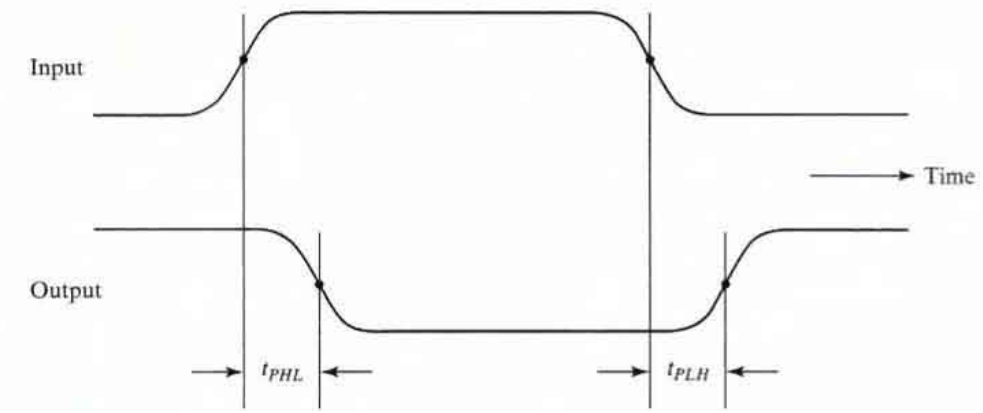


Fig 2. Measurement of Propagation delay

$$\text{The average propogation delay} = \frac{t_{PLH} + t_{PHL}}{2}$$

For example, the delays for a standard TTL gate are t_{PHL} = 7 ns and t_{PLH} = 11μs.

$$\text{The average propogation delay} = \frac{11 + 7}{2} = 9\ ns$$

NOISE MARGIN

- Spurious electrical signals from industrial and other sources can induce undesirable voltageson the connecting wires between logic circuits. These unwanted signals are referred to as*noise*.
- There are two types of noise. **DC noise** is caused by a drift in the voltage levels of asignal. **AC noise** is a random pulse that may be created by other switching signals.
- The noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit's output.
- Noise margin expressed in Volts and represents the maximum noise signal that can be tolerated by the gate shown in figure 3

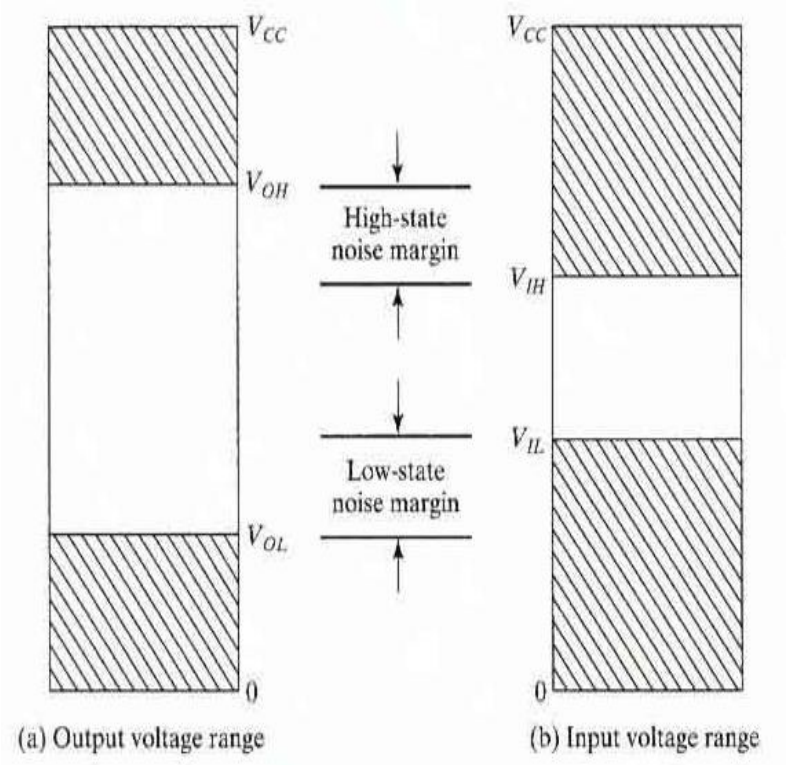


Fig 3. Signals for evaluating noise margin

V_{IL}: Low level input voltage
V_{IH}:High level input voltage
V_{OL}: Low level output voltage
V_{OH}: High level output voltage

The noise margin = $V_{OH} - V_{IH}$
Or
$V_{IL} - V_{OL}$, whichever is smaller.

RTL

The basic circuit of the RTL digital logic family is the NOR is shown in figure 4

- Each input is associated with one resistor and one transistor. The collectors of the transistors are tied together at the output.
- The **voltage levels for the circuit are 0.2 V for the low leve l and from 1 to 3.6 V** for the high level.
- If any input of the RTL gate is high, the corresponding transistor is driven into saturation and the output goes low, regard less of the states of the other transistors.
- If all inputs are low at 0.2 V, all transistors are cut off because V_{BE}< 0.6 V and the output of the circuit goes high.
- the noise margin for low signal input is 0.6 - 0.2 = 0.4 V

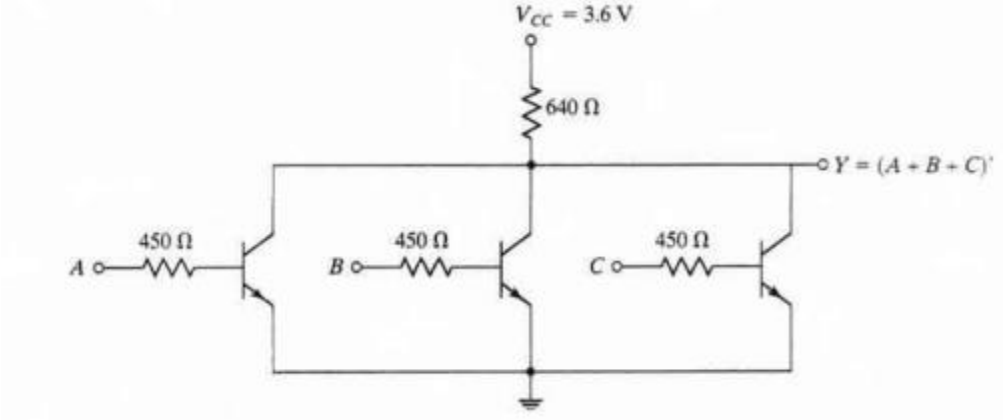


Fig 4. RTL circuit

- **The fan-out** of the RTL gate is limited by **a high output voltage**.
- As the output is loaded with inputs of other gates, more current is consumed by the load.
- This current must flow through the 640-Ω resistor.
- A simple calculation shows_h_{FE} drops to 20, the output voltage drops to about I V when the fan-out is S.
- Any voltage below 1 V in the output may not drive the next transistor into saturation as required.
- **The power dissipation** of the RTL gate is about 12 mw and the **propagation delay averages 25 ns.**

DTL BASIC GATE

- The basic circuit in the DTL digital logic family is the **NAND gate**is shown in figure 5.
- Each input is associated with one diode. The diodes and the 5kΩ resistor form an AND gate.
- The transistor serves as a current amplifier while inverting the digital signal.
- The two **voltage levels are 0.2 V for the low level and between 4 and 5 V** for the high level.

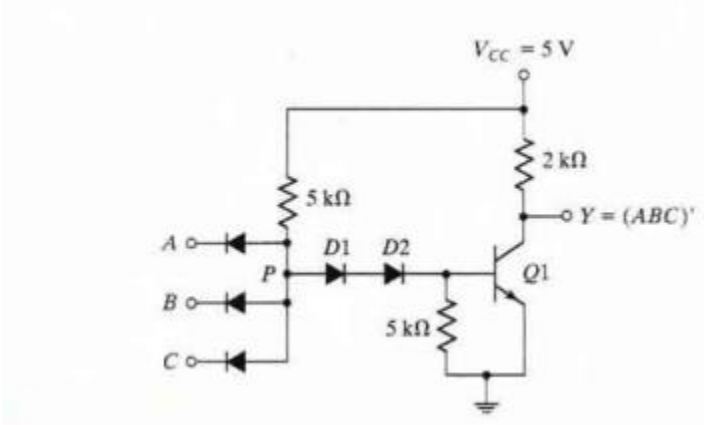


Fig 5. DTL logic Circuits

- If any input of the gale is low at 0.2 V. the corresponding input diode conducts current through VCC and the 5-kΩ resistor into the input node.
- The voltage at point P is equal 10 the input voltage of 0.2 V plus a diode drop of 0.7 V, for a total of 0.9 V.
- In order for the transister to start conducting, the voltage at point P must overcome (i.e., be at least as high as) a I-VBEdrop in QJ plus two diode drops across DI and D2, or 3 X 0.6 = 1.8 V.
- Since the voltage at P is maintained at 0.9 V by the input conducting diode. the transistor is cut off with no drop across the 2-kΩ resistor and the output voltage is high at 5 V.
- If all inputs of the gate are high, the transistor is driven into the saturation region .
- The voltage at P now is equal to VBE plus the two diode drops across DI and D2, or 0.7 X 3 = 2.1 V. Since all inputs are high at 5 V and since Vp = 2.1 V, the input diodes are reverse biased and off.
- The base current is equal to the difference of the currents flowing in the two 5kΩ resistors and is sufficient to drive the transistor into saturation.
- With the transistor saturated, the output drops to Va = 0.2 V, which is the low level for the gate .
- The **power dissipation** of a DTL gate is about **12 mW** and the **propagation delay** averages **30 ns**.
- The **noise margin is about 1 V and a fan-out as high as 8** is possible .
- The **fan-out of the DTL gale is limited by the maximum current that can flow in the collector of the saturated transistor**.
- The fan-out of a DTL gate may be increased by replacing one of the diodes in the base circuit with a transistor shown in figure 6

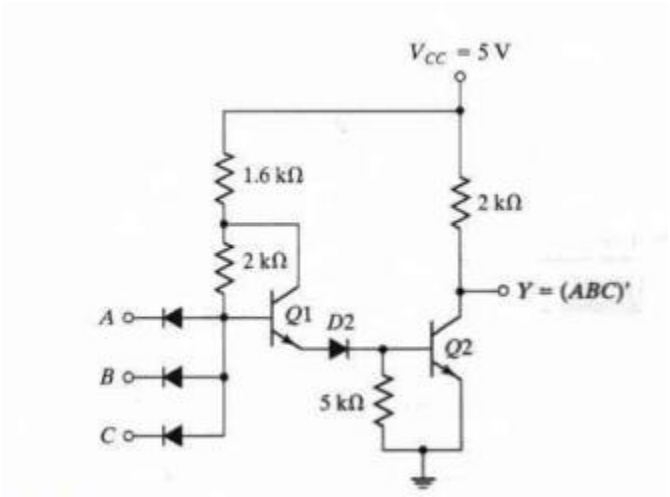


Fig 6. Modified DTL gates

- Transistor Q1 is maintained in the active region when output transistor Q2 is saturated.
- As a consequence, the modified circuit can supply a larger amount of base current to the output transistor, which can now draw a larger amount of collector current before it goes out of saturation.

- Part of the collector current comes from the conducting diode s in the loading gates when Q2 is saturated.
- Thus, an increase in the allowable saturated current in the collector allows more loadsto be connected to the output, increasing the fan-out capability of the gale .

TTL

- The original basic transistor- transistor logic (TIL) gate was a slight improvement over the DTL gate.
- TTL widely used in the design of digital systems.
- Commercial TIL ICs have a number designation that starts with 74 and follows with a suffix that identifies the series. Examples are 7404, 74S86 and 74ALS161.
- The speed-power product is an important parameter used in comparing the various TIL series. It the product of the propagation delay and power dissipation. The speed-power product is measured in picojoules (pJ).
- A low value for this parameter is desirable because it indicates that a given propagation delay can be achieved without excessive power dissipation and vice versa.
- The standard TTL gate was the first version in theTTL family. This basic gate was then designed with different resistor values to produce gates with lower power dissipation or with higher speed.
- The propagation delay of a transistor circuit that goes into saturation depends mostly on two factors: **storage time and RC time constants**.
- Reducing the storage time decreases the propagation delay. Reducing resistor values in the circuit reduces the RC time constants and decreases the propagation delay.
- Of course, the trade-off is higher power dissipation, because lower resistances draw more current from the power supply. The speed of the gate is inversely proportional to the propagation delay.
- In the **low-power TIL gate**, the resistor values are higher than in the standard gate in order to reduce the power dissipation but the propagation delay is increased.
- In the **high-speed TTL gate**, resistor values are lowered to reduce the propagation delay. but the power dissipation is increased.
- The **Schottky TTL gate** was the next improvement in the technology. The effect of the Schottky transistor is to remove the storage time delay by preventing the transistor from going into saturation. This series increases the speed of operation of the circuit without an excessive increase in power dissipation.
- **The low-power Schottky TTL** sacrifices some speed for reduced power dissipation. It is equal to the standard TTL in propagation delay, but has only one-fifth the power dissipation.
- Further innovations led to the development of the advanced Schottky series, which provides an improvement in propagation delay over the Schottky series and also lowers the power dissipation.
- The advanced low-power Schottky has the lowest speed- power product and is the most efficient series. The fast TTL family is the best choice for high-speed designs.

- All TTL series are available in S81components and in more complex forms. such as MSI and LSI components.
- The differences in the TTL series are not in the digital logic that they perform, but rather in the internal construction of the basic NAND gale.
- In any case, TTL gates in all the available series come in three different types of output configuration:
    1. Open -collector output
    2. Totem-pole output
    3. Three-state output.

1. Open-Collector Output Gate

- The basic TIL gate is a modified circuit of the DTL gate shown in figure 7.
- The multiple emitters in transistor QI are connected to the inputs, these emitters behave like the input diodes in the DTL gate, since they form a pn junction with their common base.

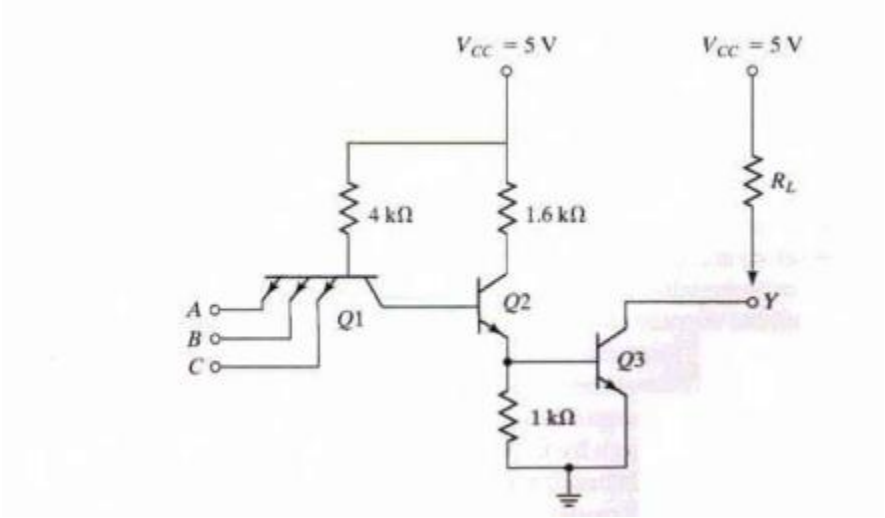


Fig 7 .open-collector TTL NAND gate

- The base-collector junction of Q1 acts as another pn junction diode corresponding to D1 in the DTL gate
- Transistor Q2 replaces the second diode D2 in the DTL gale. The output of the TTL gate is taken from the open collector of Q3. A resistor connected to Vcc must be inserted externally to the IC package for the output to "pull up" to the high voltage level when Q3 is off; otherwise, the Output acts as an open circuit.
- The two voltage levels of the TTL gate **are 0.2 V for the low level and from 2.4 to 5 v for the high level**
- The basic circuit is a **NAND** gate

Operation of NAND Gate

- **If any input is low**, the corresponding base-emitter junction in Q1 is forward biased. The voltage at the base of Q1 is equal to the input voltage of 0.2 V plus a

VBE drop of 0.7 or 0.9 V. In order for Q3 to start conducting, the path from Q1 to Q3 must overcome a potential of one diode drop in the base-collector pn junction of Q1 and two VBE drops in Q2 andQ3, or 3 x 0.6 = 1.8 V. Since the base of QI is maintained at 0.9 V by the input signal, the output transistor cannot conduct and is cut off. The output level will be high if an external resistor is connected between the output and Vcc(or an open circuit if a resistor is not used).

- **If all inputs are high**, both Q2 and Q3 conduct and saturate.
- The base voltage of Q1 is equal to the voltage across its base-collector pn junction plus two VBE drops in Q2 and Q1, or about 0.7 x 3 = 2.1 V.
- Since all inputs are high and greater than 2.4 V, the base-emitter junctions of Q1 are all reverse biased.
- When output transistor Q3 saturates (provided that it has a current path), the output voltage goes low to 0.2 V. This confirm s the conditions of a NAND operation

Effect of open collector without external resistor

- The open-collector TTL gate will operate without the external resistor when connected to inputs of other TTL gales although this kind of operation is not recommended because of the low noise immunity encountered.
- Without an external resistor, the output of the gate will be an open circuit when Q3 is off.
- An open circuit to an input of a TTL gate behaves as if it has a high level input (but a small amount of noise can change this to a low level).
- When Q3 conducts, its collector will have a current path supplied by the input of the loading gate through Vcc. the 4-k ohm resistor, and the forward-biased base-emitter junction.

Application if open-collector

Open-collector gales are used in three major applications: **driving a lamp or relay, performing wired logic and constructing a common-bus system**.

1. An open-collector output can drive a lamp placed in its output through a limiting resistor.When the output is low, the saturated transistor Q3 forms a path for the current that turns the lamp on. When the output transistor is off, the lamp turn s off because there is no path for the current.
2. If the outputs of several open-collector TTL gates are tied together with a single external resistor, a wired- AND logic is performed
3. Open-collector gates can be tied together to form a common bus. At any time, all gale outputs tied to the bus, except one, must be maintained in their high state. The selected gate may be in either the high or low state, depending on whether we want to transmit a 1 or a 0 on the bus. Control circuits must be used to select the particular gate that drives the bus at any given time

2. TOTLEM POLE OUTPUT

- The output impedance of a gate is normally a resistive plus a capacitive load.
- The capacitive load consists of the capacitance of the output transistor, the capacitance of the fan-out gates and any stray wiring capacitance.
- When the output changes from the low to the high state, the output transistor of the gate goes from saturation to cutoff and the total load capacitance C charges exponentially from the low to the high voltage level with a time constant equal to RC
- For the open-collector gate, R is the external resistor marked RL.
- For a typical operating value of C = 15 pF and RL = 4 Kohm.
- the propagation delay of a TTL open-collector gate during the turnoff time is 35 ns.
- With an active pull-up circuit replacing the passive pull-up resistor RL, the propagation delay is reduced to 10 ns.
- The figure 8 is called as totem pole because transistor Q4 "s its" upon Q3.

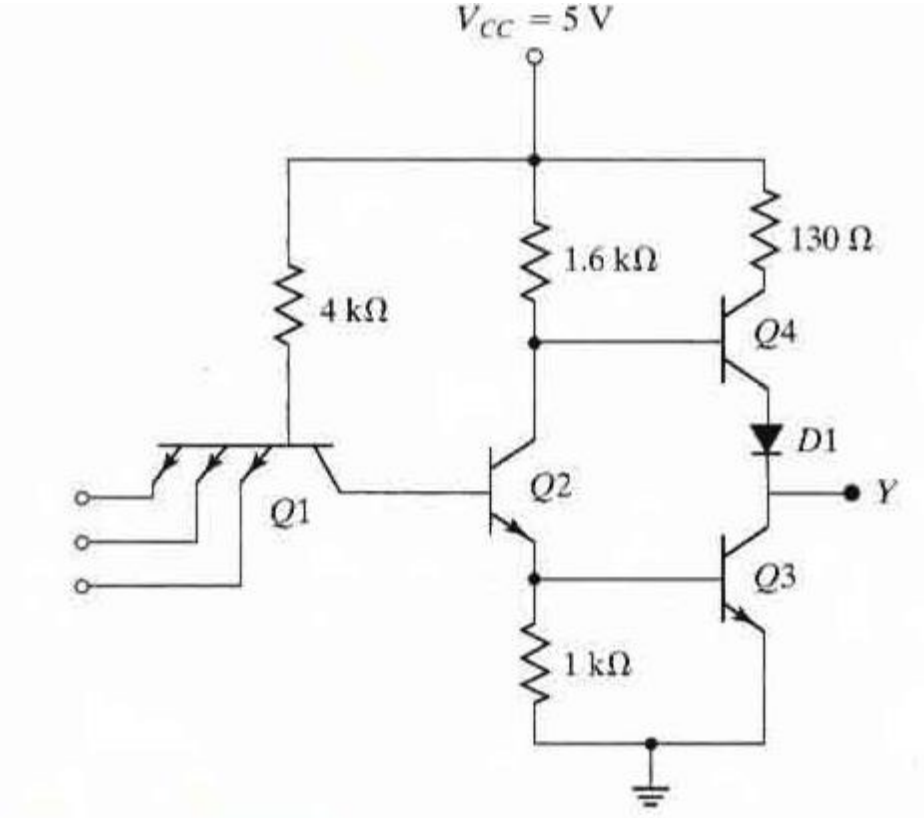


Fig. 8 TTL gate with totem pole output

Operation of Totem pole TTL

- When the output Y is in the low state, Q2 and Q3 are driven into saturation as in the open-collector gate.
- The voltage in the collector of Q2 is VBE(Q3) + VCE (Q2) or 0.7 + 0.2 = 0.9 V. The output Y = VCE(Q3) = o.2 V.

- Transistor Q4 is cut off because its base must be one VBE drop plus one diode drop, or 2 x 0.6 =1.2 V to start conducting.
- Since the collector of Q2is connected to the base of Q4, the latter's voltage is only 0.9 V instead of the required 1.2 V. so Q4 is cut off.
- The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that Q4 is cut off when Q3 is saturated.
- When the output changes to the high state because one of the inputs drop to the low state, transistors Q2 and Q3 go into cutoff.
- However, the output remains momentarily low because the voltages across the load capacitance cannot change instantaneously.
- As soon as Q2 turns off. Q4 conducts, because its base is connected to Vcc through the 1.6-K ohm resistor.
- The current needed to charge the load capacitance causes Q4 to saturate momentarily and the output voltage rises with a time constant RC.
- But R in this case is equal to 130 n, plus the saturation resistance of Q4, plus the resistance of the diode, for a total of approximately 150ohm.
- This value of R is much smaller than the passive pull-up resistance used in the open-collector circuit. As a consequence, the transition from the low to high level is much faster.
- As the capacitive load charges, the output voltage rises and the current in Q4 decreases, bringing the transistor into the active region.
- Thus, in contrast to the other transistors, Q4 is in the active region when Q4 is in a steady -state condition.
- The final value of the output voltage is then 5 V, minus a VBE drop in Q4,minus a diode drop in DJ to about 3.6 V.
- Transistor Q3 goes into cutoff very fast, but during the initial transition time, both Q3 and Q4 are on and a peak current is drawn from the power supply.
- This current spike generates noise in the power-supply distribution system.
- When the change of state is frequent, the transient-current spikes increase the power-supply current requirement and the average power dissipation of the circuit increases.

3. SCHOTTKY TTL

- Propagation delay is reduced by eliminating saturation by placing Schottky diode between the base and collector of each saturated transistor in the circuit
- The Schottky diode is formed by the junction of a metal and semiconductor
- The voltage across a conducting Schottky diode is only 0.4 V.
- The presence of a Schottky diode between the base and collector prevents the transistor from going into saturation. The resulting transistor is called a Schottky transistor. The use of Schottky transistors in a TTL shown in figure.9 decreases the propagation delay without sacrificing power dissipation.

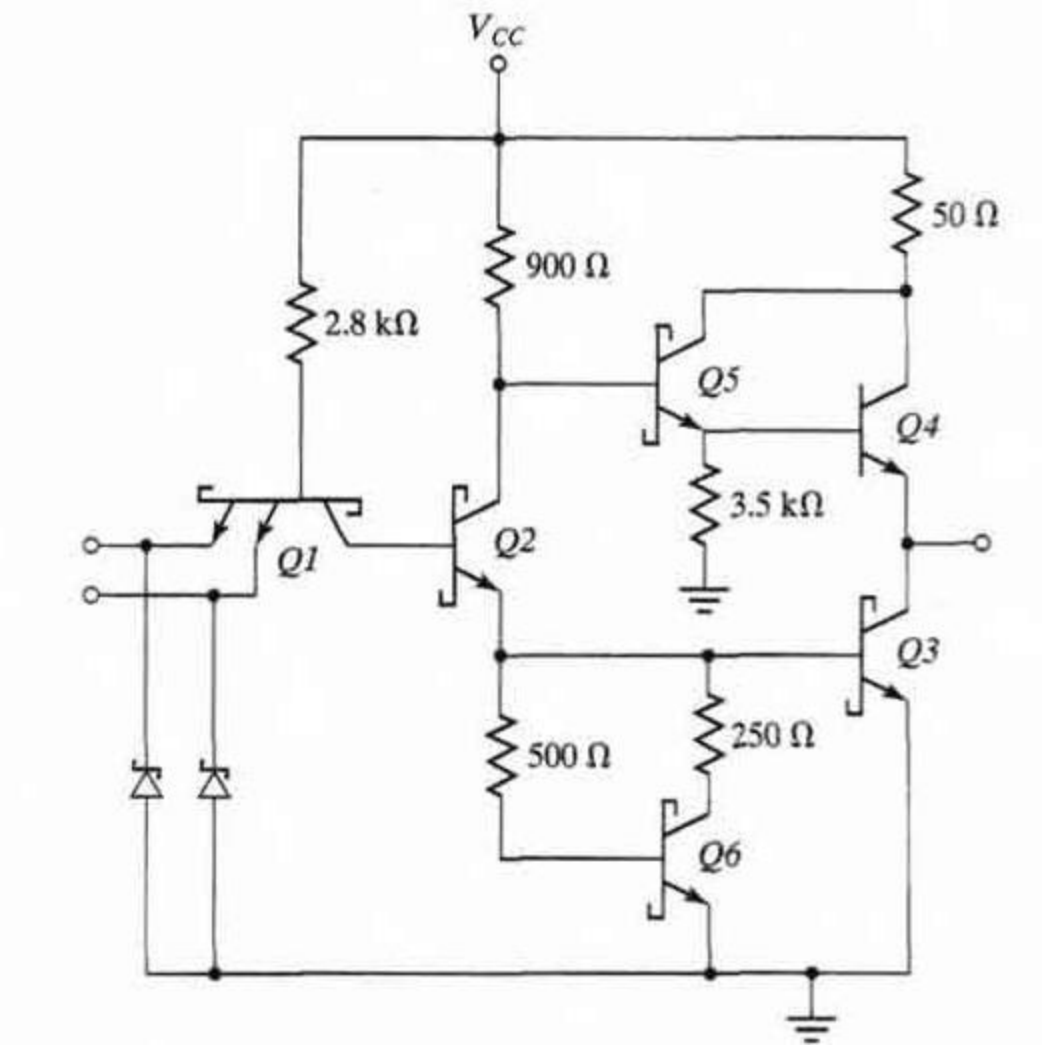


Fig 9.Schottky TTL gate

- Two new transistors, Q5 and Q6, have been added, and Schottky diodes are inserted between each input terminal and ground. There is no diode in the totem-pole circuit. However. the new combination of Q5 and Q4 still gives the two VBE drops necessary to prevent Q4 from conducting when the outpu t is low. This combination constitutes a double emitter-follower called a **Darlington pair**.
- The Darlington pair provides a very high current gain and extremely low resistance, exactly what is needed during the low-to-high swing of the output, resulting in a decrease in propagation delay.

Effect of diodes

- The diodes in each input shown in the circuit help clamp any ringing that may occur in the input lines. Under transient switching conditions, signal lines appear inductive; this, along with stray capacitance, causes signal s to oscillate, or **"ring**."

- When the output of a gate switches from the high to the low state, the ringing waveform at the input may have excursions as great as 2-3 V below ground, depending on the line length.
- The diodes connected to ground help clamp this ringing, since they conduct as soon as the negative voltage exceeds 0.4 V.
- When the negative excursion is limited, the positive swing is also reduced.
- Clamp diodes have been so successful in limiting line effects that all versions of TTL gates use them
- Turn off is reduced by transistor Q6 and two resistors

I2L OR MERGED TRANSISTOR LOGIC

- Its main advantage is High packaging density and this family used in LSI functions.
- It consist of npn and pnp BJT. It reduces the number of metal connections
- Its operation is similar to RTL gates with few differences
    - the base resistor is removed altogether in the I2L
    - the collector resistor used in the RTL is replaced by a pnp transistor and act as the load for I2L gate
    - I2L transistor use multiple collectors instead of individual trasnsitor

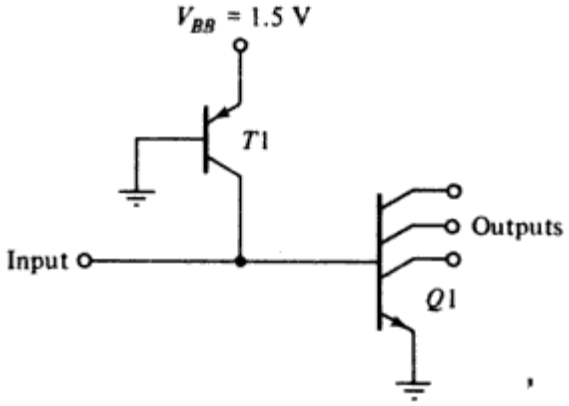


Fig.10 I^2L basic gate

- The schematic diagram of the basic I^2L gate is shown in figure.10. It has an npntransistor, Q1, with multiple collectors for the output.
- The base circuit has pnp transistor, T1, connected to supply voltage V_{BB}.
- The study of operationof I2L is made by interacting with other gate instead of stand alone

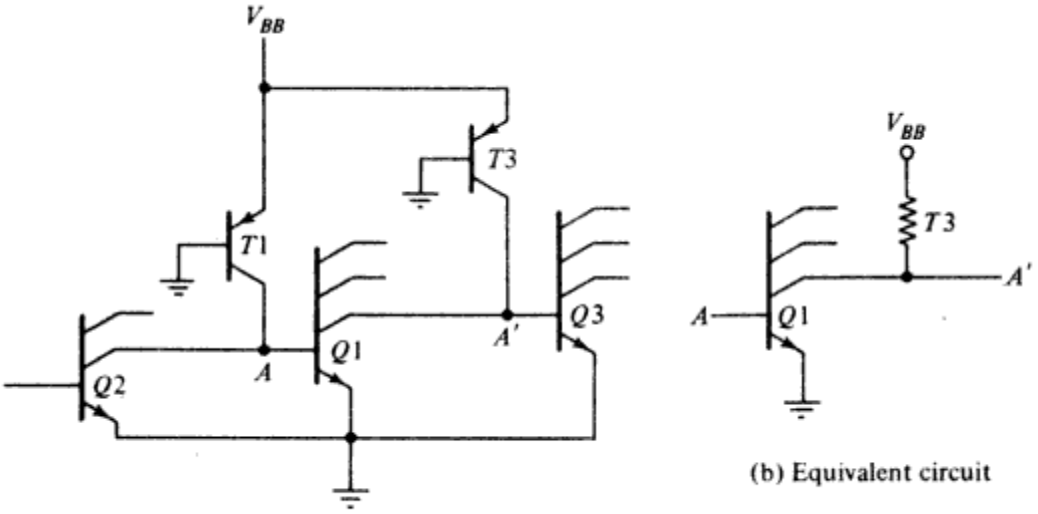
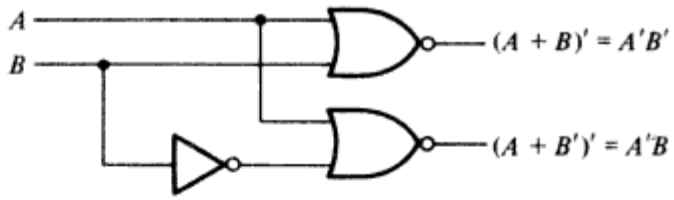
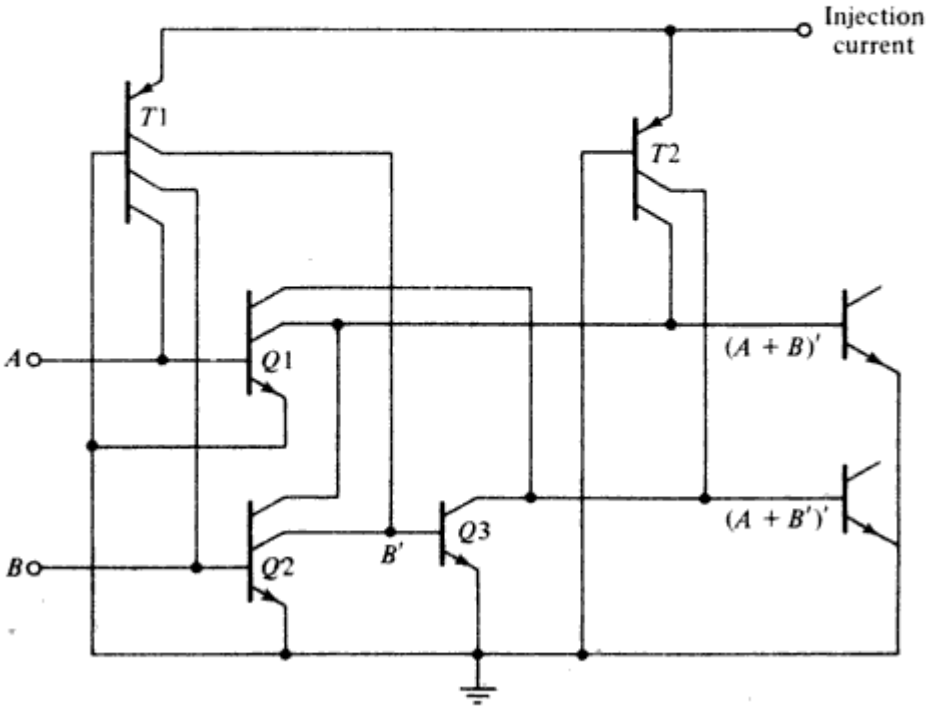


Fig 11.Connection of othergates to the inputs and outputs of a basic I2L.

- Figure 11 shows the interaction of the basic gate formed by the Q1 and T1 with other gates in itsinput and output. One collector of Q2 supplies the input to the basic gate.
- Transistor T1 in the basic gate act as a load that injects current to the collector of the Q2.
- One of the collectors of the Q1 act as an output of the basic gate and is connected to the base of Q3.
- Transistor T3, connected to the base of Q3, act as load to inject current to the collector of Q1 in the basic gate.The basic gate here act as inverter and its equivalent circuits is shown Fig11 (b)
- The pnp act as collector load for all other gates that are connected to this base
- When I2L basic gate connected to other gates, performs the NOR logic function which is given in figure 12.



(a) Logic diagram



(b) Circuit diagram

Fig 12. Typical among I2L gate

- The collectot of Q1 and Q2 sre tied together to form NOR function. Input B is complemented by the transistor Q2.
- The collector of Q3 and Q1 are tied together to form the second NOR function. The base of each npntrasnsitor receives the injection current from the multiple collector pnp transistor T1 and T2. The emitter of npn transistor are connected to the base of the pnptranssitor to facilitate the construction
- The voltage level of I2L - **High 0.7V, Low: 0.2V**
- Fanout = 3
- Propagation delay = 5ns
- Power dissipiation= 5mW per gate

EMITTER -COUPLED LOGIC

- Emitter-coupled logic (ECL) is a **non-saturated digital logic family**ie works in Active region. Since transistors do not saturate, it is possible to achieve **propagation delays** as low **as 1-2 ns**.
- This logic family has the lowest propagation delay of any family and is used mostly in systems requiring very **high speed operation**.
- **Its noise immunity and power dissipation** ,however,are the **worst** of all the logic families available.

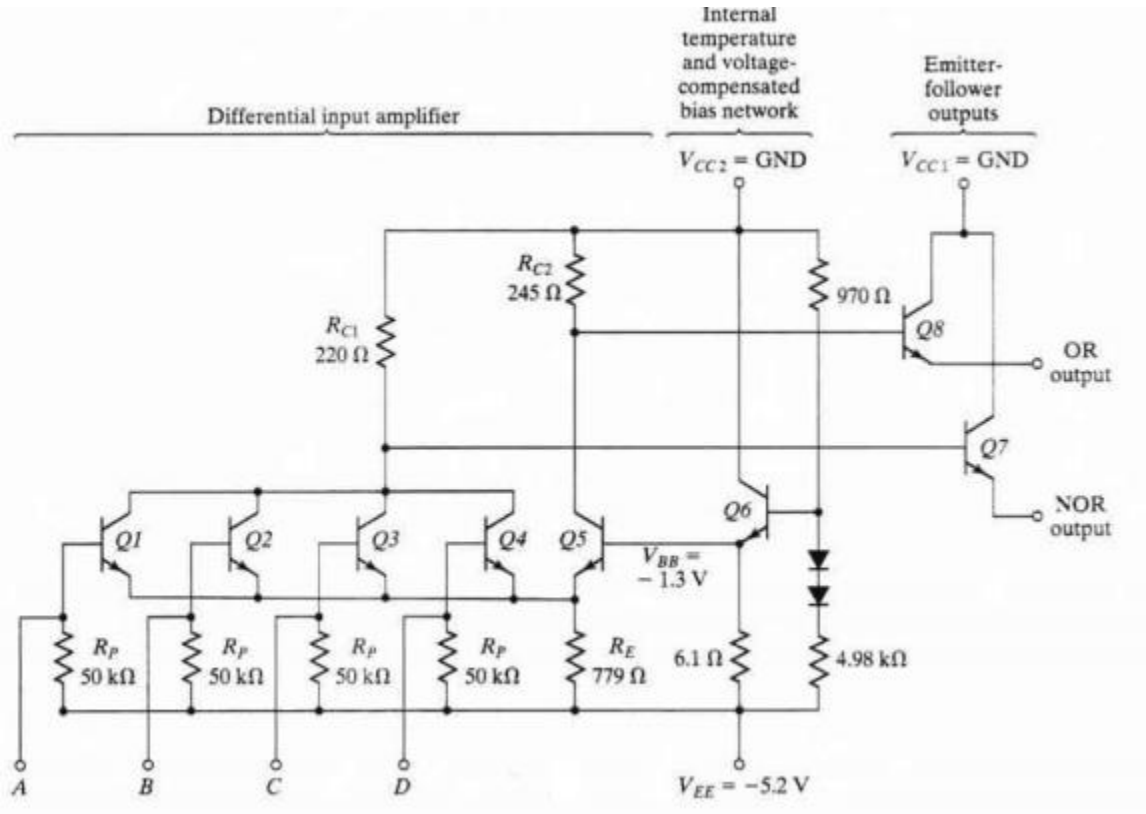


Fig 13. ECL logic circuit

- The outputs provide both the OR and NOR functions.
- Each input is connected to the base of a transistor. The **two voltage levels are about -0.8 V for the high state and about - 1.8 V for the low state.**
- The circuit shown in figure 13 consists of a **differential amplifier,a temperature- and voltage-compensated bias network and an emitter-follower output.**
- The emitter outputs require a pull-down resistor for current to flow.
- This is obtained from the input resistor Rp of another similar gate or from an external resistor connected to a negative voltage supply.
- The internal temperature- and voltage -compensated bias circuit supplies a reference voltage to the differential amplifier.

- Bias voltage V_{BB} set at - 1.3 V, which is the midpoint of the signal's logic swing. The diodes in the voltage divide,together with Q6, provide a circuit that maintains a constant V_{BB} value despite changes in temperature or supply voltage.
- Any one of the power supply inputs could be used as ground. However, the use of the Vccnode as ground and V_{EE} at - 5.2 V results in the best noise immunity.
- If any input in the ECL gate is high, the corresponding transistor is turned ON and Q5 is turned off.
- An input of - 0.8 V causes the transistor to conduct and places -1.6 V on the emitters of all of the transistors. (The VBE drop in ECL transistors is 0.8 V.)
- Since VBB = - 1.3 V, the base voltage of Q5 is only 0.3 V more positive than its item set. Q5 is cut off because its VBE voltage needs at least 0.6 V to stan conducting.
- The current in resistor Rc2 flows into the base of Q8 (provided that there is a load resistor).
- This current is so small that only a negligible voltage drop occurs across Rc2.
- The OR output of the gate is one VBE drop below ground or - 0.8 V, which is the high stale.
- The current flowing through Rc1 and the conducting transistor causes a drop of about 1 V below ground.
- The NOR output is one V_{BE} drop below this level or - 1.8 V, which is the low stale.
- If all inputs are at the low level, all input transistors turn off and Q5 conducts.
- The voltage in the common-emitter node is one V_{BE} drop below VBB, or - 2.1 V. Since the base of each input is at a low level of - 1.8 V, each base-emitterjunction has only 0.3 V and all input transistors are cut off.
- Rc2 draws current through Q5 that results in a voltage drop of about 1 V, making the OR output one VBE drop below this at -1.8 V. or the low level.
- The current in RC2 is negligible and the NOR Output is one V_{BE} drop below ground, at - 0.8 V. or the high level. This analysis verifies the OR and NOR operations of the circuit.
- **The propagation delay of the ECL gate is 2 ns** and **the power dissipation is 25 mW**, giving a **speed-power product of 50**,which is about the same as that for the Schottky TTL.
- The **noise margin is about 0.3 V** and is not as good as that in the TTL gate.
- **High fan-out is possible** in the ECL gate because of the high input impedance of the differential amplifier and the low output impedance of the emitter-follower.
- Because of the extreme high speed of the signals, external wires act like transmission lines. Except for very short wires of a few centimeters.
- ECL outputs must use coaxial cables with a resistor termination to reduce line reflections.

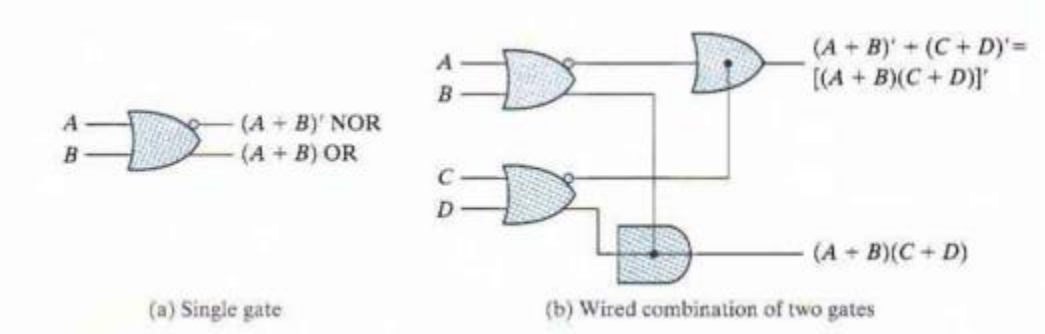


Fig 14. Graphic symbol and wired combination if the ECL gate

- The graphical symbol for the ECL shown in Fig14 aTwo outputs are available: one for the NOR function and the other for the OR function.
- The outputs of two or more ECL gates can be connected together to form wired logic
- Fig14 b showsAn external wired connection of two NO R outputs produces a wired-OR function.
- An internal wired connection of two OR outputs is employed in some ECL ICs to produce a wired-AND (sometimes called dot-AN D) logic. This property may be utilized when ECL gates are used to form the OR- AND- INVERT and the OR-AND functions.

METAL -OXIDE SEMICONDUCTOR

- The field-effect transistor (FET) is a unipolar transistor, since its operation depends on the flow of only one type of carrier.
- There are two types ofFETs:
  - the junction field-effect transistor (JFET) and
  - the metal-oxide semiconductor (MOS).
- The former is used in linear circuits and the latter in digital circuits. MOS transistors can be fabricated in less area than bipolar transistors. The basic structure shown in figure 15

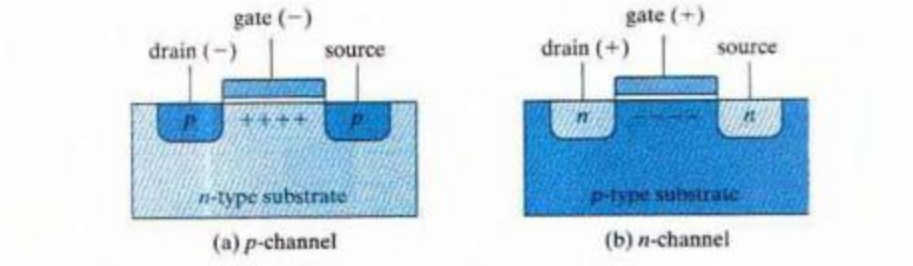


Fig 15. Basic structure of MOS transistor

- The p-channel MOS consists of a lightly doped substrate of n-type silicon material.
- Two regions are heavily doped by diffusion with p-type impurities to form the source and drain. 1be region between the two type sections serves as the channel.
- The gate is a metal plate separated from the channel by an insulated dielectric of silicon dioxide

- A negative voltage (with respect to the substrate) at the gate terminal causes an induced electric field in the channel that attracts p-type carriers (holes) from the substrate .
- As the magnitude of the negative voltage on the gate increases, the region below the gate accumulates more positive carriers, the conductivity increases, and current can now from source to drain, provided that a voltage difference is maintained between these two terminals.
- There are four basic types of MOS structures.
- The channel can be p or n type,depending on whether the majority carriers are holes or electrons.
- The mode of operation can be enhancement or depletion, depending on the state of the channel region at zero gate voltage.
- If the channel is initially doped lightly with p-type impurity (in which case it is called a diffused channels. a conducting channel exists at zero gate voltage and the device is said to operate in the depletion mode.
- In this mode,current flows unless the channel is depleted by an applied gate field. If the region beneath the gate is left initially uncharged. a channel must be induced by the gate field before current can flow.
- Thus, the channel current is enhanced by the gate voltage and such a device is said to operate in the enhancement mode.
- The source is the terminal through which the majority carriers enter the device.
- The drain is the terminal through which the majority carriers leave the device. In a n-channel MOS. the source terminal is connected to the substrate and a negative voltage is applied to the drain terminal.
- When the gate voltage is above a threshold voltage VT (abo ut - 2 V), no current flow s in the channel and the drain -to-source path is like an open circuit.
- When the gate voltage is sufficiently negative below VT a channel is formed and p-type carriers flow from source 10 drain.
- p-type carriers are positive and correspond to a positive current flow from source to drain.
- In the n-channel MOS, the source terminal is connected to the substrate and a positive voltage is applied to the drain terminal.
- When the gate voltage is below the threshold voltage Vr (about 2 V), no current flows in the channel.
- When the gate voltage is sufficiently positive above Vr to fonn the channel, a-type carriers flow from source todrain, n-type carriers are negative and correspond to a positive current flow from drain to source.

- The threshold voltage may vary from 1 to 4 V, depending on the particular process used.

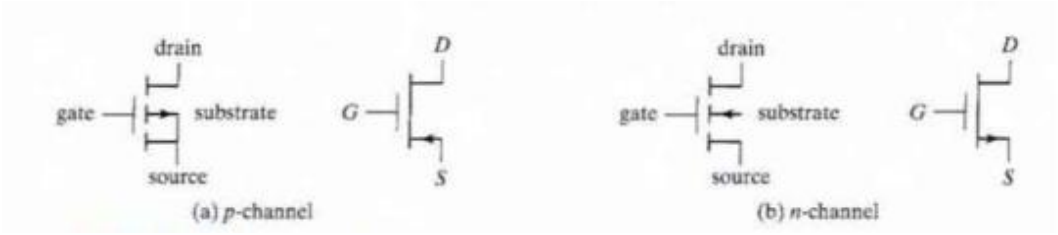


Fig 16. Symbol for MOs transistors

- The symbol shown in figure 16 for the enhancement type is the one with the broken-line connection between source and drain .
- In this symbol, the substrate can be identified and is shown connected to the source.
- An alternative symbol omits the substrate and instead an arrow is placed in the source terminal to show the direction of positive current flow (from source to drain in the p-channel MOS and from drain to source in the n-channel MOS).
- Because of the symmetrical construction of source and drain, the MOS transistor can be operated as a bilateral device.
- Although normally operated so that carriers flow from source to drain,there arecircumstances when it is convenient to allow carriers to flow from drain to source.
- Figure 17 shows the MOS logic circuits using

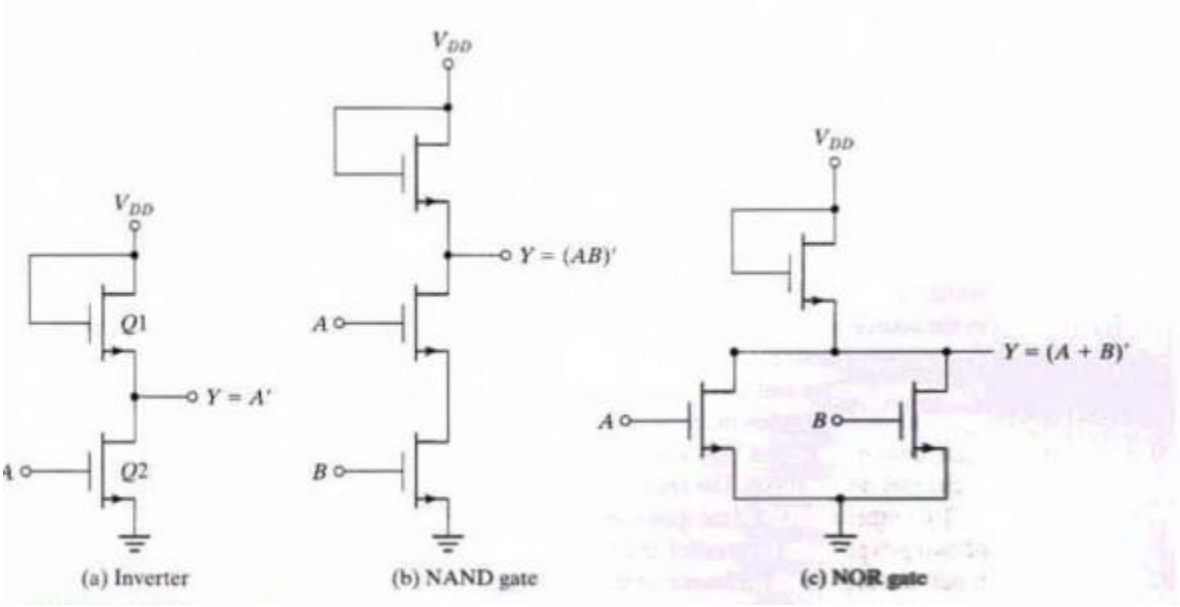


Fig 17. MOS logic circuits

COMPLEMENTARY MOS

- Complementary MOS (CMOS) circuits take advantage of the fact that both n-channel and p -channel devices can be fabricated on the same substrate.
- CMOS circuits consist of both types of MOS devices interconnected to form logic functions.

- The basic circuit is the inverter, which consists of one p-channel transistor and one n-channel transistor.
- The source terminal of the p-c hannel device is at VDD,and the source terminal of the a-channel device is at ground.
- The value of VDD may be anywhere from +3 to +18 V. The two voltage levels are 0 V for the low level and VDD for the high level (typically. 5 V).
- To understand the operation of the inverter, we must review the behavior of the MOS transistor from the previous section:
- 1. The a-channel MOS conducts when its gate-to-source voltage is positive.
- 2. The n-channel MOS conducts when its gale-to-source voltage is negative.
- 3. Either type of device is turned off if its gate-to-source voltage is zero.
- Now consider the operation of the inverter shown in figure 18 a. When the input is low, both gates are at zero potential.
- The input Is at – VDD relative to the source of the p-channel device and at 0 V relative to the source of the a-channel device.
- The result is that the p-channel device is turned on and the a-channel device is turned off.
- Under these conditions, there is a low-impedance path from VDD to the output and a very high impedance path from output to ground.
- Therefore, the output voltage approaches the high level VDD under normal loading conditions
- When the input is high, both gates are at VDD and the situation is reversed: The p..channel device is off and the a-channel device on.
- The result is that the output approaches the low level of 0 V.

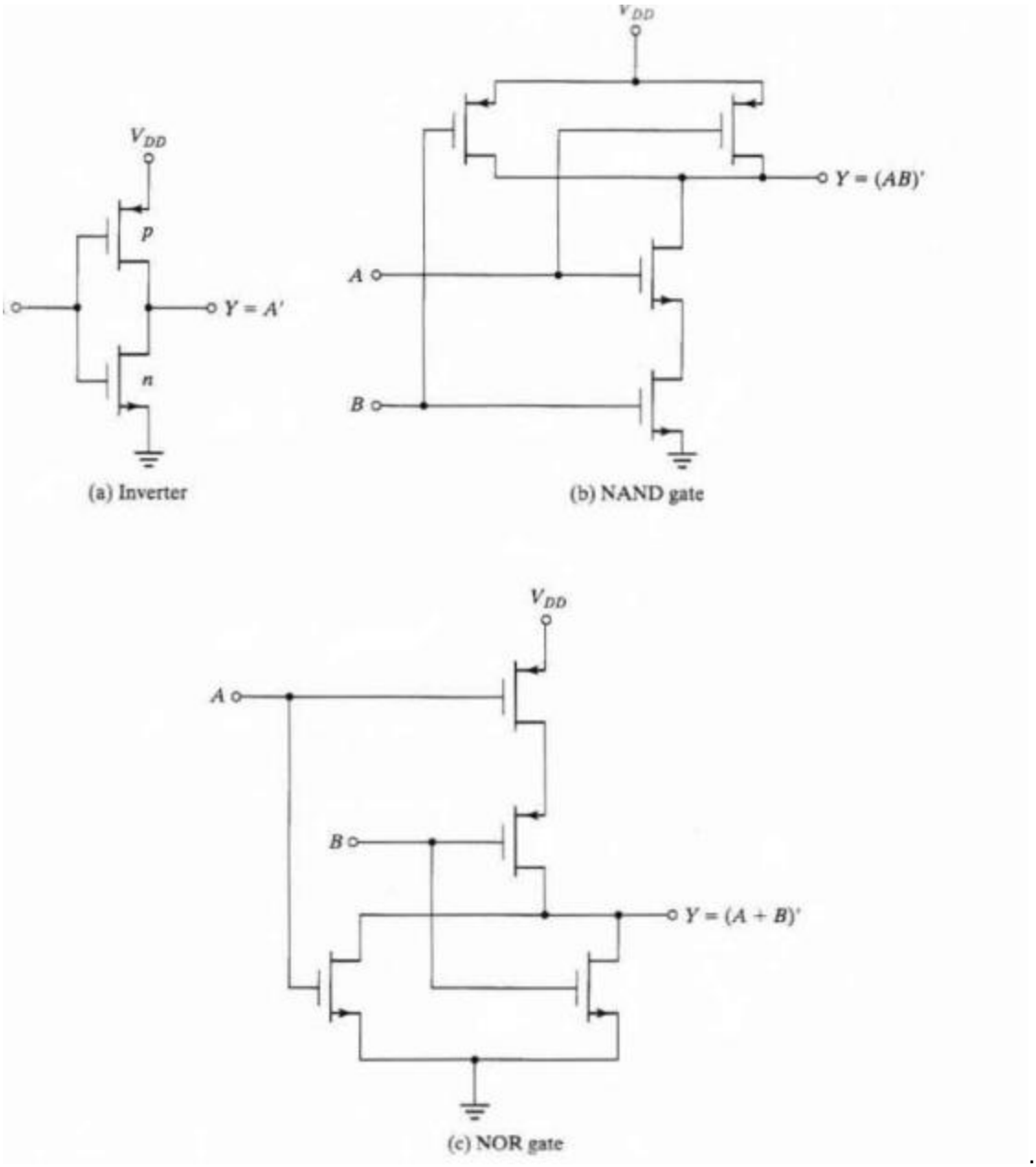


Fig 18. CMOS logic circuits

- A two-input NAND gate shown in figure 18 b consists of two p-type units in parallel and two e -type units in series
- If all inputs are high, both p-channel transistors turn off and both n-channel transistors turn on.
- The output has low impedance to ground and produces a low state.
- If any input is low the associated p -channel transistor is turned off and the associated p-channel transistor is turned on.
- The output is coupled to VDD and goes 10the high state.

- Multiple-input NAND gates may be formed by placing equal numbers of p-type and n-type transistors in parallel and series respectively in an arrangement similar .
- A two-input NOR gate shown in fig 18 c. consists of two n-type units in parallel and two p -type unit, in series.
- When all inputs are low both p-channel units are on and both n-channel units are off.
- The output is coupled to VDD and goes to the high state.
- If any input is high the associated p-channel transistor is turned off and the associated n-channel transistor turns on, connecting the output to ground and causing a low-level output.
- MOS transistors can be considered to be electronic switches that either conduct or are open.
- As an example, the CMOS inverter can be visualized as consisting of two switches.
- Applying a low voltage to the input causes the upper switch (p) to close, supplying a high voltage to the output.
- Applying a high voltage to the input causes the lower switch (n) to close, connecting the output to ground.
- Thus, the output Vout is the complement of the input Vin, Commercial applications often use other graphic symbols for MOS transistors to emphasize the logical behavior of the switches.
- The arrows showing the direction of current flow are omitted. Instead. the gate input of the p- channel transistor is draw n with an inversion bubble on the gate terminal to show that it is enabled with a low voltage.
- The inverter circuit is redrawn with these symbols in Fig. 18. A logic 0 in the input causes the upper transistor to conduct, making the output logic 1.
- A logic 1 in the input enables the lower transistor to conduct. making the output logic 0.

CMOS Characteristics

- When a CMOS logic circuit is in a static state, its power dissipation is very low.
- This is because at least one transistor is always off in the path between the power supply and ground when the state of the circuit is not changing. As a result. a typical CMOS gate has static power dissipation on the order of 0.0 1mw.
- However, when the circuit is changing state at the rate of 1MHz,the power dissipation increases to about 1 m W, and at In MHz it is about 5 mW.

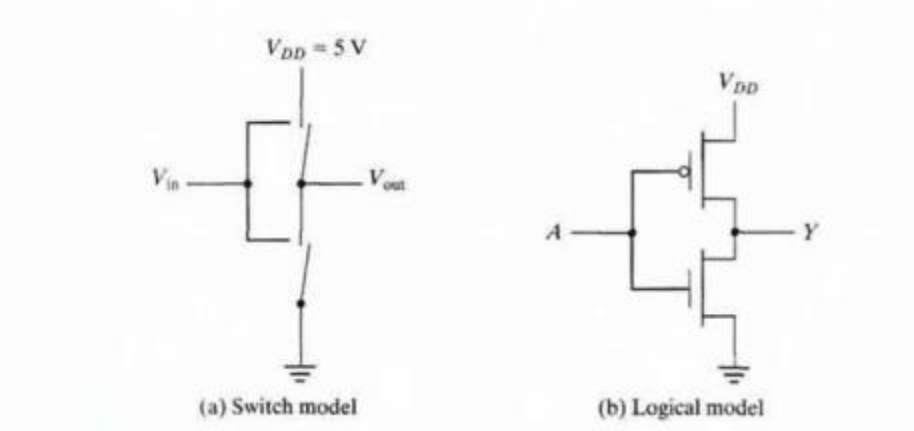


Fig 19. CMOS inverter

- CMOS logic is usually specified for a single power-supply operation over a voltage range from 3 to 18 V with a typical voc value of 5 V.
- Operating CMOS at a larger power-supply voltage reduces the propagation delay lime and improves the noise margin, but the power dissipation is increased.
- The propagation delay time with VDD = 5 V ranges from 5 to 20 ns, depending on the type of CMOS used.
- The noise margin is usually about 40 percent of the power supply voltage.
- The fan-out of CMOS gates is about 30 when they are operated at a frequency of 1 MHz.
- The fan-out decreases with an increase in the frequency of operation of the gates.
- There are several series of the CMOS digital logic family. The 74C series are pin and function compatible with TTL devices havin g the same number.
- For example,CMOS IC type 74C04 has six inverters with the same pin configuration as TIL type 7404.
- The high-speed CMOS 74VHC series is an improvement over the 74C series. with a tenfold increase in switching speed.
- The 74HCT series is electrically compatible with TIL ICs. This means that circuits in this series can he connected to inputs and outputs of TTL lC s without the need of additional interfacing circuits.
- Newer versions of CMOS are the high-speed series 74VHC and its TTL compatible version 74VHCT.
- The CMOS fabrication process is simpler than that of TTl.. and pro vides a greater packing density. Thus, more circuits can be placed on a given area of silicon at a reduced cost per function.
- This property together with the low power dissipation of CMOS circuits good noise immunity, and reasonable propagation delay, makes CMO S the most popular standard as a digital logic family.

Unit –III

Analysis and Synthesis of Sequential Logic Circuits

Sequential logic Circuit (SLC)

A sequential logic circuit is a digital circuit in which the output at any point of time depends on present inputs and past outputs. Sequential circuits include memory elements along with combinational logic circuits. The memory elements are connected to the combinational logic circuit as a feedback path. **Fig 1** shows the block diagram of a sequential logic circuit.

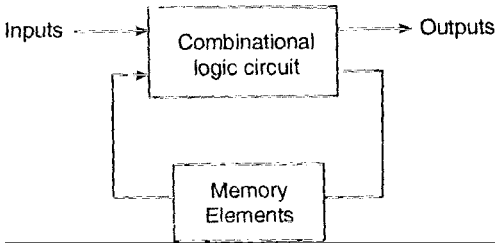


Fig. 1 Block diagram of sequential logic circuit.

Finite State Machines

Classification of SLC

The sequential circuits can be classified into two categories depending on the timing of their signals

1. Synchronous sequential logic circuit
2. Asynchronous sequential logic circuit

In case of synchronous sequential circuits, it is assumed that the behavior of the system synchronized by a clock. The system behavior is determined by the values of present state and external input signals at discrete instants of time.

In case of asynchronous sequential logic circuits the order in which input signals change affected network behavior. Further more, these changes are allowed to occur at any instant of time.

Mealy Model

Fig. _2____shows the clocked synchronous sequential Mealy machine. The output of mealy machine is the function of present inputs and present state (Flip flop outputs).

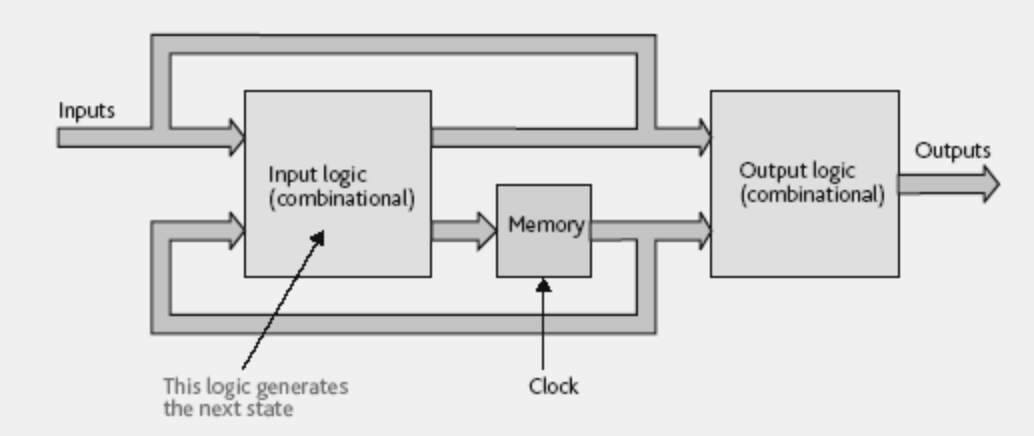


Fig _2____ model for mealy machine

Moore Machine

Fig. __3___ shows the block diagram of a Moore machine. The output of Moore machine depends only op the present state. So the output of Moore machine is a function of its present state

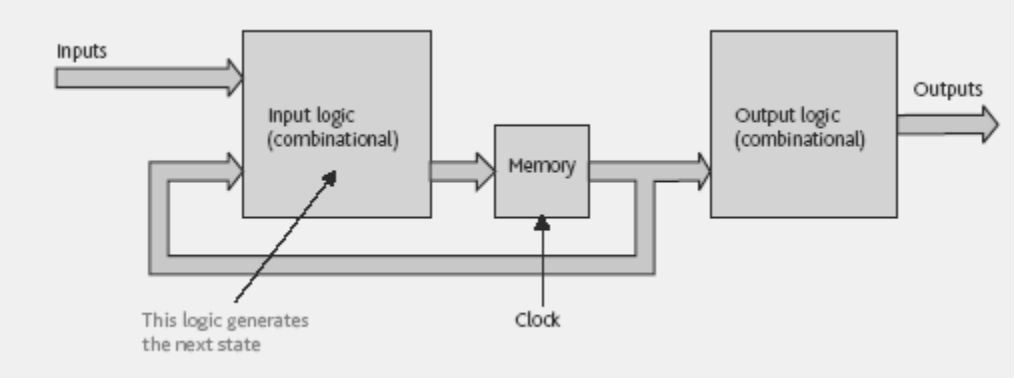


Fig __3___ model for Moore machine

Difference between Moore and Mealy Machine

SNo.	*Moore machine*	*Mealy machine*
1.	The output of this machine is the function of the present state only	Its output is function of input as well as present state present
2.	Input changes do not affect the output	Input changes may affect the output of the circuit
3.	It requires more number of states for implementing same function	It requires less number of states for implementing same function
4	Speed is high	Speed is low
5	Design process is very complicate	Less complex than Moore design

ANALYSIS OF SYNCHRONOUS SEQUENTIAL CIRCUITS

- The behavior of sequential circuit can be determined from the inputs, the output and state of its flip flops.
- The outputs and next state are both a function of its inputs and the present state.
- The analysis of a sequential circuit consists of obtaining a table or diagram for the time sequence of inputs, outputs and internal states.
- The analysis of the clocked sequential circuits can be done by following the procedure as

Analysis Procedure

1. Identify type of circuit either Mealy or Moore circuit
2. Derive excitation equation (Boolean expression)
3. Derive next state and output equations
4. Generate state table
5. Generate state diagram

Analysis of Example Sequential Logic Circuit

Figure 7.6 shows a clocked sequential circuit. It has one input variable X, output variable Y and two clocked JK flin flops. The flip flops are labelled as A and *B* and their outputs are labelled as A and A, B and B respectively.

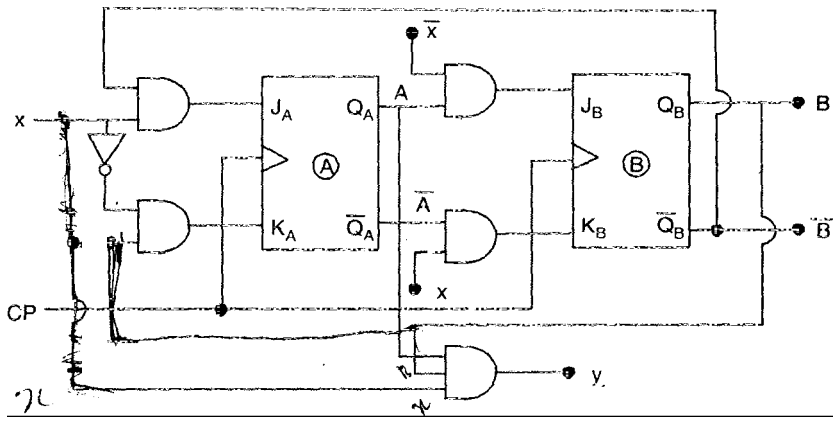


Fig __4_

Step 1 : Type of circuit

The output of given logic circuit y (Fig. __4____) depends on present input and also on present state (Flip flop outputs) of flip flops, so the given sequential logic circuit is Mealy sequential machine.

Step 2 : Excitation equations

The excitation equations or Boolean expressions of flip flops A and *B* are obtained. The equations will be in the form of present states A and *B* and external input x. Since there are two JK flip flops which have output A and *B.* Therefore the excitation equation (equation formed for flip flop input)

For Flip flop – A

$$J_A = x\overline{B} \quad \text{and} \quad K_A = \overline{x}B$$

For Flip flop – A

$$J_B = \overline{x}A \quad \text{and} \quad K_B = x\overline{A}$$

Step 3 : Next state equations

The state equations can be derived directly from the logic diagram. Looking at Fig. ____, we can see that the signal for J input of the flip flop A is generated by the function $x\overline{B}$ and the signal for input K by the function $\overline{x}B$. Substituting $J_A = x\overline{B}$ and $K_A = \overline{x}B$ into a JK flip flop characteristic equation given by

Characteristic Equation of JK Flip flop

$$Q_{n+1} = J\overline{Q_n} + \overline{K}Q_n$$

Substitute the J_A and K_A in the above equation to obtain the state equation of fkip-flop A

State equation of flip flop A

$$A_{n+1} = \left(\overline{B}x\right)\overline{Q_n} + \overline{\overline{x}B}Q_n \quad \text{where } Q_n = A$$

$$A_{n+1} = \left(\overline{B}x\right)\overline{A} + \overline{\overline{x}B}A$$

Simplify the above equation we get

$$A_{n+1} = A\overline{B} + Ax + \overline{B}x$$

Similarly we get next state equation for flip-flop B

$$B_{n+1} = AB + A\overline{x} + B\overline{x}$$

Output equation $y = A\overline{B}x$

Step 4 : State Table

The Table ____ shows the state table for the given sequential logic circuit. It represents the relationship between input, output, and flipflop states. It consists of three columns: Present state, next state and output.

Present state: it specifies the state of flip-flop before occurrence of a clock pulse

Next state :it is the state of flip flop after the application of clock

Output: this section gives the value of the output variables during the present state. Both next state and output section have two columns representing two possible input conditions x=0 and x=1.

State Table

Present state	Next state		Output Y	
	x=0	x=1	x=0	x=1
AB	AB	AB		
00	00	10	0	0
01	01	00	0	0
10	11	10	0	1
11	01	11	0	0

Step 5 State diagram

State diagram is a graphical representation of a state table. Fig. ____shows the state diagram for sequential circuit. Here each state is represented by a circle, and transition between states is indicated by directed lines connecting the circles. The binary number inside each circle identifies the state represented by the circle. The directed lines are labelled with two binary numbrs separated by a symbol `I' (slash). The input value that causes the state transition is labelled first and output value is next.

0/0

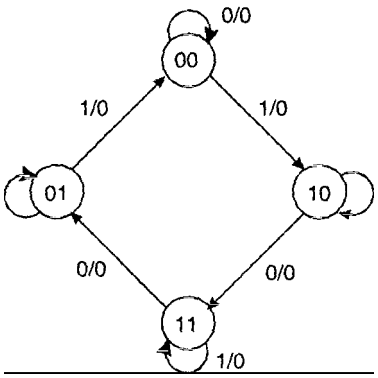
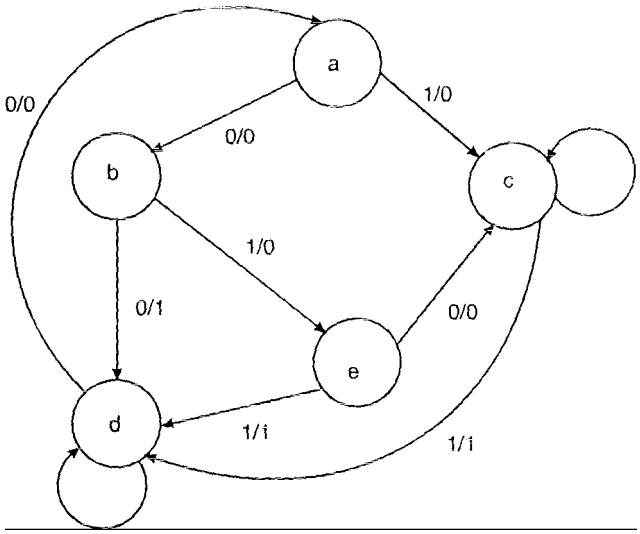


***Fig__5___ State* diagram.**

1,5 STATE REDUCTION

- Any logic design process must consider the problem of minimizing the cost of the final circuit.
- One way to reduce the cost is by reducing the number of flip flops, $i.e.$ by reducing the number of states.
- The state reduction technique basically avoids the introduction of redundant equivalent states. The reduction of redundant states reduces the number of flip flops and logic gates required, thus reducing the cost of the final circuit.
- Two states are said to be redundant or equivalent, if every possible set of inputs generate exactly the same outputs and the same next states.
- When two states are equivalent one of them can be removed without altering input output relationship. Let us consider the state diagram as shown in Fig. 7.8.
- The states are denoted by letter symbols instead of their binary values because instate reduction technique internal states are important, but input output sequences are important. The procedure contains two steps.



Step 1: Finding State table for the given state diagram
First the given state diagram is converted into a state table.

Present state	Next state		output	
	x=0	x=1	x=0	x=1
a	**b**	**c**	**0**	**0**
b	**d**	**e**	**1**	**0**
c	**c**	**d**	**0**	**1**
d	**a**	**d**	**0**	**0**
e	**c**	**d**	**0**	**1**

Step 2 : Finding equivalent states

It is determined from the state diagram. The equivalent state table is given for the above state diagram as

The two present states go to the same next state and have the same output for both the input combinations. We can easily find this from the state table, states c and e are equivalent. This is because both c and *e* states go to states c and d outputs of 0 and 1 for x = 0, x = 1 respectively. Therefore, the state *e* can be removed and replaced by c. The final reduced table and state diagram are given in the table _____ and Fig._____. The second row have *e* state for the input x = l, it is replaced by c because the states c and *e* are equivalent.

Reduced state table

Table 7.2

	Next state		*Output*	
Present state	*x=0*	*x=1*	*x=0*	*x=1*
a	*b*	*c*	*0*	*0*
b	*d*	*c*	*1*	*0*
c	c	*d*	*0*	*1*
d 1/0	*a*	*d*	*0*	*0*

Reduced State Diagram

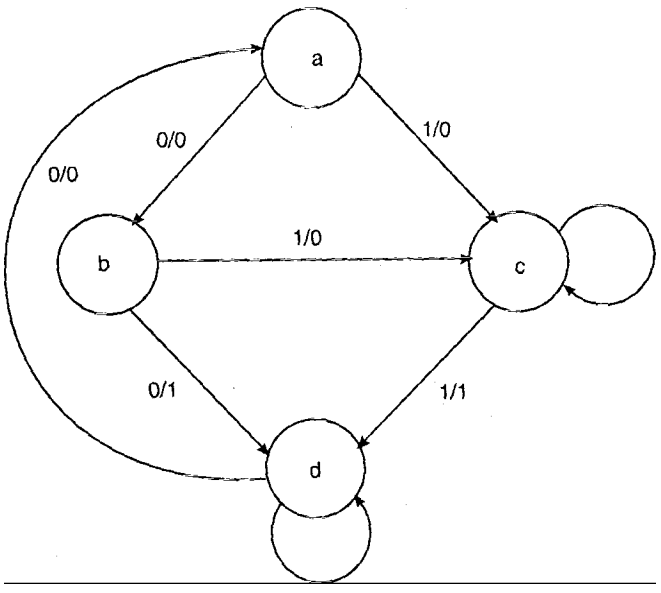


Fig 6

DESIGN PROCEDURE FOR CLOCKED SEQUENTIAL CIRCUIT

The following steps are followed to design the clocked sequential logic circuit.

1. Obtain the state table from the given circuit information such as a state diagram, a timing diagram or description.
2. The number of states may be reduced by state reduction technique.
3. Assign binary values to each state in the state table.
4. Determine the number of flip flops required and assign a letter symbol to each flip flop.
5. Choose the flip flop type to be used according to the application.
6. Derive the excitation table from the reduced state table.
7. Derive the expression for flip flop inputs and outputs using k-map simplification (The present state and inputs are considered for k-map simplification) and draw logic circuit

using flip flops and gates.

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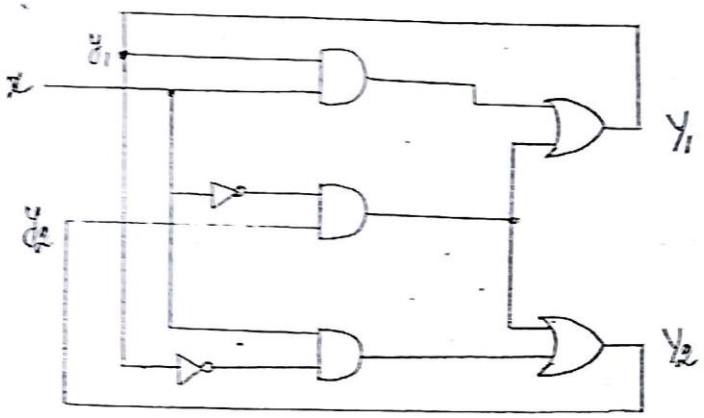
4:20

Analysis Procedure of Asynchronous Circuit

The analysis procedure will be presented by means of i) transition table, ii) flow table and iii) the stability of asynchronous sequential circuits.

Transition Table



* The circuit consists of one i/p variable x and two internal states.

* The internal states have two excitation variables, Y_1 & Y_2 and two secondary variables y_1 & y_2

* The delay associated with each feed back loop is obtained from the propagation delay b/w each y i/p and its corresponding Y o/p.

Viru Radhi

(4)

Asynchronous Sequential Logic

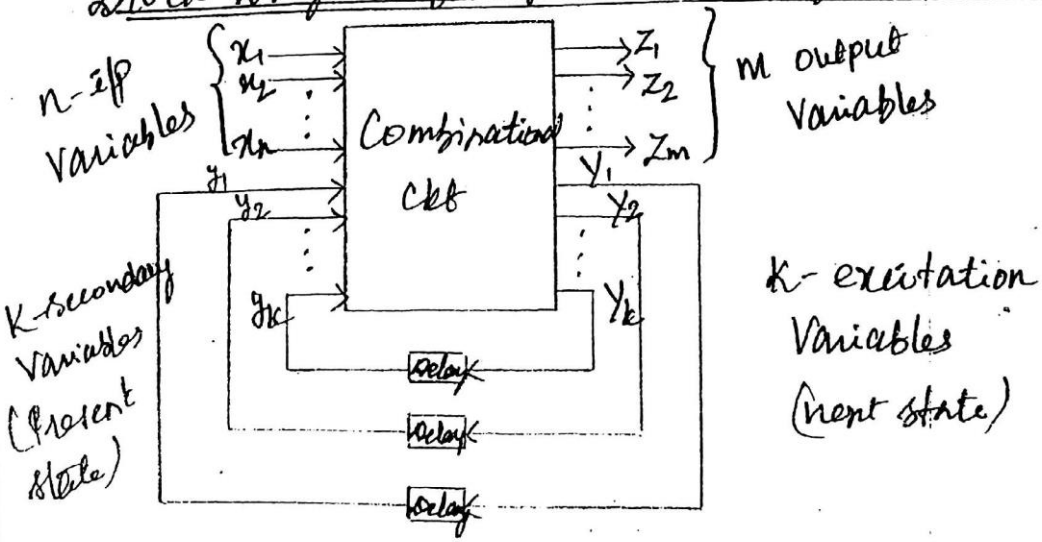
* It consists of a combinational ckt and delay elements connected to form feedback loops.

* There are n i/p variables, m o/p variables and k internal states.

* The delay elements provides short-term memory for the sequential ckt.

* The present state and next state variables in asynchronous sequential ckts are called as secondary variables and excitation variables.

Block diagram of asynchronous sequential circuit



* When the i/p variable changes in value, the y secondary variables do not change instantaneously.

* It takes a certain amount of time for the signal to propagate from the i/p terminals, through the combinational ckt, to the Y excitation variables, which generate new values for the next state.

* These values propage through the delay elements and become the new present state for the secondary variables.

* For a given value of i/p variables, the system is "stable" if the circuit reaches a steady state condition with

$Y_i = Y_i$ for $i = 1, 2, \ldots k$, Otherwise the ckt is in a continuous transition and it is said to be "Unstable".

Fundamental Mode:-

Only one i/p variable can change at any one time and the time b/w two i/p changes must be longer than the time it takes the circuit to reach a stable state

* Only one i/p variable can change at any one time; simultaneous changes of two or more variables are prohibited.

Types of Races

1. Non-critical Race
2. Critical Race.

Non Critical Race:-

: If the final stable state that the circuit reaches does not depend on the order in which the state variables change, the race is called a non critical race.

Critical Race:-

If the final stable state (two or more stable different stable state) that the circuit reaches depends on the order in which the state variables change, the race is called a critical race.

* for proper Operation critical races must be avoided.

Examples of non-critical races:-

* Starting with the total stable state $y_1 y_2 x_1 x_2 = 0000$, and change the i/p from 0 to 1
* The state variables must then change from 00 to 11, which defines a race condition.

* The possible transition are either they can change simultaneously from 00 to 11, or they may

y_1y_2 \ x	0	1
00	(00)	11
01		11
11		(11)
10		11

final total stable state is $y_1y_2x = 111$.

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10 \rightarrow 11$

y_1y_2 \ x	0	1
00	(00)	11
01		(01)
11		01
10		11

final total stable state is $y_1y_2x = 011$

Possible Transitions
$00 \rightarrow 11 \rightarrow 01$
$00 \rightarrow 01$
$00 \rightarrow 10 \rightarrow 11 \rightarrow 01$

change in sequence from 00 to 01 and then to 11, or they may change in sequence from 00 to 10 and then to 11.

* In all cases, the final stable state is the same, so the race is non-critical.

Examples for Critical Races:-

y_1y_2 \ x	0	1
00	(00)	11
01		(01)
11		(11)
10		(10)

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01$
$00 \rightarrow 10$

y_1y_2 \ x	0	1
00	(00)	11
01		11
11		(11)
10		(10)

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10$

4.22

Procedure for obtaining transition table from the ckt diagram of an asynchronous circuit:-

1. Determine all feedback loops in the ckt
2. Designate the o/p of each feedback loop with variable y_i and its corresponding o/p with Y_i for $i = 1, 2, \ldots k$, where k is the no. of feedback loops in the circuit.
3. Derive the Boolean functions of all Y's as a function of the external i/ps and the y's.
4. Plot each Y function in a map, using the y variables for the rows and the external i/ps for the columns.
5. Combine all the maps into one table showing the value of $Y = Y_1 Y_2 \ldots Y_k$ inside each square.
6. Circle those values of Y in each square that are equal to the value of $y = Y_1 Y_2 \ldots Y_k$ in the same row.

4.23

Primitive flow Table:

(Flow table which has only one stable state in each row is called as primitive flow table.)

Example -2 shows a flow table with more than one stable state in the same row.

* It has two states, a & b; two i/ps x_1 and x_2; and one o/p Z.

* The binary value of the o/p variable is indicated inside the square next to the state symbol and is separated from the state symbol by a comma.

* From the table, the behaviour of the ckt is observed as;

* If $x_1 = 0$, the ckt is in state a.

* If x_1 goes to 1 while x_2 is 0, the ckt goes to state b.

* With i/ps $x_1 x_2 = 11$, the ckt may be either in state a or in state b.

If it is in state a, the o/p is 0, and if it is in state b, the o/p is 1.

* State b is maintained if the i/ps changes from 10 to 11.

* In asynchronous ckt, the internal state can change immediately after a change in the i/p. Because of this rapid change, it is sometimes convenient to combine the internal state with the i/p value together and it is called as Total state of the ckt.

* This ckt has four stable total state - $y_1 y_2 x$ = 000, 011, 110 and 101 and four unstable total states - 001, 010, 111, 100.

State Table:

* If we regard the secondary variables as the present state and the excitation variables as the next state, state table is obtained.

* In the asynchronous transition table, there usually is at least one next-state entry that is the same as the present-state value in each row.

State table for the circuit

Present State	Next state	
	X=0	X=1
00	00	01
01	11	01
10	00	10
11	11	10

Flow Table:-

In Asynchronous Sequential Ckts, the states are represented by letter symbols without making specific reference to their binary values. Such a table is called a flow Table

* The flow table also includes the o/p values of the ckt for each stable state.

Examples of flow table:-

y \ x	0	1
a	(a)	b
b	c	(b)
c	(c)	d
d	a	(d)

4-states with 1 i/p

Example 1

x_1x_2 / y_1y_2	00	01	11	10
a	(a),0	(a),0	(a),0	b,0
b	a,0	a,0	(b),1	(b),0

2-states with 2-i/ps and 1 o/p.

Example-2.

* Example 1 has 4 states, designated by the letters a, b, c, & d

* Assigning the binary values to the states; a=00; b=01; C=11 and d=10.

* The table of example-1 is called a "Primitive flow table" because it has only one stable state in each row

4-21

* The transition table shows the value of $Y = Y_1 Y_2$ inside each square

* The first bit of Y is obtained from the value of Y_1, and the second bit is obtained from the value of Y_2 in the same square position.

K-Map for Y_1

y_1y_2 \ x	0	1
00	0	0
01	1	0
11	1	1
10	0	1

$Y_1 = xy_1 + x'y_2$

K-Map for Y_2

y_1y_2 \ x	0	1
00	0	1
01	1	1
11	1	0
10	0	0

$Y_2 = xy_1' + x'y_2$

Transition Table

y_1y_2 \ x	0	1
00	(00)	01
01	11	(01)
11	(11)	10
10	00	(10)

* For a state to be stable, the Secondary variables must match the excitation variables (ie) the value of Y must be the same as that of y; $Y = Y_1 Y_2$)

* Those entries in the transition table where $Y = y$ are circled to indicate a stable condition. An Uncircled entry represents an unstable state.

* The analysis of the circuit is done by considering the excitation variables as o/ps and secondary variables as i/ps.

* From the diagram.

$$\therefore Y_1 = xy_1 + x'y_2$$

$$Y_2 = xy_1' + x'y_2$$

Truth Table

Plotting truth table for Y_1 & Y_2

Truth Table for Y_1.

y_1	y_2	x	Y_1
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Truth Table for Y_2

y_1	y_2	x	Y_2
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

* K-Map is plotted for Y_1 & Y_2.

* Transition table is obtained from the maps by combining the binary values corresponding squares.

* The possible transition are either they can change simultaneously from 00 to 11, or they may

y_1y_2 \ x	0	1
00	(00)	11
01		11
11		(11)
10		11

final total stable state is $y_1y_2x = 111$.

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10 \rightarrow 11$

y_1y_2 \ x	0	1
00	(00)	11
01		(01)
11		01
10		11

final total stable state is $y_1y_2x = 011$

Possible Transitions
$00 \rightarrow 11 \rightarrow 01$
$00 \rightarrow 01$
$00 \rightarrow 10 \rightarrow 11 \rightarrow 01$

change in sequence from 00 to 01 and then to 11, or they may change in sequence from 00 to 10 and then to 11.

* In all cases, the final stable state is the same, so the race is non-critical.

Examples for Critical Races:-

y_1y_2 \ x	0	1
00	(00)	11
01		(01)
11		(11)
10		(10)

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01$
$00 \rightarrow 10$

y_1y_2 \ x	0	1
00	(00)	11
01		11
11		(11)
10		(10)

Possible Transitions
$00 \rightarrow 11$
$00 \rightarrow 01 \rightarrow 11$
$00 \rightarrow 10$

4.24

Race Conditions:-

A Race condition is said to be exist in an asynchronous sequential circuit when two or more binary state variables change value in response to a change in an i/p variable.

* Due to unequal delay, a race condition may cause the state variables to change in an unpredictable manner.

Example:-

* if the state variables must change from 00 to 11, the difference in delays may cause the first variable to change sooner than the second with the result that the state variables changes in sequence from 00 to 10 and then to 11.

(e) $00 \rightarrow 10 \rightarrow 11$.

* If the second variable changes sooner than the first, the state variables will change from 00 to 01 and then to 11.

(e) $00 \rightarrow 01 \rightarrow 11$.

* Thus, the order by which the state variables change may not be known in advance

* The dot stays in state a if the i/p changes from 01 to 11.

Note:

In fundamental mode two i/p variables cannot be changed simultaneously. (ie) from 00 to 11.

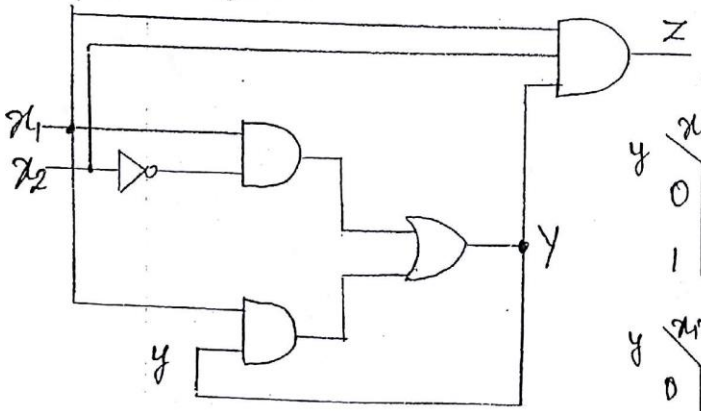
Flow table into Transition table:-

By assigning a distinct binary values to each state, flow table is converted into transition table, from which logic diagram can be obtained.

* By assigning binary 0 to state a and binary 1 to state b, the transition table is drawn

* The o/p map is obtained directly from the o/p values in the flow table.

Logic Diagram



Transition Table

$Y = x_1x_2' + x_1y$

y \ x1x2	00	01	11	10
0	(0)	(0)	(0)	1
1	0	0	(1)	(1)

y \ x1x2	00	01	11	10
0	0	0	0	0
1	0	0	1	0

K-Map for o/p $z = x_1x_2y$

Hazards:-

The unwanted switching transients that may appear at the o/p of the circuit are called Hazards.

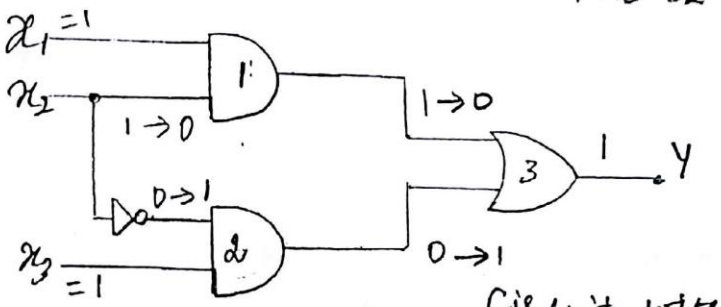
* The Hazards cause the circuit to malfunction.

* The main cause of Hazards is the different propagation delays at different paths.

* Hazards occurs in the combinational ckt. where they may cause a temporary false o/p value.

Hazards in Combinational Circuits:-

AND-OR Circuit



Circuit with Hazards.

* Initially, i/ps x_1=1, x_2=1 and x_3=1

* This causes the o/p of gate 1 to be 1, that of gate 2 to be 1, and the o/p of the circuit to be equal to 1.

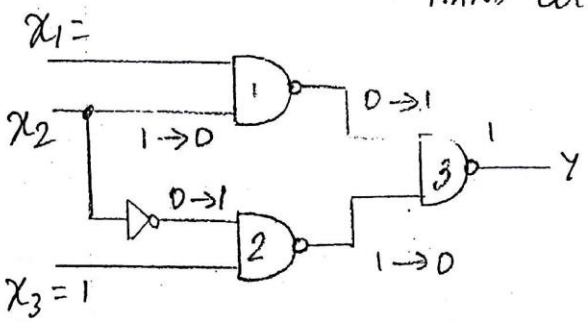
* Now Consider a Change in x_2 from 1 to 0. Then the o/p of gate 1 Changes to 0 and that of gate 2 Changes to 1, leaving the o/p at 1.

* However the o/p may momentarily go to 0 if the propagation delay through the inverter is taken into Consideration.

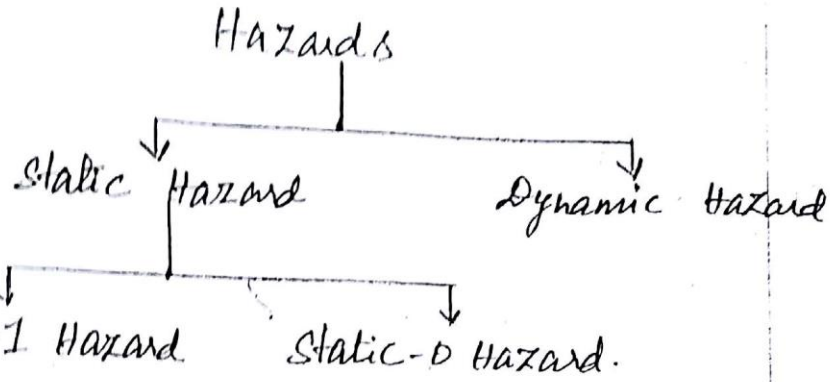
* The delay in the Inverter may Cause the o/p of gate 1 to Change to 0 before the o/p of gate 2 Changes to 1.

* In that ~~gate~~ Case, both i/ps of gate 3 are momentarily equal to 0, Causing the o/p to go to 0 for the short time during which the i/p signal from x_2 is delayed while it is Propagating through the inverter Circuit.

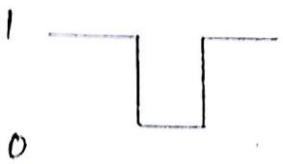
NAND Circuit



Types of Hazards:-



Static-1 Hazard:- (1 → 0).

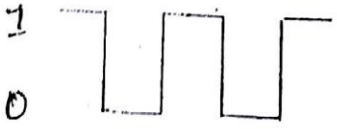


In a combinational circuit, if o/p goes momentarily 0, when it should remain a 1, the hazard is known as Static-1 Hazard.

Static-0 Hazard:- (0 → 1).

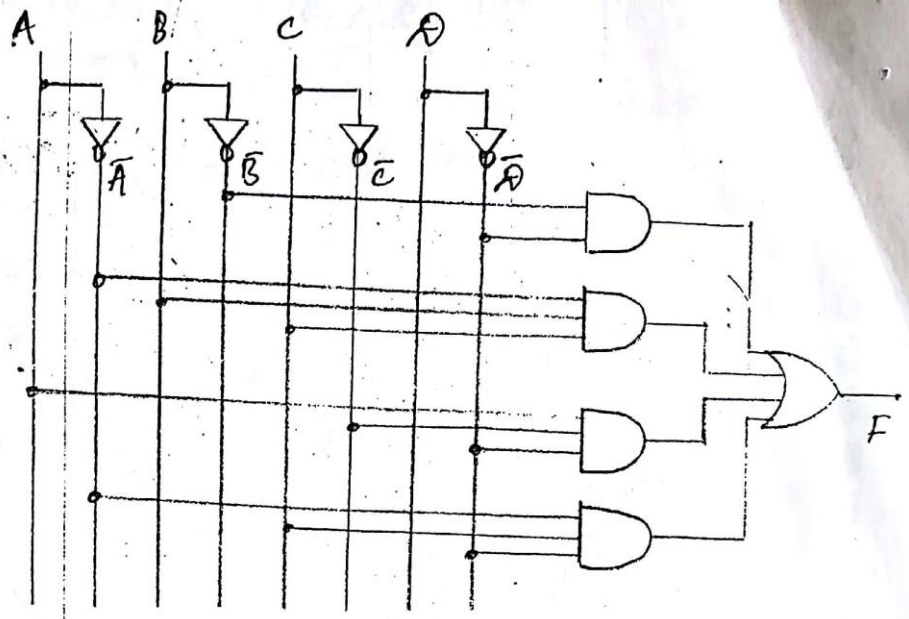
In a combinational ckt if o/p goes momentarily 1, when it should remain a 0, the Hazard is known as Static 0 Hazard.

Dynamic Hazard:



In a combinational ckt if o/p changes three or more times from 1 to 0 or from 0 to 1, the Hazard is known as Dynamic Hazard.

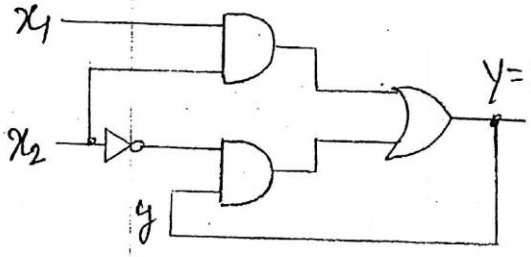
Hazard free Circuit



Hazards in Sequential Circuits:-

* If a momentary incorrect signal is fed back in an Asynchronous sequential circuits, it may cause the circuit to go to the wrong stable state.

Logic Diagram



y \ x_1x_2	00	01	11	10
0	(0)	(0)	1	(0)
1	(1)	0	(1)	(1)

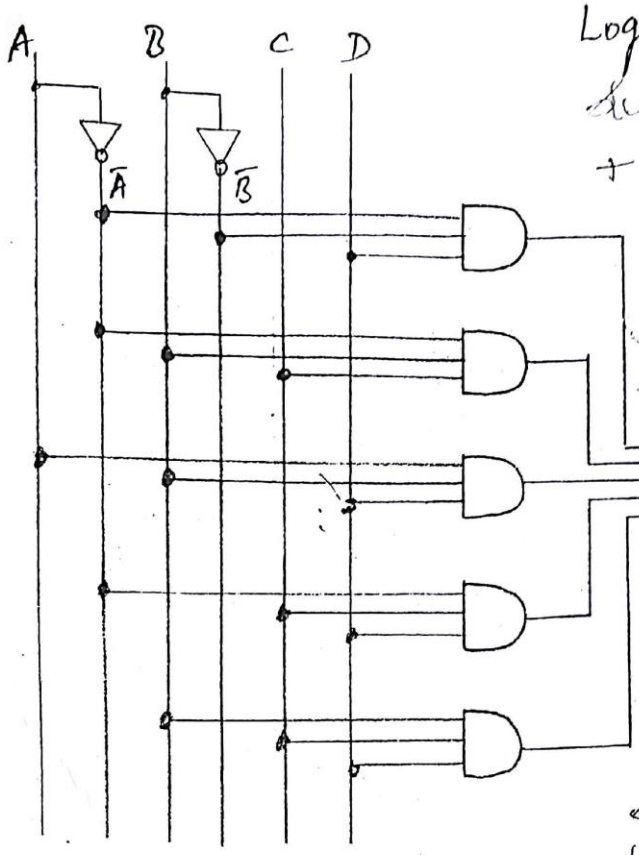
Transition table

y \ x_1x_2	00	01	11	10
0			(1)	
1	(1)		(1)	(1)

K-Map for Y

* Because of the Hazard, o/p Y may go to 0

* If the Ckt is in total stable state $yx_1x_2 = 111$ and i/p x_2 changes from 1 to 0, the next total stable state should be 110.



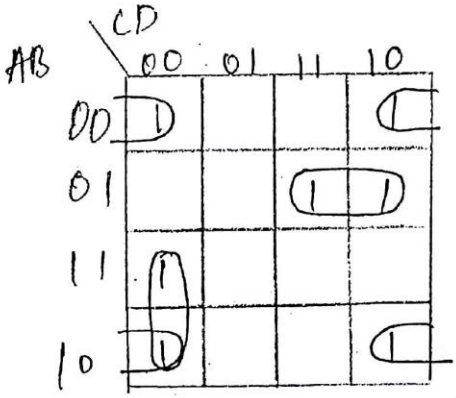
Logic Diagram

Hazard free ckt for the given function.

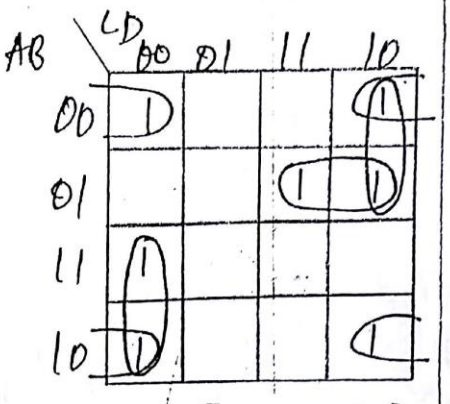
Example :2

For the Boolean function obtain the Hazard free circuit; $F(A,B,C,D) = \Sigma m(0,2,6,7,8,10,12)$

Sol



$F = \bar{B}\bar{A} + \bar{A}BC + A\bar{C}\bar{D}$



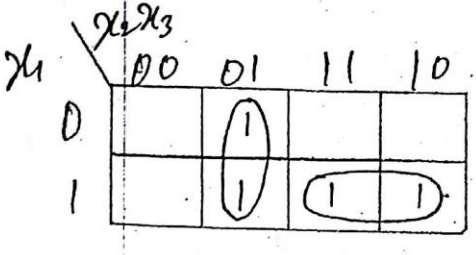
$F = \bar{B}\bar{D} + \bar{A}BC + A\bar{C}\bar{D} + \bar{A}C\bar{D}$

Eliminating a Hazard:-

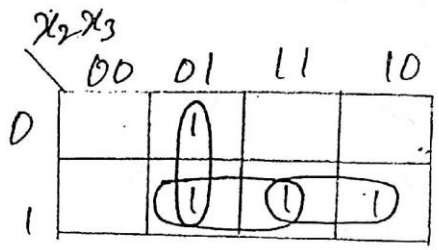
Hazards can be eliminated by enclosing more no. of minterms or maxterms

Eg:-

If the ckt has minterms $x_1x_2 + \bar{x}_2x_3$, then these two minterms must be enclosed by introducing another minterm x_1x_3.



$Y = x_1x_2 + \bar{x}_2x_3$



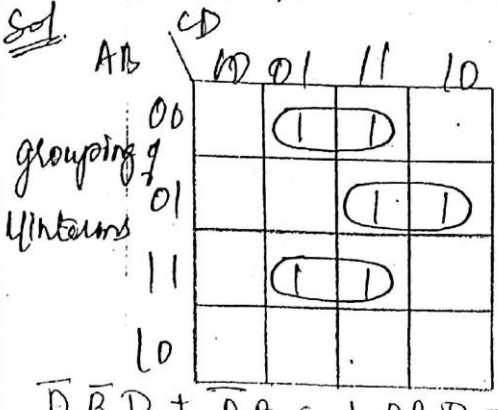
$Y = x_1x_2 + \bar{x}_2x_3 + x_1x_3$

Example: 1

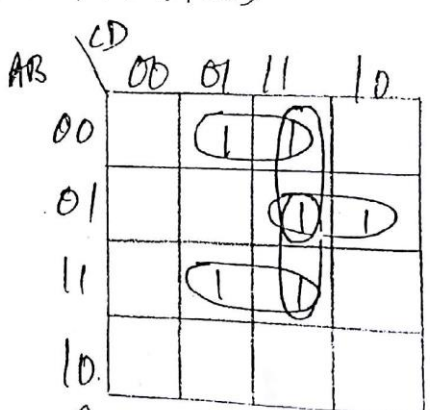
For the boolean function obtain the hazard free circuit.

$F(A,B,C,D) = \Sigma m(1,3,6,7,13,15)$

Sol



$\bar{A}\bar{B}D + \bar{A}BC + ABD = F$

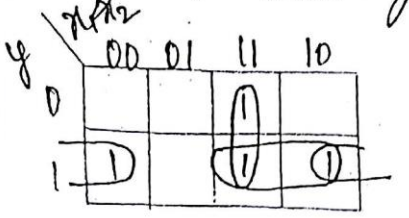


Enclosing Minterms

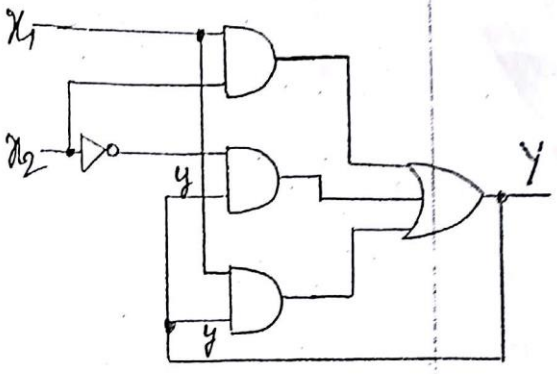
momentarily.

* If this false signals feed back into gate 2 before the o/p of the inverter goes to 1, the o/p of gate 2 will remain at 0 and the circuit will switch to the incorrect total stable state 010.

* This malfunction can be eliminated by adding an extra gate.



$$Y = x_1x_2 + \bar{x}_2y + x_1y$$



To design a sequential circuit that will output 1 only when the sequence 1101 is received and will ignore any other pulses

The procedural steps are as follows:

1. Obtain a primitive flow table from the given design specifications. This is the most difficult part of the design because it is necessary to use intuition and experience to arrive at the correct interpretation of the problem specification

2. Reduce a flow-table by merging rows in the primitive flow table. A formal procedure for merging rows in the flow table.

3. Assign binary state variables to each row of the reduced flow table to obtain the transition table

4. Assign output values to the clashes associated with the unstable state to obtain the output maps.

5 Simplify the boolean expr. of the excitation and output variable and draw the logic diagram. This logic diagram can be drawn using SR latches, as

Design Example:

It is necessary to design a gated latch circuit with two inputs, G(gate) and D(data) and one output, Q. Binary information present at

the D input is transferred to the Q output when G1 is equal to 1. The Q output will follow the input as long as G1 = 1. When G1 = 0, the information that was present at the D input at the time the transition occurred is retained at the Q output. A gated latch is a memory element that accepts the value of D when G1 = 1 and retains this value after G1 goes to 0. Once G1 = 0, a change in D does not change the value of the output Q.

Each row in the table specifies a total state, which consists of a letter designation for the internal state and a possible input combination for D and G1. The output Q is also shown for each total state. We start with the two total states that have G1 = 1.

From the design specifications, that Q = 0 if DG1 = 01 and Q = 1 if DG1 = 11 because D must be equal to Q when G1 = 1. We assign these conditions to states a and b. When G1 goes to 0, the output depends on the last value of D. Thus if the transition of DG1 is from 01 to 00 to 10, then Q must remain 0 because D is 0 at the time of the transition from 1 to 0 in G1. If the transition of DG1 is from 11 to 10 to 00, then Q must remain 1. Transitions of two input variables, as from 01 to 10 or from 11 to 00 are not allowed

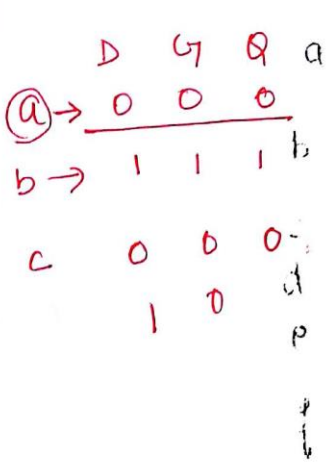
in fundamental - mode operation

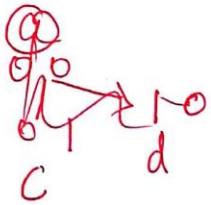
State	Input D	Input G_1	Output Q	comments
a ✓	0	1	0	D = Q because G_1 = 1
b ✗	1	1	1	D = Q, G_1 = 1
c ✓	0	0	0	After state a or d
d ✓	1	0	0	After state c
e ✗	1	0	1	After state b or f
f ✗	0	0		After state e.

Non Critical.

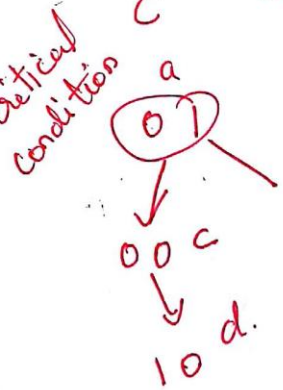
From the Table I write primitive flow table for the gated Latch.

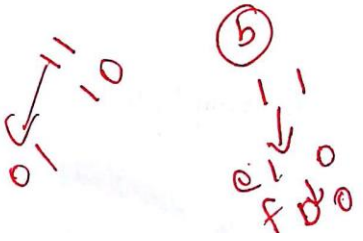
	00	01	11	10
a	c, –	(a), 0	b, –	–, –
b	–, –	a, –	(b), 1	e, –
c	(c), 0	a, –	–, –	d, –
d	c, –	–, –	b, –	(d), 0
e	f, –	–, –	b, –	(e), 1
f	(f), 1	a, –	–, –	e, –





Critical condition





Reduction of the Primitive flow Table

DG

	00	01	11	10
a	c,-	(a),0	b,-	-,-
c	(c),0	a,-	-,-	d,-
d	c,-	-,-	b,-	(d),0

DG

	00	01	11	10
b	-,-	a,-	(b),1	
e	f,-	-,-	b,-	
f	(f),1	a,-	-,-	

a) States that are candidates for merging.

DG

	00	01	11	10
a,c,d	(c),0	(a),0	b,-	(d),0
b,e,f	(f),1	a,-	(b),1	(e),1

DG

	00	01	11	10
a	(a),0	(a),0	b,-	(a),0
b	(b),1	a,-	(b),1	(b),1

a = c = d,
b = e = f

b) Reduced table

Transition table and logic diagram

assign a = 0, b = 1

DG

y	00	01	11	10
0	00	00	1,-	00
1	1,1	0,-	11	11

DG

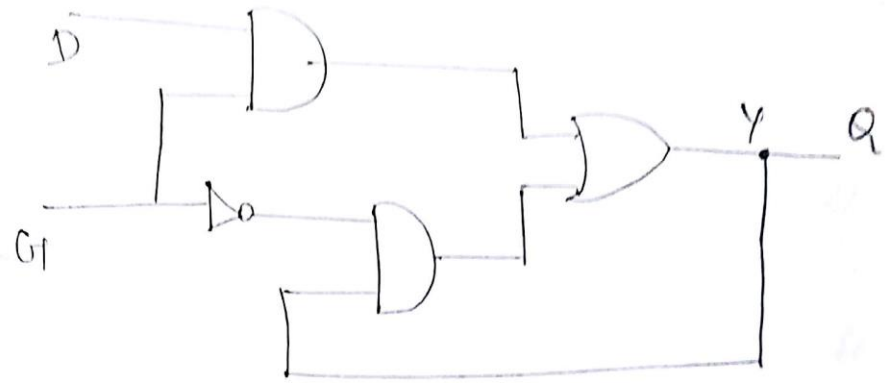
y	00	01	11	10
0	0	0	1	0
1	1	0	1	1

a) $Y = DG + G'y$

b) $Q = Y$

The simplified boolean function for Y from k ma

Logic dig:



$Y = DG_1 + G_1' y$, $Q = Y$.

Analysis of Asynchronous Sequential Circuit:

The

UNIT – V

PROCESSOR AND CONTROL UNIT DESIGN

Processor and control unit design: Registers – Register transfer logic – inter register transfer, bus transfer and memory transfer, Arithmetic logic and shift micro operations –Macro operations – Processor logic design – Processor organization- Bus organization –Processor unit employing a scratch pad memory – Accumulator– Design of ALU – Design of status register- Design of processor unit with control variables – Design of accumulator– Control logic design – Single flip-flop/state method –Sequence register and decoder method.

REGISTER-TRANSFER LOGIC

- Digital systems are composed of modules that are constructed from digital components, such as registers, decoders, arithmetic elements, and control logic
- The modules are interconnected with common data and control paths to form a digital computer system
- The operations executed on data stored in registers are called *microoperations*
- A microoperation is an elementary operation performed on the information stored in one or more registers
- Examples are shift, count, clear, and load
- Some of the digital components from before are registers that implement microoperations
- The internal hardware organization of a digital computer is best defined by specifying
  - The set of registers it contains and their functions
  - The sequence of microoperations performed on the binary information stored
  - The control that initiates the sequence of microoperations
- Use symbols, rather than words, to specify the sequence of microoperations
- The symbolic notation used is called a *register transfer language*
- A programming language is a procedure for writing symbols to specify a given computational process
- Define symbols for various types of microoperations and describe associated hardware that can implement the microoperations

Definition for RTL

A symbolic notation for representing registers, for specifying operations on the contents of registers, and for specifying control functions. This symbolic notation is called a *register-transfer language* or *computer hardware description language.*

- A statement in a register-transfer language consists of a control function and a list of microoperations.
- The control function specifies the control condition and timing sequence for executing the listed microoperations.

The microoperations specify the elementary operations to be performed on the information stored in registers.

The types of microoperations most often used in digital systems

1. **Interregister-transfer microoperations** do not change the information content when the binary information moves from one register to another.
2. **Arithmetic microoperations** perform arithmetic on numbers stored in registers.
3. **Logic microoperations** perform operations such as AND and OR on individual pairs of bits stored in registers of microoperations
4. **Shift microoperations** specify operations for shift registers.

INTERREGISTER TRANSFER

- The registers in a digital system are designated by capital letters to denote the function of the register.
- For example, the register that holds an address for the memory unit is usually called the memory address register and is designated *MAR* .
- Other designations for registers are A, B, R1, R2, and IR.

Figure 5.1 shows four ways to represent a register in block diagram form.

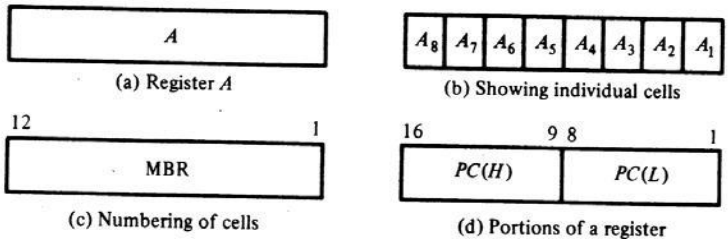


Fig 5.1 register representation

Basic *symbols* for register-transfer logic		
Symbol	Description	Examples
Letters (and numerals)	Denotes a register	*A, MBR, R2*
Subscript	Denotes a bit of a register	A_2, *Bb*
Parentheses ( )	Denotes a portion of a register	*PC(H), MBR(OP)*
Arrow <--	Denotes transfer of information	*AF-B*
Colon :	Terminates a control function	z' T_o:
Comma ,	Separates two microoperations	*A~B,Be-A*
Square brackets [ ]	Specifies an address for memory transfer	*MBR <-- M[MAR]*

Information or data transfer

Information transfer from one register to another is designated in symbolic form by means of the *replacement operator.* The statement:

$A \leftarrow B$ (statement without control statement)

The above statement denotes the transfer of the *contents* of register *B* into register *A.* It designates a replacement of the contents of A by the contents of *B.* By definition, the contents of the source register *B* do not change after the transfer.

Statement with control Signal

The condition that determines when the transfer is to occur is called a *control function.* A control function is a Boolean function that can be equal to 1 or 0. The control function is included with the statement as follows:

$x' T : A \leftarrow B$

The control function is terminated with a colon. It symbolizes the requirement that the transfer operation be executed by the hardware only when the Boolean function x'T, = 1, i.e., when variable x = 0 and timing variable T, = 1.

Example of Hardware representation

- Every statement written in a register-transfer language implies a hardware construction for implementing the transfer.
- Figure 5.*2* shows the implementation of the statement of $A \leftarrow B$.
- The outputs of register *B* are connected to the inputs of register *A,* and the number of lines in this connection is equal to the

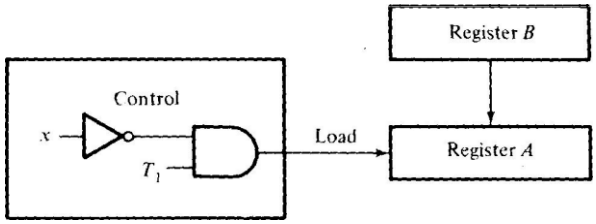


Fig 5.2 Hardware implementation of the statement

ARITHMETIC, LOGIC, AND SHIFT MICROOPERATIONS

- The interregister-transfer microoperations do not change the information content when the binary information moves from the source register to the destination register.
- All other microoperations change the information content during the transfer.
- Among all possible operations that can exist in a digital system, there is a basic set from which all other operations can be obtained.
- In this section, we define a set of basic microoperations, their symbolic notation, and the digital hardware that implements them.
- Other microoperations with appropriate symbols can be defined if necessary to suit a particular application.

Arithmetic Microoperations

- There are four categories of the most common microoperations:
  - **Register transfer**: transfer binary information from one register to another
  - **Arithmetic:** perform arithmetic operations on numeric data stored in registers
  - **Logic:** perform bit manipulation operations on non-numeric data stored in registers
    o **Shift:** perform shift operations on data stored in registers
- The basic arithmetic microoperations are addition, subtraction, increment, decrement, and shift
- Example of addition: R3 ← R1 +R2
- Subtraction is most often implemented through complementation and addition
- Example of subtraction: R3 ← R1 + $\overline{R2}$ + 1 (strikethrough denotes bar on top – 1's complement of R2)
- Adding 1 to the 1's complement produces the 2's complement
- Adding the contents of R1 to the 2's complement of R2 is equivalent to subtracting

Symbolic designation	Description
$F \leftarrow A + B$	Contents of A plus B transferred to F
$F \leftarrow A - B$	Contents of A minus B transferred to F
$B \leftarrow \overline{B}$	Complement register B (1's complement)
$B \leftarrow \overline{B} + 1$	Form the 2's complement of the contents of register B
$F \leftarrow A + \overline{B} + 1$	A plus the 2's complement of B transferred to F
$A \leftarrow A + 1$	Increment the contents of A by 1 (count up)
$A \leftarrow A - 1$	Decrement the contents of A by 1 (count down)

- Multiply and divide are not included as microoperations
- A microoperation is one that can be executed by one clock pulse
- Multiply (divide) is implemented by a sequence of add and shift microoperations (subtract and shift)

Logic Microoperations

- Logic operations specify binary operations for strings of bits stored in registers and treat each bit separately
- Example: the XOR of R1 and R2 is symbolized by

  P: R1 ← R1 ⊕ R2
- Example: R1 = 1010 and R2 = 1100

  1010 1010 Content of R1
  1100 1100 Content of R2
  0110 Content of R1 after P = 1

•Symbols used for logical microoperations:

OR: ∨

AND: ∧

XOR: ⊕

- The + sign has two different meanings: logical OR and summation
- When + is in a microoperation, then summation
- When + is in a control function, then OR
- Example:

  P + Q: R1 ← R2 + R3, R4 ← R5 ∨ R6
- There are 16 different logic operations that can be performed with two binary variables

PROCESSOR ORGANIZATION

- The processor part of a computer CPU is sometimes referred to as the *data path* of the CPU because the processor forms the paths for the data transfers between the registers in the unit.
- The various paths are said to be controlled by means of *gates* that open the required path and close all others.
- A processor unit can be designed to fulfill the requirements of a set of data paths for a specific application.
- In a processor unit, the data paths are formed by means of buses and other common lines.
- The control gates that formulate the given path are essentially multiplexers and decoders whose selection lines specify the required path.
- The processing of information is done by one common digital function whose data path can be specified with a set of common selection variables

Bus Organization

- A bus organization for four processor registers is shown in Fig.5.3.
- Each register is connected to two multiplexers (MUX) to form input buses A and *B.*
- The selection lines of each multiplexer select one register for the particular bus.
- The A and *B* buses are applied to a common arithmetic logic unit.
- The function selected in the ALU determines the particular operation that is to be performed.
- The shift microoperations are implemented in the shifter.
- The result of the microoperation goes through the output bus S into the inputs of all registers.
- The destination register that receives the information from the output bus is selected by a decoder.
- When enabled, this decoder activates one of the register load inputs to provide a transfer path between the data on the S bus and the inputs of the selected destination register. The output bus S provides the terminals for transferring data to an external destination. One input of multiplexer A or *B* can receive data from the outside

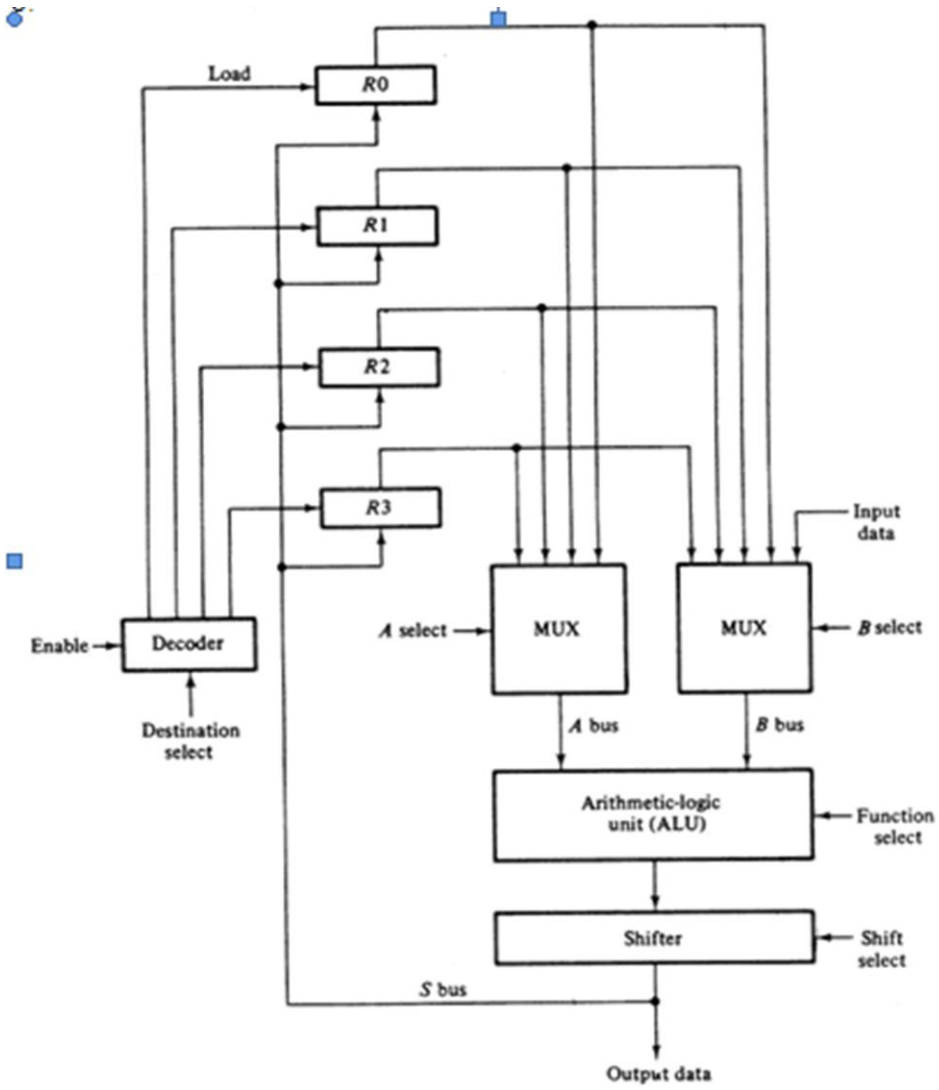


Fig 5.3 Processor registers and ALU connected through common buses

- The control unit that supervises the processor bus system directs the information flow through the ALU by selecting the various components in the unit. For example, to perform the microoperation:

$$R1 \leftarrow R2 + R3$$

- The control must provide binary selection variables to the following selector inputs:

1. M UX A selector: to place the contents of R *2* onto bus A.
2. MUX *B* selector: to place the contents of *R3* onto bus *B.*
3. ALU function selector: to provide the arithmetic operation A + *B.*
4. Shift selector: for direct transfer from the output of the ALU onto output bus S (no shift).

- Decoder destination selector: to transfer the contents of bus S into R 1.

ARITHMETIC LOGIC UNIT

An arithmetic logic unit (ALU) is a multi operation, combinational-logic digital function. It can perform a set of basic arithmetic operations and a set of logic operations: The ALU has a number of selection lines to select a particular operation in the unit. The selection lines are decoded within the ALU so that k selection variables can specify up to 2' distinct operations.

DESIGN OF ARITHMETIC CIRCUIT

- The basic component of the arithmetic section of an ALU is a parallel adder.
- A parallel adder is constructed with a number of full-adder circuits connected in cascade
- By controlling the data inputs to the parallel adder, it is possible to obtain different types of arithmetic operations.
- Figure 5.4 demonstrates the arithmetic operations obtained when one set of inputs to a parallel adder is controlled externally.
- The number of bits in the parallel adder may be of any value. The input carry C_{in} goes to the full-adder circuit in the least significant bit position. The output carry C_{out} comes from the full-adder circuit in the most significant bit position.

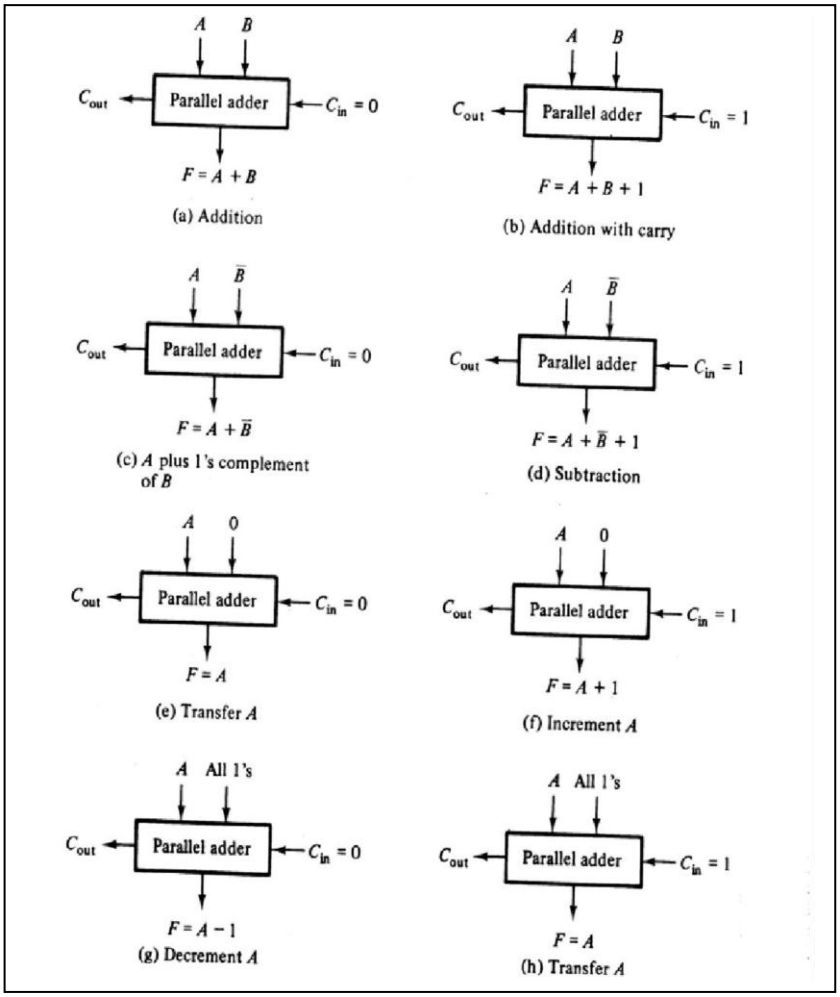


Fig 5.4 arithmetic operation

- From the above Fig 5.5, by changing the B input and C_{in} we get 8 operaton. So the input B is applied in four different form by using following circuit

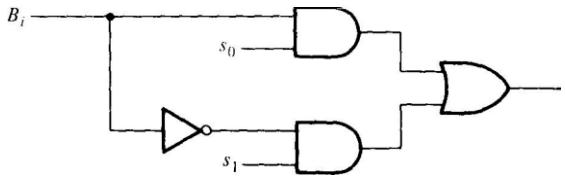


Fig 5.5

The input A is applied directly to the 4-bit parallel adder and the input B is modified. The resultant arithmetic circuit is shown in Fig 5.6

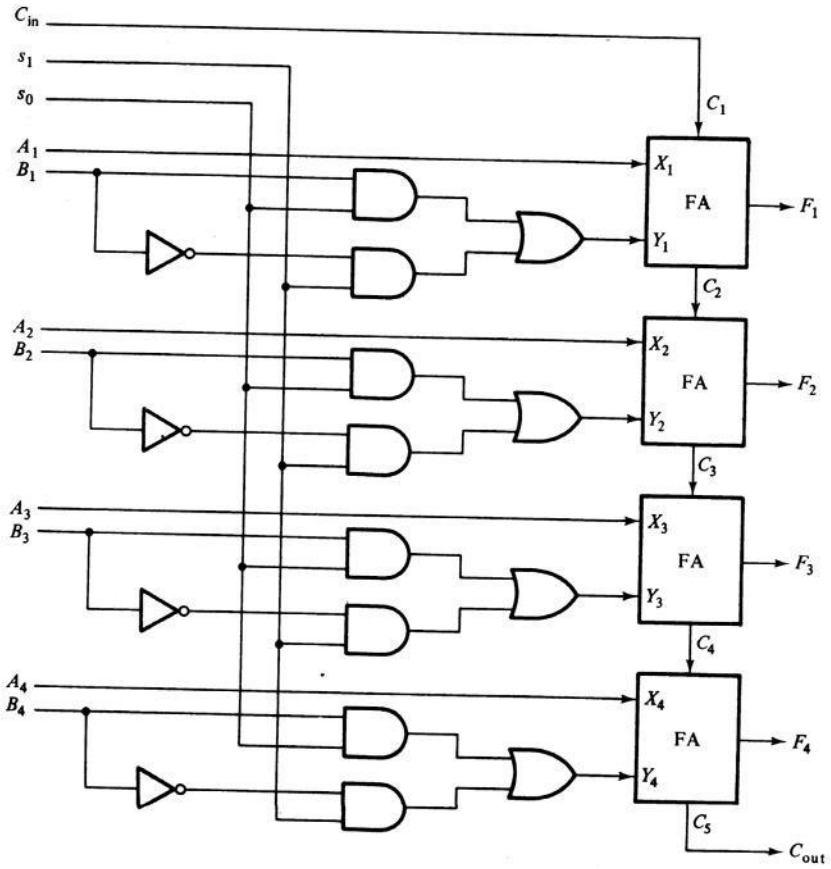
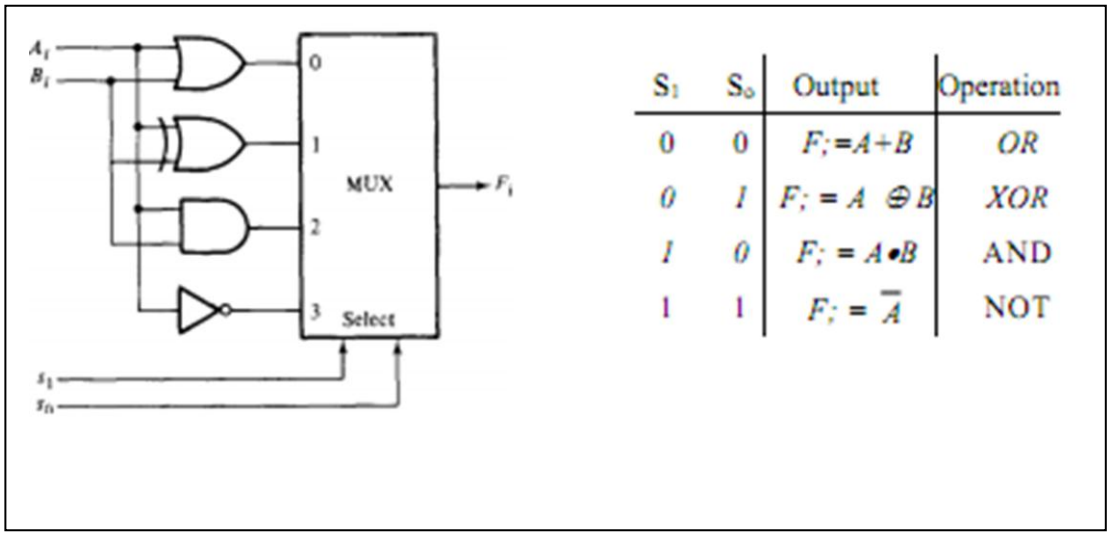


Fig 5.6 Arithmetic circuit

DESIGN OF LOGIC CIRCUIT

- The logic microoperations manipulate the bits of the operands separately and treat each bit as a binary variable.
- The 16 logic operations can be generated in one circuit and selected by means of four selection lines.
- Since all logic operations can be obtained by means of AND, OR, and NOT (complement) operations, it may be more convenient to employ a logic circuit with just these operations.
- For three operations, we need two selection variables.
- But two selection lines can select among four logic operations, so we choose also the exclusive-OR (XOR) function for the logic circuit to be designed in this and the next section.
- The simplest and most straightforward way to design a logic circuit is shown in Fig. 5.7. The diagram shows one typical stage designated by subscript i.
- The circuit must be repeated n times for an n-bit logic circuit. The four gates generate



S_1	S_0	Output	Operation
0	0	$F_i = A + B$	OR
0	1	$F_i = A \oplus B$	XOR
1	0	$F_i = A \bullet B$	AND
1	1	$F_i = \overline{A}$	NOT

Figure 5.7 one stage of logic circuit (a) Logic diagram (b) Function table

The four gate generate four logic operations OR, XOR, AND, and NOT. The two selection variables in the multiplexer select one of the gates for the output. The function table lists the output logic generated as a function of the two selection variables.

- The logic circuit can be combined with the arithmetic circuit to produce one arithmetic logic unit.
- Selection variables S_l and S_o can be made common to both sections provided we use a third selection variable, S_2, to differentiate between the two.
- This configuration is illustrated in Fig 5.7. The outputs of the logic and arithmetic circuits in each stage go through a multiplexer with selection variable S_2.

  When $S_2 = 0$, the arithmetic output is elected,
  when $s_2 = 1$, the logic output is selected.
- Although the two circuits can be combined in this manner, this is not the best way to design an ALU.

- A more efficient ALU can be obtained if we investigate the possibility of generating logic operations in an already available arithmetic circuit. This can be done by inhibiting all input carries into the full-adder circuits of the parallel adder. Consider the Boolean function that generates the output sum in a full-adder circuit:

$$F.=X \oplus Y \oplus C_{in}$$

- The input carry G in each stage can be made to be equal to 0 when a selection variable s_z is equal to 1. The result would be:

$$F=X \oplus Y$$

This expression is valid because of the property of the exclusive-OR operation $x \oplus 0 = x$

DESIGN OF ARITHMETIC LOGIC UNIT

Design steps

1. Design the arithmetic section independent of the logic section.
2. Determine the logic operations obtained from the arithmetic circuit in step 1, assuming that the input carries to all stages are 0.
3. Modify the arithmetic circuit to obtain the required logic operations.

The third step in the design is not a straightforward procedure and requires a certain amount of ingenuity on the part of the designer. There is no guarantee that a solution can be found or that the solution uses the minimum number of gates. The example presented here demonstrates the type of logical thinking sometimes required in the design of digital systems.

The final ALU is shown in Fig. 5.8 Only the first two stages are drawn, but the diagram can be easily extended to more stages. The inputs to each full-adder circuit are specified by the Boolean functions:

$$X_i = A_i + S_2\overline{S_1}S_0 B_i + S_2\overline{S_1}S_0 B_i$$
$$Y_i = S_0 B_i + \overline{S_1} B_i$$
$$Z_i = \overline{S_2} C_i$$

When $s_2 = 0$, the three functions reduce to:

$$X_i = A_i$$
$$Y_i = S_0 B_i + S_1 \overline{B_i}$$
$$Z_i = C$$

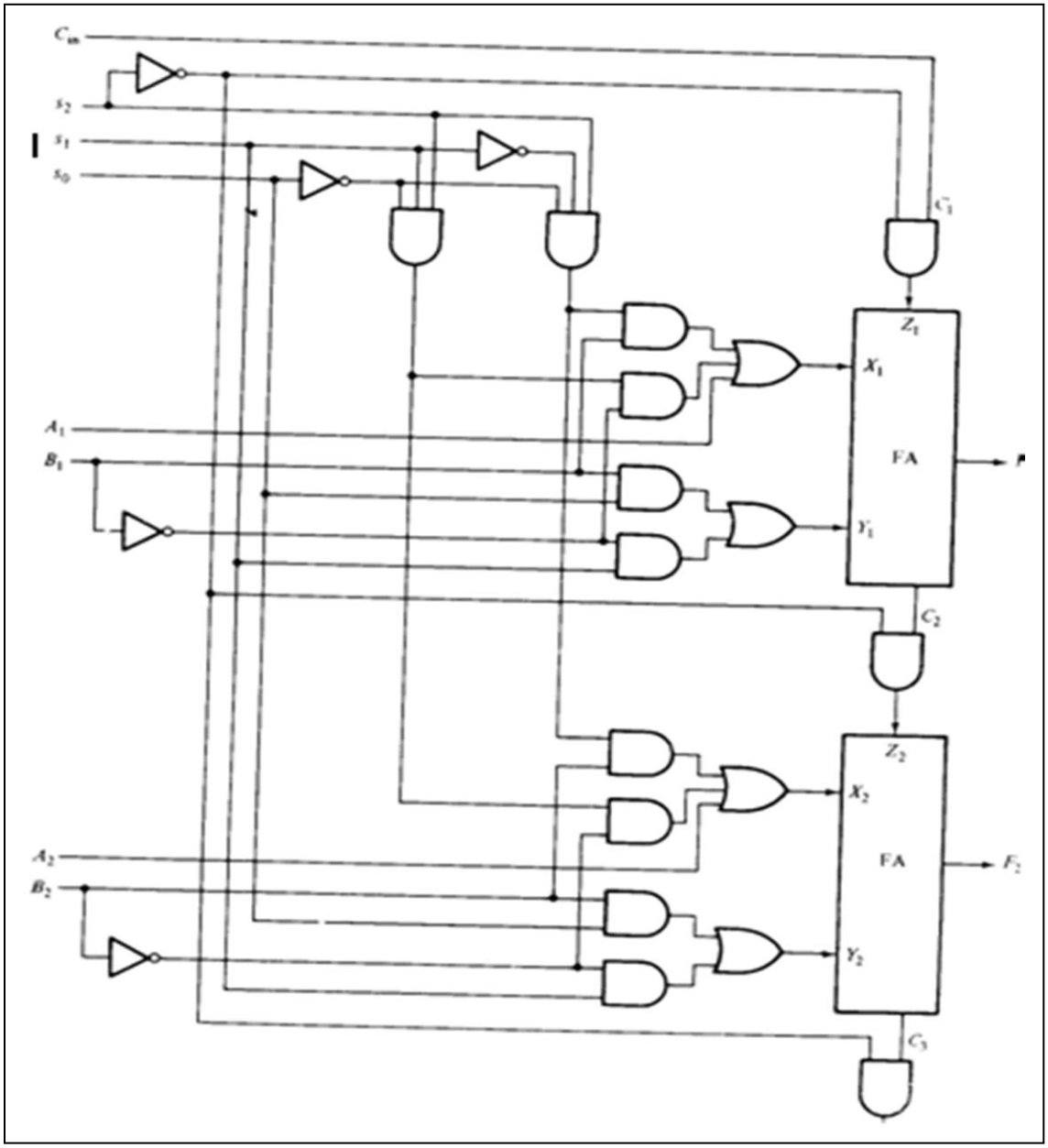


Figure 5.8 Logic diagram of arithmetic logic unit (ALU)

Fig 5.8 shows the two stage ALU logic circuit and the corresponding function table is shown in table 3

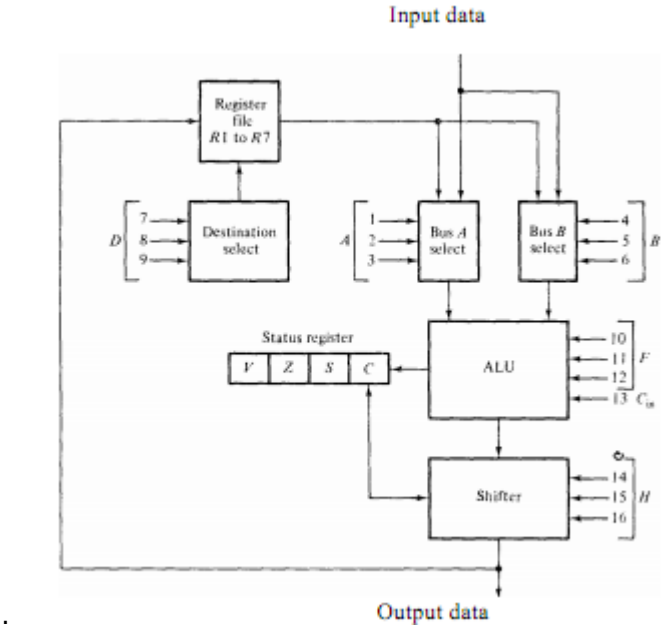
TABLE 5.3 Function table for the ALU of Fig. 5.8

Selection				Output	Function
S_2	S_1	S_0	Cin		
0	0	0	0	F = A	Transfer *A*
0	0	0	1	F = A + 1	Increment *A*
0	0	1	0	F = A + B	Addition
0	0	1	1	F = A + B + 1	Add with carry
0	1	0	0	F = A - B - 1	Subtract with borrow
0	1	0	1	F = A - B	Subtraction
0	1	1	0	F = A - 1	Decrement *A*
0	1	1	1	F = A	Transfer *A*
1	0	0	X	F = A V B	OR
1	0	1	X	F = A $\oplus$ B	XOR
1	1	0	X	F = A $\wedge$ B	AND
1	1	1	X	F = $\overline{A}$	Complement *A*

PROCESSOR UNIT

- A block diagram of a processor unit is shown in Fig. 5.9(a).It consists of seven registers R 1 through R 7 and a status register.
- The outputs of the seven registers go through two multiplexers to select the inputs to the ALU.
- Input data from an external source are also selected by the same multiplexers. The output of the ALU goes through a shifter and then to a set of external output terminals.

- The output from the shifter can be transferred to any one of the registers or to an external destination.
- There are 16 selection variables in the unit, and their function is specified by a control word in Fig. 5.9 (b). The 16-bit control word, when applied to the selection variables in the processor, specifies a given microoperation.
- The control word is partitioned into six fields, with each field designated by a letter name. All fields, except Cin, have a code of three bits.
- Three bits of A select source register for the input to left side of the ALU. The B field is the same, but it selects the source information for the right input of the ALU.
- The D field selects a destination register.
- The F field, together with the bit in C_{in}, selects a function for the ALU. The H field selects the type of shift in the shifter unit



(a) Block diagram

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
A			B			D			F			C_{in}	H		

(b) Control word

Figure 5.9 Processor unit with control variables

- The functions of all selection variables are specified in Table 4.
- The 3-bit binary code listed in the table specifies the code for each of the five fields A, B, D, input data, F, and H.
- The register selected by A, B, and D is the one whose decimal number is equivalent to the binary number in the code.
- When the A or B field is 000, the corresponding multiplexer selects the input data. When D = 000, no destination register is selected.

- The three bits in the F field, together with the input carry C_{in}, provide the 12 operations of the ALU as specified in Table 4.4. Note that there are two possibilities for F = A. In one case the carry bit C is cleared, and in the other case it is set to 1

TABLE 5.4 Functions of control variables for the processor of Fig. 5.9

Binary code	Function of selection variables					
	A	B	D	F with $C_{in}=0$	F with $C_{in}=1$	H
000	Input data	Input data	None	A, C ← 0	A + 1	No shift
001	R1	R1	R1	A + B	A + B + 1	Shift-right, $I_R = 0$
010	R2	R2	R2	A - B - 1	A - B	Shift-left, $I_L = 0$
011	R3	R3	R3	A - 1	A, C ← 1	0's to output bus
100	R4	R4	R4	A V B	-	-
101	R5	R5	R5	$A \oplus B$	-	Circulate-right with C
110	R6	R6	R6	$A \wedge B$	-	Circulate-left with C
111	R7	R7	R7	$\overline{A}$	-	-

DESIGN OF ACCUMULATOR

- Some processor units distinguish one register from all others and call it an accumulator register.
- The block diagram of an accumulator that forms a sequential circuit is shown in Fig 5.10.
- The A register and the associated combinational circuit constitutes a sequential circuit.
- The combinational circuit replaces the ALU but cannot be separated from the register, since it is only the combinational-circuit part of a sequential circuit.
- The A register is referred to as the accumulator register and is sometimes denoted by the symbol AC. Here, accumulator refers to both the A register and its associated combinational circuit.
- The external inputs to the accumulator are the data inputs from B and the control variables that determine the micro operations for the register.
- The next state of register A is a function of its present state and of the external inputs.

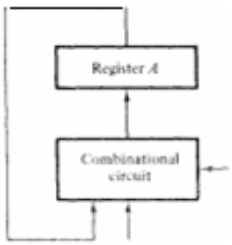


Figure 5.10 Block diagram of accumulator

- The accumulator is similar to these registers but is more general, since it can perform data-processing operations.
- An accumulator is a multifunction register that, by itself, can be made to perform all of the microoperations in a processor unit. The microoperations included in an accumulator depend on the operations that must be included in the particular processor.

- Table 5.5 shows the list of microoperation for an accumulator

Control variable	Microoperation	Name
Pi	A ←A + B	Add
Pz	A ← 0	Clear
P 3	A ← $\overline{A}$	Complement
Pa	A ←A ∧ B	AND
Ps	A ←A ∨ B	OR
P6	A ←A ⊕B	Exclusive-OR
P7	A ← shr A	Shift-right
Pa	A ←shl A	Shift-left
P9	A ← A + I	Increment
	I f (A = 0) then (Z = 1)	Check for zero

Control unit organization

- The digital system is divided into two parts one is data processing part and control logic.
- The relationship between the control and the data processor in a digital system is shown in Fig.5.11
- The data processor part may be a general-purpose processor unit, or it may consist of individual registers and associated digital functions.
- The control initiates all microoperations in the data processor. The control logic that

generates the signals for sequencing the microoperations is a sequential circuit whose internal states dictate the control functions for the system.

- The digital circuit that acts as the control logic provides a time sequence of signals for initiating the microoperations in the data-processor part of the system.

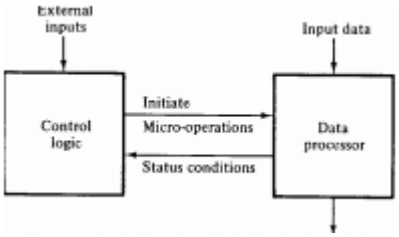


Fig 5.11 Control and data-processor interaction

Types of control unit

1. Hardwired control unit: A control unit implemented with SSI and MSI devices is said to be a hard-wired control.
2. Microprogrammed or microprocessor control unit : microprogram control which uses an LSI device such as a programmable logic array or a read-only memory

Comparison between hardwired and microprogrammed control unit

Sl.No.	Hardwired control unit	Microprogrammed control unit
1	Implemented using SSI and LSI devices	Implemented using LSI such as programmable devices
2	Speed is high	Speed is low as compare to hardwired control
3	If any alterations or modifications are needed, the circuits must be rewired to fulfill the new requirements	No need to rewiring, just modify the contents of memory

Four methods of control organization

1. One flip-flop per state method.
2. Sequence register and decoder method.
3. PLA control.
4. Microprogram control

One Flip-Flop per State Method

- This method uses one flip-flop per state in the control sequential circuit.
- Only one flip-flop is set at any particular time; all others are cleared.
- A single bit is made to propagate from one flip-flop to the other under the control of decision logic.
- In such an array, each flip-flop represents a state and is activated only when the control bit is transferred to it.
- It uses a maximum number of flip-flops. For example, a sequential circuit with 12 states requires a minimum of four flip-flops because $2^3 < 12 < 2^4$. Yet by this method, the control circuit uses 12 flip-flops, one for each state.

- Fig 5. 12 shows the block diagram of one flip-flop per state method

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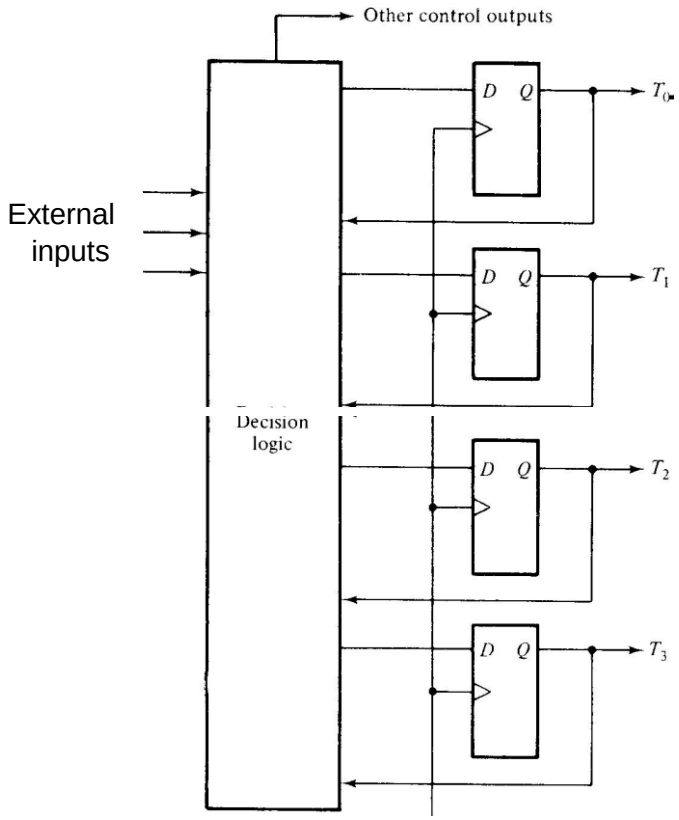

Fig 5.12 Control logic with one flip-flop per state

- In this figure 5.12 has four flip-flop per state T_i, i = 0, 1, 2, 3.at any given time interval between two clock pulses, only one flip-flop is equal to 1; all others are equal to 0.
- The transition from the present state to the next is a function of the present T_i that is a 1 and certain input conditions.
- The next state is manifested when the previous flip-flop is cleared and a new one is set. Each of the flip-flop outputs is connected to the data-processing section of the digital system to initiate certain microoperations.
- The other control outputs shown in the diagram are a function of the T's and external inputs. These outputs may also initiate microoperations.

The **advantage** of the one flip-flop per state method is the simplicity with which it can be designed. This type of controller can be designed by inspection from the state diagram that describes the control sequence

Sequence Register and Decoder Method

This method uses a register to sequence the control states. The register is decoded to provide one output for each state. For *n* flip-flops in the sequence register, the circuit will have 2^n states and the decoder will have 2^n outputs.

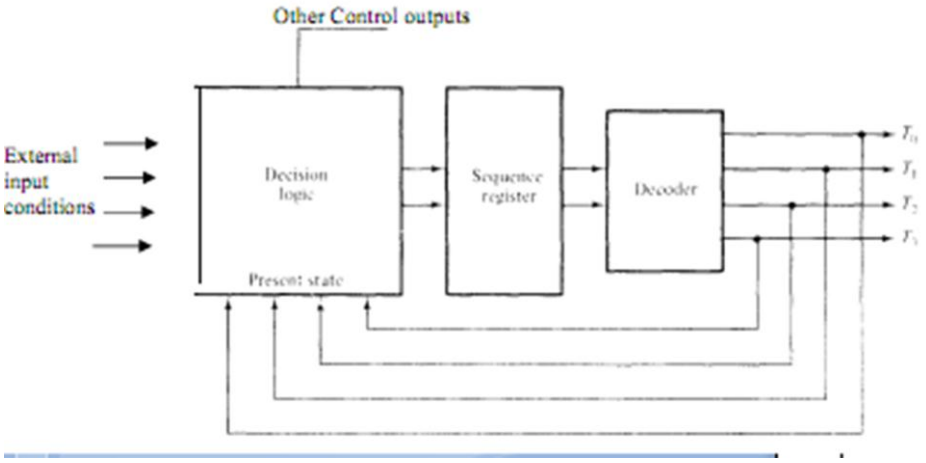

Figure 5.13 Control logic with sequence register and decoder

- Figure 5.13 shows the configuration of a four-state sequential control logic.
- The sequence register has two flip-flops and the decoder establishes separate outputs for each state in the register.
- The transition to the next state in the sequence register is a function of the present state and the external input conditions.
- Since the outputs of the decoder are available anyway, it is convenient to use them as present-state variables rather than use the direct flip-flop outputs.
- Other outputs which are a function of the present state and external inputs may initiate microoperations in addition to the decoder outputs.

PLA Control

The PLA control is essentially similar to the sequence register and decoder method except that all combinational circuits are implemented with a PLA, including the decoder and the decision logic. By using a PLA for the combinational circuit, it is possible to reduce the number of ICs and the number of interconnection wires.

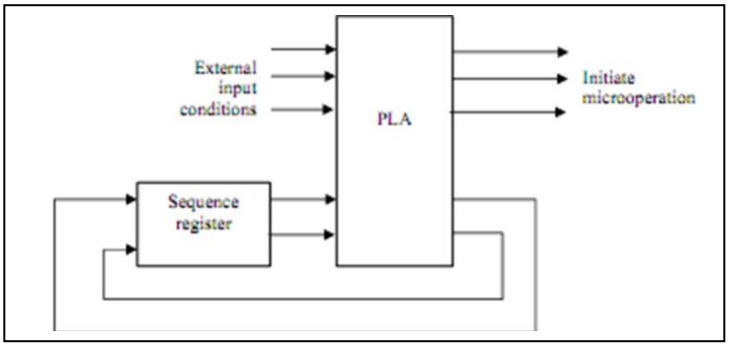

Fig 5.14 PLA control logic

- Figure 5.14 shows the configuration of a PLA controller. An external sequence register establishes the present state of the control circuit.

- The PLA outputs determine which microoperations should be initiated, depending on ex-ternal input conditions and the present state of the sequence register.
- At the same time, other PLA outputs determine the next state of the sequence register.
- The sequence register is external to the PLA if the unit implements only combinational circuits. However, some PLAs are available which include not only gates, but also flip-flops within the unit. This type of PLA can implement a sequential circuit by specifying the links that must be connected to the flip-flops in the same manner that the gate links are specified.

Microprogram Control

- The purpose of the control unit is to initiate a series of sequential steps of microoperations.
- The control variables at any given time can be represented by a string of 1's and 0's called a *control word.* As such, control words can be programmed to initiate the various components in the system in an organized manner.
- A control unit whose control variables are stored in a memory is called a microprogrammed control unit. Each control word of memory is called a *microinstruction,* and a sequence of microinstructions is called a *microprogram.*
- Figure 5.15 illustrates the general configuration of the microprogram control unit.
- The control memory is assumed to be a ROM, within which all control information is permanently stored.
- The control memory address register specifies the control word read from control memory. It must be realized that a ROM operates as a combinational circuit, with the address value as the input and the corresponding word as the output.
- The content of the specified word remains on the output wires as long as the address value remains in the address register. No read signal is needed as in a random-access memory.
- The word read from control memory represents a microinstruction. The microinstruction specifies one or more microoperations for the components of the system.

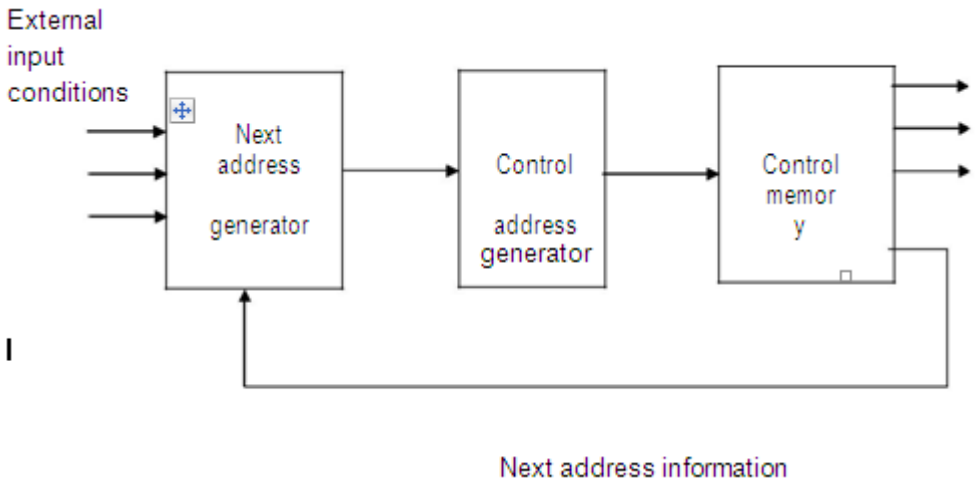

Figure 5.15 Microprogram control logic

- Once these operations are executed, the control unit must determine its next address. The location of the next microinstruction may be the next one in sequence, or it may be located somewhere else in the control memory. For this reason, it is necessary to use some bits of the microinstruction to control the generation of the address for the next microinstruction. The next address may also be a function of external input conditions.
- While the microoperations are being executed, the next address is computed in the next-address generator circuit and then transferred (with the next clock pulse) into the control address register to read the next microinstruction.