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1

Integrated Circuit Fabrication

1.1 INTRODUCTION

We are going through a period of micro-electronic revolution. For a common person, the role of electronics is limited to audio-visual gadgets like radio and television, but the truth is, today the growth of any industry like communication, control, instrumentation or computer, is dependent upon electronics to a great extent. And integrated circuits are electronics.

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions. In this chapter, we describe the basic processes used in the fabrication of integrated circuits. Both bipolar and MOS fabrication are treated. These circuits naturally offer a number of distinct advantages over those made by interconnecting discrete components. These may be listed as follows:

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)
5. Matched devices
6. Increased operating speeds (due to the absence of parasitic capacitance effect)
7. Reduction in power consumption.

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1.8.3 Complementary MOSFET (CMOS) Fabrication

It is possible to fabricate NMOS and PMOS enhancement devices on the same silicon chip. These devices are called complementary MOSFETs (abbreviated as CMOS, COS/MOS). The CMOS circuit of Fig. 1.29 (a) when implemented with polysilicon gate FETs has the cross-sectional view as shown in Fig. 1.29 (b). An n-type 'well' or 'tub' is diffused in the p-type substrate. The PMOS transistor (Q_2) is fabricated within this well. The n-type region forms the substrate or body B_2 for the the PMOS transistor. There are two additional steps required in the fabrication of PMOS transistor (Q_2) compared to NMOS transistor (Q_1), such as, the formation of n-region and ion implantation of p-type source and drain regions. The rest of the processes are the same as discussed for NMOS fabrication.

It can be seen that B_1 is tied to S_1 and is connected to the lowest voltage (GND) whereas B_2 is tied to S_2 and held at supply voltage V_{DD}. Since B_1 is p-type and B_2 is n-type, both the source substrate diodes (B_1-S_1 and B_2-S_2) are reverse biased and thus cut off. Thus isolation between NMOS and PMOS transistor is automatically achieved.

The circuit of Fig. 1.29 (a) is a CMOS inverter where G_1 is tied to G_2 and D_1 is connected to D_2. However, we have not shown these connections in the cross-sectional view of Fig. 1.29 (b).

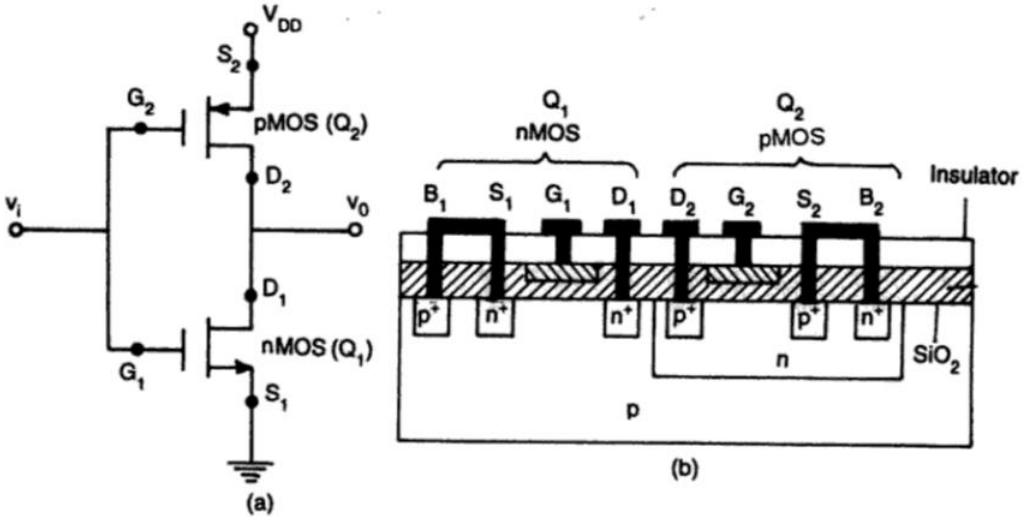

Fig. 1.29 (a) CMOS inverter, (b) Cross-section of CMOS IC

1.9 THIN AND THICK FILM TECHNOLOGY

Film ICs are classified as thick film and thin film circuits. Film technology at present can produce only passive components. The use of the term 'Thin Film' has been made in this chapter often, wherever

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After this, the entire wafer is covered with a protective isolating layer usually of SiO_2. The contact areas (including the body) are next defined using photolithographic process. Finally aluminium is evaporated over the entire wafer and another mark is used to pattern the circuit connections. The final cross-section is shown in Fig. 1.28 (d).

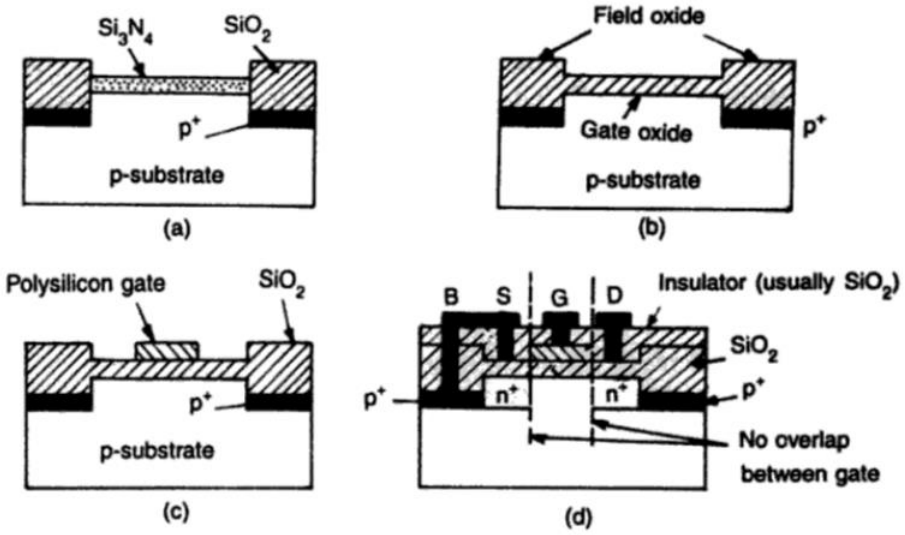

Fig. 1.28 Fabrication of polysilicon gate enhancement NMOS (a) Thick oxide growth and p^+ implantation, (b) Selective etching of Si_3N_4 and thin oxide growth, (c) Deposition of polysilicon gate, (d) Final cross-sectional view showing metallization and interconnection between substrate and source

There are two important points to be noticed in this structure.

1. The polysilicon-gate provides self alignment of the gate with the source and drain. In a conventional metal gate structure of Fig. 1.27, the gate electrode is normally designed to overlap the edges of the source and drain region by about 5 μm to avoid any masking errors. This, however, results in small overlap capacitance C_{gs} between gate G and source S and C_{gd} between gate G and drain D. These capacitances are of the order of 1 to 3 pF and lower the speed of operation and increase the power consumption. The silicon gate due to self aligning property eliminates these capacitances.
2. Another advantage of this structure is that no isolation island is required. This is because drain terminal in an NMOS device is held positive with respect to the source which is tied to the substrate. This cuts off the drain to substrate diode and the source to substrate diode formed due to p^+ region and the current flows only along the channel between D and S. In BJT the isolation diffusion occupies an extremely large percentage of chip area. With MOSFET, it is possible to get a packaging density twenty times more than that of BJT IC.

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Use of Silicon Nitride (Si_3N_4)

It has been found that Si_3N_4 has superior masking properties compared to SiO_2. The Si_3N_4 is sandwiched between two SiO_2 layers and provides the necessary barrier to prevent impurities penetrating through the SiO_2 layer. The dielectric constant of Si_3N_4 is 7.5 whereas that of SiO_2 is 4. This increased overall dielectric constant reduces V_T.

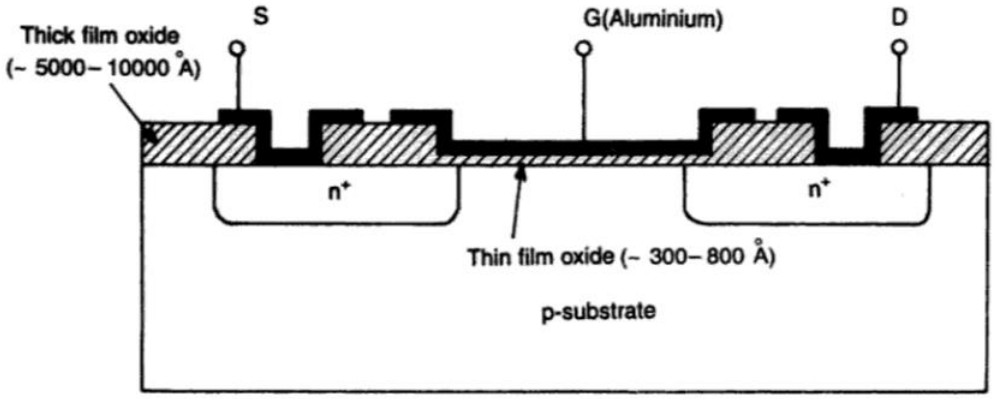

Fig. 1.27 n-channel MOSFET

Polysilicon Gate

Polycrystalline silicon when doped with phosphorus is conductive and is used as the gate electrode instead of aluminium. This reduces V_T to about 1 to 2V. Such devices are called silicon gate MOS transistors. The fabrication of NMOS enhancement device using these improved techniques is shown in Fig. 1.28.

The Si_3N_4 is first coated on the entire surface of a p-type wafer. With the help of a mask, sufficient area is defined to include the source, gate and drain. The Si_3N_4 is next etched away from the surface outside the transistor region. Now p^+ impurities are ion-implanted in the exposed p-substrate. These p^+ regions serve to isolate the various devices. Next a thick SiO_2 layer called field oxide is grown over the p^+ regions. The Si_3N_4 region, however, remains unaffected by the oxidation. The structure now is as shown in Fig. 1.28 (a).

The Si_3N_4 is now removed by selective etching and then SiO_2 layer (800 to 1000Å) is thermally grown over the transistor area as shown in Fig. 1.28 (b).

Polycrystalline silicon commonly known as polysilicon is now deposited over the entire wafer. The polysilicon gate is now formed by selective removal of polysilicon as shown in Fig. 1.28 (c).

The n^+ source and drain regions are formed by ion implantation. The field oxide and the polysilicon gate prevent the penetration of dopants below these regions. The thin oxide layer, however, allows the penetration of dopants and thus drain and source regions are formed.

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1.8 FABRICATION OF FET

Unipolar monolithic ICs use JFET or MOSFET as an active device. The fabrication technique of JFET, MOSFET and CMOS is discussed.

1.8.1 JFET Fabrication

The structure of an *n*-channel JFET is shown in Fig. 1.26. The basic processes used are the same as in BJT fabrication. The epitaxial layer which formed the collector of the BJT is used as the *n*-channel of the JFET. The p^+ gate is formed in the n-channel by the process of diffusion or ion-implantation. The n^+ regions have been formed under the drain and source contact regions to provide good ohmic contact.

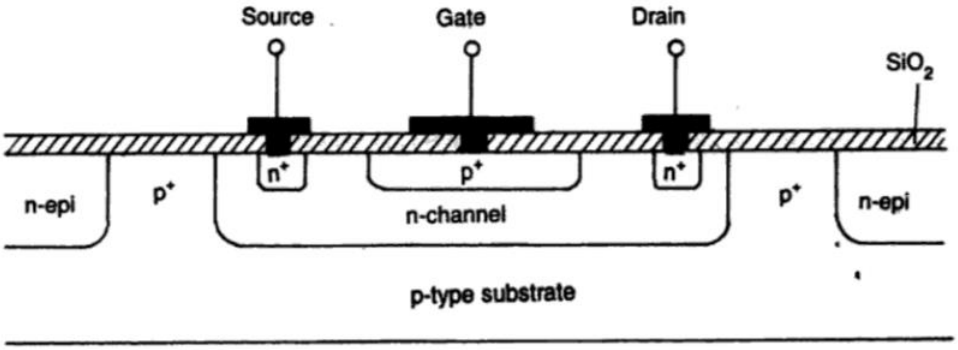

Fig. 1.26 *n*-channel JFET structure

1.8.2 MOSFET Fabrication

Two types of MOSFET devices are available, such as, enhancement type and depletion type. The cross-sectional view of *n*-channel aluminium gate enhancement MOSFET is shown in Fig. 1.27. In this structure, the metallic gate G is separated from the semiconductor channel by the insulating SiO_2 layer. The insulating layer of silicon dioxide gives an extremely high input resistance (10^{10} to 10^{15} Ω) for the MOSFET.

The value of V_T, the threshold voltage for MOSFET fabricated by this technique is typically 3 to 6V and power supply voltage of 12V is used for the drain supply. This large voltage is not compatible with the 5V supply used in digital ICs. A number of techniques have been developed to lower the magnitude of V_T which leads to improved device performance.

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which is less than the cut-in voltage for Si-base to collector junction ($\simeq$ 0.5 V), so that the transistor does not enter into saturation.

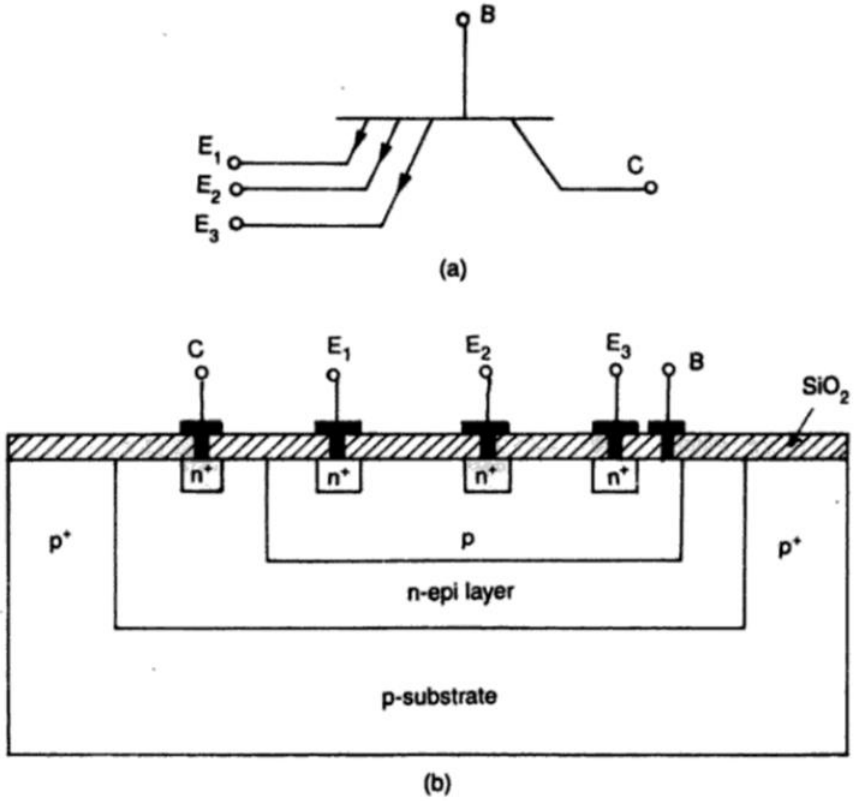

Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Figure 1.19 (b, c) shows the cross-sectional view of a Schottky transistor, and its symbol. A Schottky diode is formed between base and collector by allowing Al-metallization for the base lead to make contact with the n-type collector region. This is discussed in detail in Sec. 1.7.2.

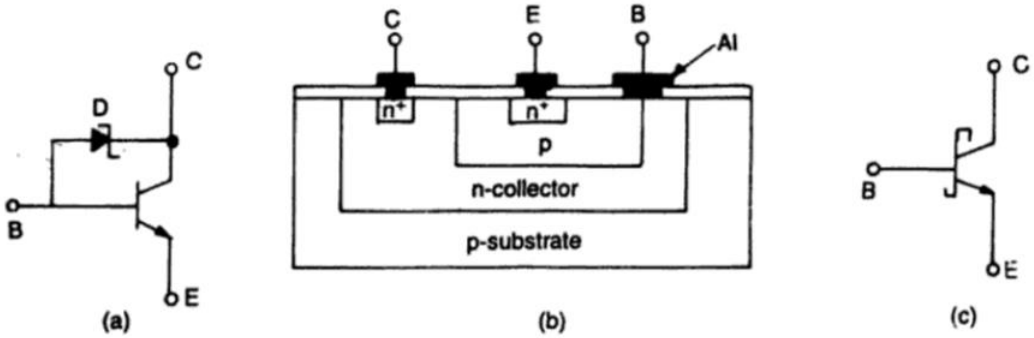

Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

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Triple Diffused pnp Transistor

If to a standard *npn* transistor, an extra *p*-type diffusion is added after the *n*-diffusion, it is quite possible to obtain a *pnp* transistor and is known as triple diffused *pnp* transistor. However the usefulness of such a structure is limited due to additional fabrication steps required and serious design considerations.

Comparison of npn and pnp IC Transistors

In general, *npn* transistors are preferred in integrated circuits compared to *pnp* transistors due to a variety of reasons.

1. A vertical *pnp* transistor has the disadvantage that its collector has to be held at a fixed negative voltage.
2. Lateral *pnp* transistor has inferior characteristic as the base width is usually larger controlled by lateral diffusion of p-type impurities and photographic limitations during mask making and alignment. Therefore, *pnp* transistor normally gives current gain as low as 1.5 to 30 compared to 50 to 300 for the *npn* transistor. With improved technology, however, it has now been possible to increase the gain to 100.
3. We know that collector region is heated during base and emitter diffusions, so the diffusion coefficient of the collector impurities should be as small as possible to avoid the movement of the collector junction. Since *n*-type impurities have smaller diffusion constant than *p*-type impurities, the *n*-type collector moves very little while *p*-type moves appreciably. This makes the *npn* transistor superior in performance with relatively easier process control.

Multi-emitter Transistor

In many applications such as transistor-transistor logic (TTL), we need multiemitter transistor of the type shown in Fig. 1.18 (a). The cross-sectional view of such a transistor is shown in Fig. 1.18 (b) where n^+ emitter is diffused at three places in the *p*-type base. Thus it is possible to save chip area and enhance component density of an IC.

The Schottky Transistor

In digital circuits, many times it is desired that the switching should be very fast. This can be achieved if the transistor is prevented from entering into saturation. Figure 1.19 (a) shows such an arrangement where a Schottky diode (Sec. 1.7.2) is used as a clamp between the base and collector.

If base current is increased to saturate the transistor, the voltage at the collector drops thereby making diode D conduct. As soon as diode D conducts, the base to collector voltage drops to about 0.4 V

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pnp Transistor

pnp transistors in integrated circuits are fabricated in one of the following three ways:

Vertical or substrate *pnp*
Lateral *pnp*
Triple diffused *pnp*

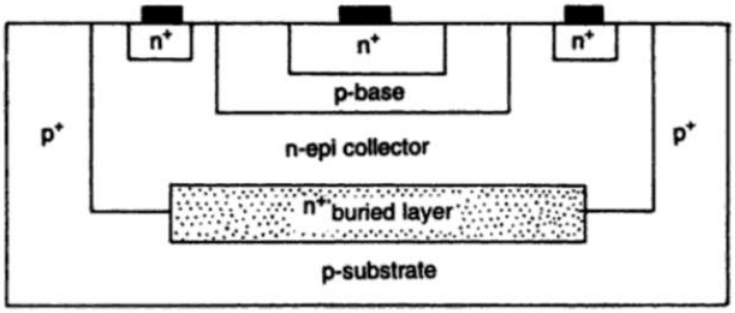

Fig. 1.16 Use of "buried n^+ layer" to reduce collector series resistance

Vertical *pnp* Transistor

The *p*-type substrate itself is used as *p*-collector, *n*-epitaxial layer for the base and the next *p*-diffusion (base in *npn* structure) as the emitter region. This type of *pnp* transistor has the limitation that collector has to be held at a fixed negative potential, as substrate is to be held at the most negative potential in the circuit for providing good isolation.

Lateral *pnp*-Transistor

This is the most common form of an integrated *pnp* transistor which can be fabricated simultaneously with the *npn* transistor and requires no additional masking or diffusion step. The *n*-type epi layer is used as the base of the *pnp* transistor. During the *p*-type base diffusion for the *npn* transistor, two adjacent *p*-regions are diffused to form emitter and collector regions of the lateral *pnp* transistor as shown in Fig. 1.17.

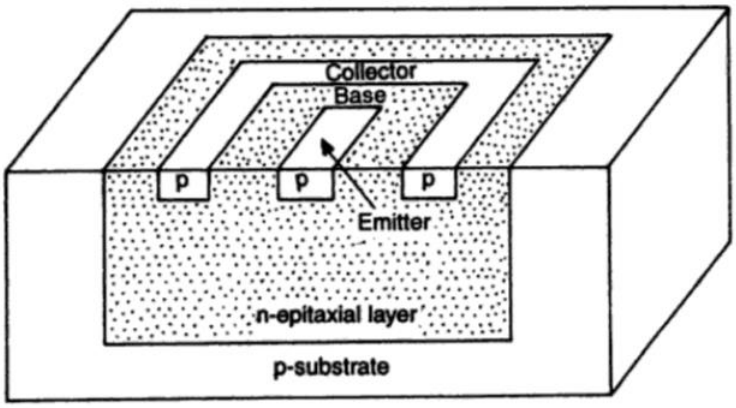

Fig. 1.17 A *pnp* lateral transistor

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difference makes an integrated transistor poorer than discrete transistor in two ways:

(i) Collector contact being at the top increases the collector current path, thereby increasing the collector series resistance and hence $V_{CE\ (sat)}$ of the device.

(ii) In the integrated transistor, additional parasitic capacitance appears between collector and substrate is held at negative potential. However, these shortcomings of the integrated transistors can be overlooked on account of a number of advantages inherent in integrated technology. In this, circuit performance is highly improved as matched transistors can be obtained for example to be used in difference amplifiers. Integrated transistors spaced within 30 mils can have V_{BE} matching better than 5 mV and h_{FE} match of ± 10 percent.

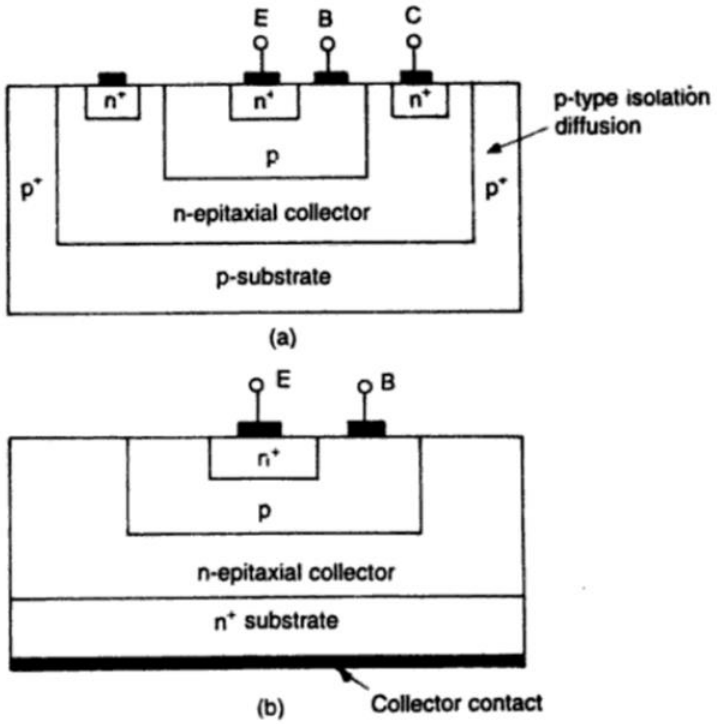

Fig. 1.15 Cross-section of (a) Monolithic integrated circuit transistor, (b) a discrete planar epitaxial transistor

Use of 'Buried n^+ Layer' to reduce Collector Series Resistance

The higher collector series resistance of an integrated transistor can be easily reduced by a process known as 'buried layer' shown in Fig. 1.16. In this, a heavily doped n^+ region is sandwiched between the n-type epitaxial collector and p-type substrate. This buried n^+ region provides a low resistivity current path from the active collector region (n-type layer) to the collector contact (n^+ contact layer). In effect, the n^+ layer shunts the n-layer of the collector region with respect to the flow of the current thus effectively reducing the collector resistance.

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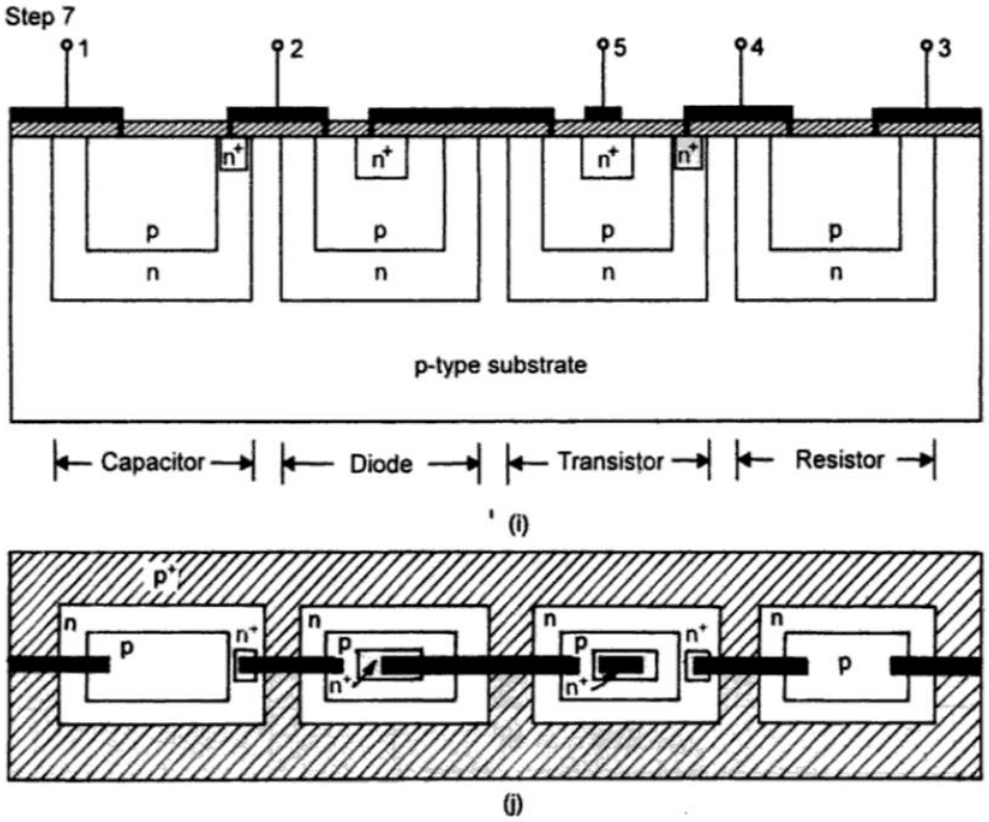

Fig. 1.14 (i, j)

1.7 ACTIVE AND PASSIVE COMPONENTS OF ICs

Now the reader is familiar with the basic technology involved in the fabrication of ICs. More light will be thrown on the various devices which constitute a monolithic circuit. These include:

1. Transistors
2. Diodes
3. Resistors
4. Capacitors
5. Inductors.

1.7.1 Monolithic Transistors

Figure 1.15 (a) shows the cross-sectional view of an IC transistor. Let us compare it with the conventional discrete transistor also fabricated using planar technology and shown in Fig. 1.15 (b).

The most striking feature in the two structures is that in the IC transistor, collector contact is on the top whereas in the discrete transistor it is at the bottom. In IC transistor, collector contact has to be taken from the top because collector is isolated from the substrate and the next isolation island by reverse-biased diodes. This structural

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Aluminium, normally used for making interconnections, is a *p*-type impurity in silicon, and can produce an unwanted rectifying contact with the lightly doped *n*-material. However, heavy concentration of phosphorous (~ 2×10^{20} cm^{-3}) doping causes a high degree of damage to the Si-lattice at the surface, thus effectively making it semi-metallic. This n^+ layer thus makes a good ohmic contact with the Al-layer. The top view corresponding to Fig. 1.14 (g) is shown in Fig. 1.14 (h).

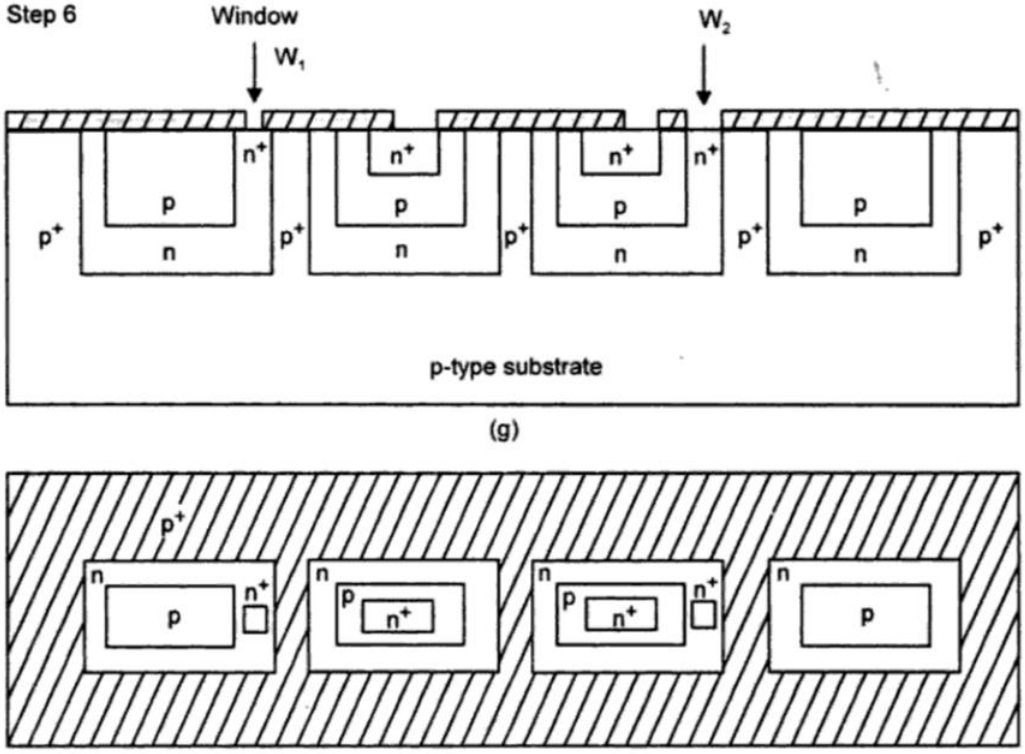

Fig. 1.14 (g-h)

Step 7: Aluminium Metallization

Now the IC chip is complete with all the active and passive devices and only interconnections between the various components have to be made in accordance with the circuit in Fig. 1.3. The chip is further subjected to the process of the formation of a new SiO_2 layer and masked etching to open a new set of windows at the points where contacts have to be made.

Now, a thin even coating of aluminium is vacuum-deposited over the entire surface of the wafer. The interconnection pattern between the components is then formed by photo resist techniques. The undesired aluminium areas are etched away leaving a pattern of interconnections between transistor, resistor, diode and capacitor as shown by the cross-sectional and top view in Fig. 1.14 (i) and Fig. 1.14 (j) respectively.

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The concentration of acceptor atoms ($N_A \simeq 5 \times 10^{20}$ cm^{-3}) in the region between isolation islands is generally kept higher than p-type substrate for which $N_A = 1.4 \times 10^{15}$ atoms/cm^3. This ensures that the depletion region of the reverse biased diode will not extend into p^+ region to the extent of electrically connecting the two isolation islands. There will, however, be a significant amount of barrier or transition capacitance present as a by product of the isolation diffusion. The top view of the isolation islands is depicted in Fig. 1.14 (e).

Step 5: Base Diffusion

Refer to Fig. 1.14 (f). A new layer of SiO_2 is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique. Now, p-type impurities, such as boron, are diffused through the openings into the islands of n-type epitaxial silicon. The depth of this diffusion must be controlled so that it does not penetrate through n-layer into the substrate. This diffusion is utilized to form base region, of the transistor, resistor, the anode of the diode and junction capacitor.

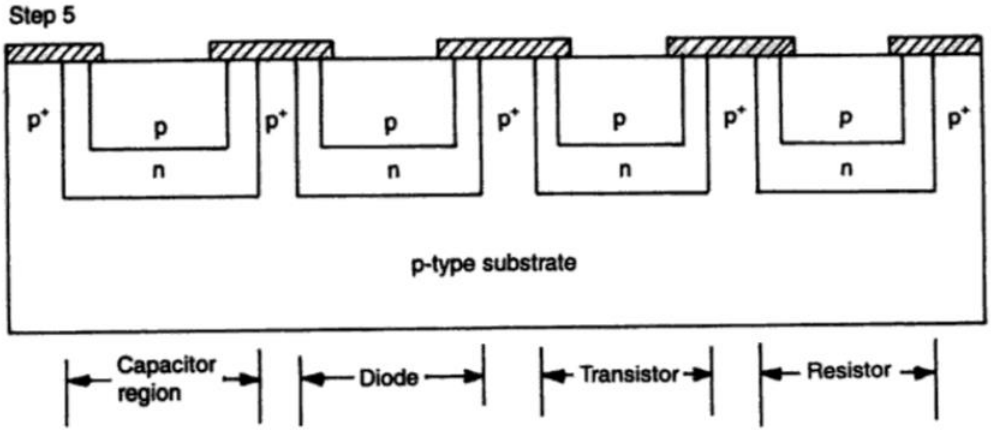

Fig. 1.14 (f)

Step 6: Emitter Diffusion

Refer to Fig. 1.14 (g). A new layer of SiO_2 is again grown over the entire wafer and selectively etched to open a new set of windows and n-type impurity (phosphorus) is diffused through them. This forms transistor emitter and cathode region of diode.

Windows (W_1, W_2 etc.) are also etched into n-region where contact is to be made to the n-type layer. Heavy concentration of phosphorus (n^+) is diffused into these regions simultaneously with the emitter diffusion. The reason for using heavily doped n-regions can be explained as follows:

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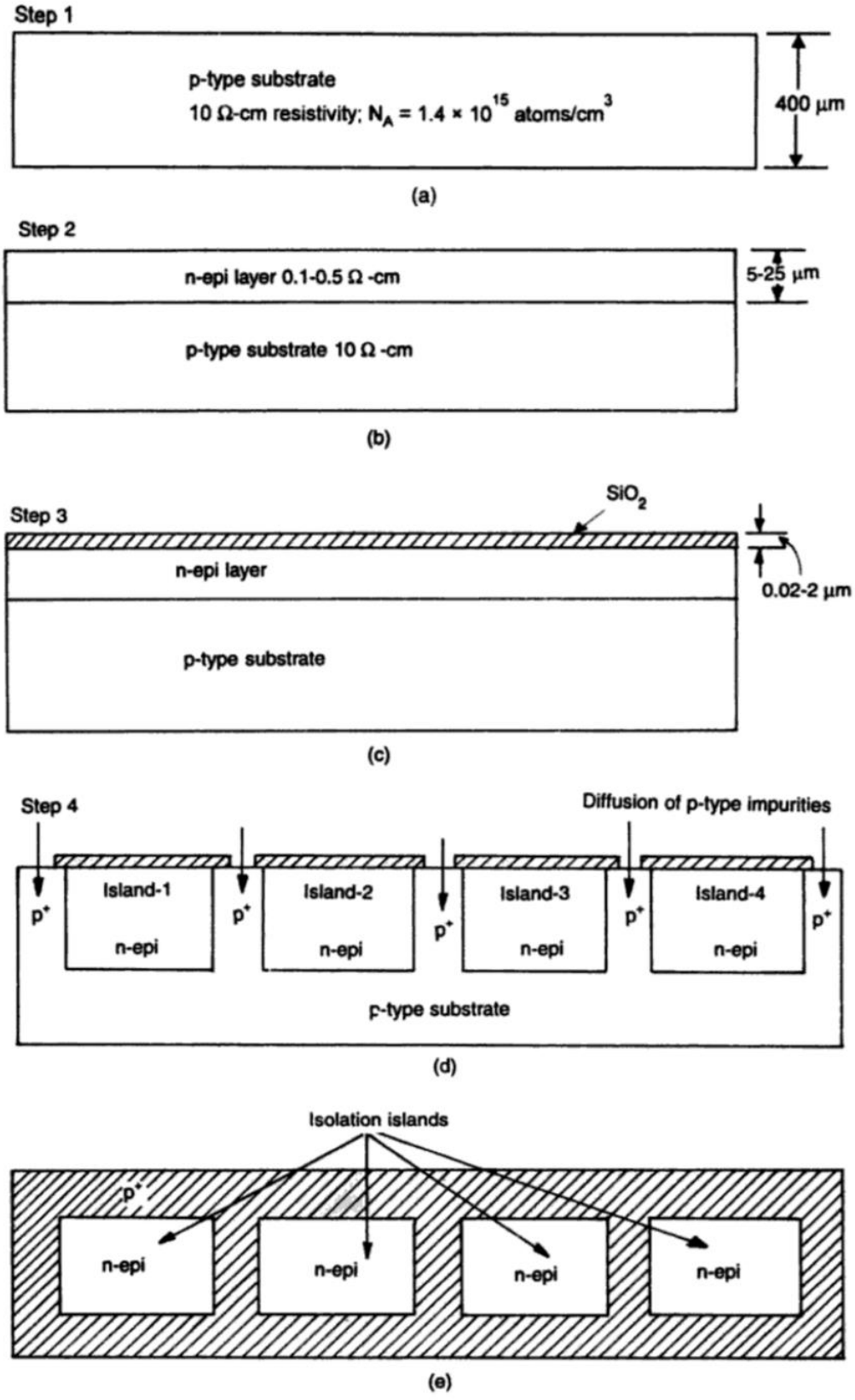

Fig. 1.14 (a-e) Steps in the fabrication of the circuit shown in Fig. 1.3

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even 24 or 36 or 42 leads are also available for special circuits. Ceramic packages, whether of flat type or dual-in-line are costly due to fabrication process, but have the advantage of best hermetic sealing. Most of the general purpose ICs are dual-in-line plastic packages due to economy. Figure 1.13 (a, b) shows the exploded view of TO-5 and flat package.

1.6 FABRICATION OF A TYPICAL CIRCUIT

We shall here show the various steps utilized in converting the circuit of Fig. 1.3 into the monolithic IC of Fig. 1.4.

Step-1: Wafer Preparation

Refer Fig. 1.14 (a). The starting material called the substrate is a *p*-type silicon wafer prepared as discussed in Sec. 1.5.1. The wafers are usually of 10 cm diameter and 0.4 mm(~ 400 μm) thickness. The resistivity is approximately 10 Ω-cm corresponding to concentration of acceptor atom, $N_A = 1.4 \times 10^{15}$ atoms/cm^3.

Step-2: Epitaxial Growth

An *n*-type epitaxial film (5–25 μm) is grown on the *p*-type substrate as shown in Fig. 1.14 (b). The ultimately becomes the collector region of the transistor, or an element of the diode and diffused capacitor associated with the circuit. So in general it can be said that all active and passive components are fabricated within this layer. The resistivity of *n*-epitaxial layer is of the order of 0.1 to 0.5 Ω-cm.

Step 3: Oxidation

Refer Fig. 1.14 (c) A SiO_2 layer of thickness of the order of 0.02 to 2 μm is grown on the *n*-epitaxial layer.

Step 4: Isolation Diffusion

In the circuit of Fig. 1.3 four components have to be fabricated, so we require four islands which are isolated. For this, SiO_2 is removed from five different places using photolithographic technique. Refer Fig. 1.14 (d). The wafer is next subjected to heavy *p*-type diffusion for a long time interval so that *p*-type impurities penetrate the *n*-type epitaxial layer and reach the *p*-type substrate. The area under the SiO_2 are *n*-type islands that are completely surrounded by *p*-type moats. As long as the *pn* junctions between the isolation islands are held at reverse bias, that is, the *p*-type substrate is held at a negative potential with respect to the *n*-type isolation islands, these regions are electrically isolated from each other by two back-to-back diodes, providing the desired isolation.

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1.5.9 Assembly Processing and Packaging

Each of the wafer processed contains several hundred chips, each being a complete circuit. So these chips must be separated and individually packaged. A common method called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package.

There are three different package configurations available.

1. TO-5 glass metal package
2. Ceramic flat package
3. Dual-in-line (ceramic or plastic type)

TO-5 packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but

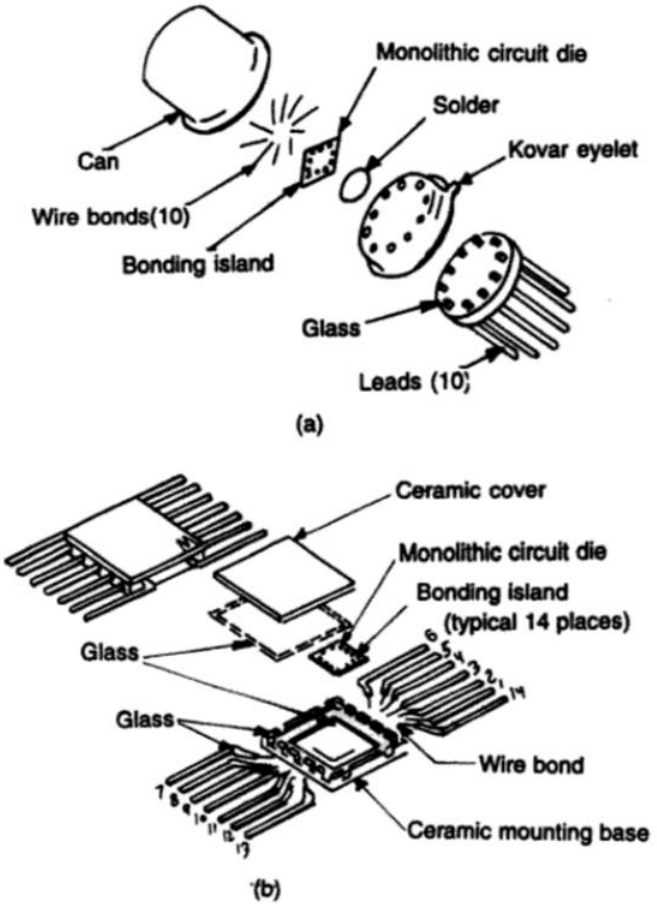

Fig. 1.13 Exploded view of (a) lead TO-5 package (b) 14-lead version of the flat package, showing the various components as well as the completed flat package

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1.5.8 Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages.

1. It is relatively a good conductor.
2. It is easy to deposit aluminium films using vacuum deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, non-rectifying (i.e. ohmic) contact with *p*-type silicon and the heavily doped *n*-type silicon.

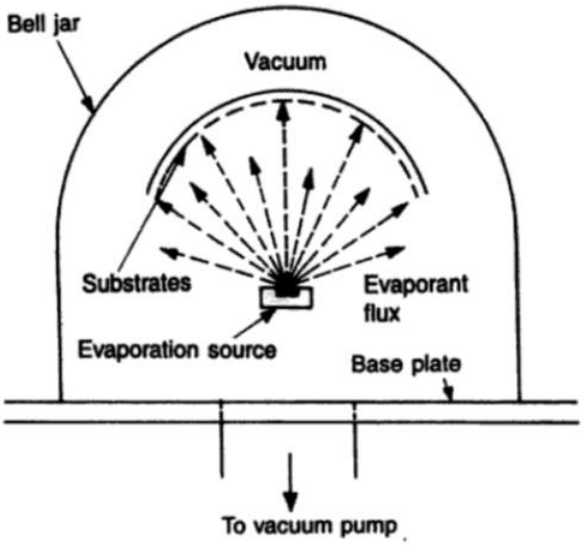

Fig. 1.12 Vacuum evaporation for metallization

The film thickness of about 1 μm and conduction width of about 2 to 25 μm are commonly used. The process takes place in a vacuum evaporation chamber as shown in Fig. 1.12. The pressure in the chamber is reduced to the range of about 10^{-6} to 10^{-7} torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focussed at the surface of the material to be evaporated. This heats up the material to very high temperature and it starts vaporizing. These vapors travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration. This is done by photolithographic process and aluminium is etched away from unwanted places by using etchants like phosphoric acid (H_3PO_4).

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biased providing electric isolation between these islands. The different components are fabricated in these isolation islands. The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher (p^+) than the p-type substrate. This prevents the depletion region of the reverse biased diode from penetrating more into p^+ region and possibly connecting the isolation islands.

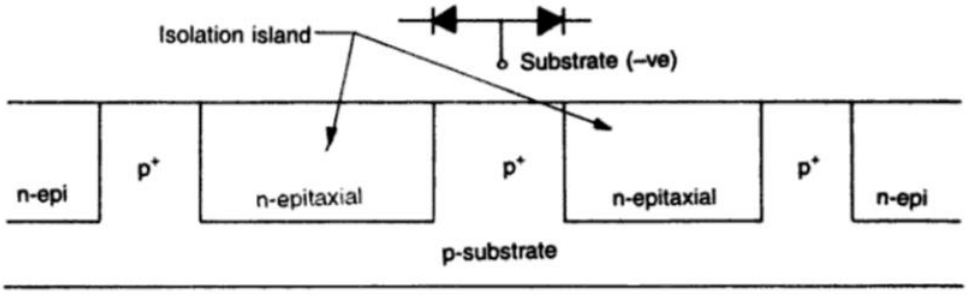

Fig. 1.11 (a) *p-n* junction isolation

There is, however, one undesirable by-product of this isolation process. It is the presence of a transition capacitance at the isolating *pn* junctions, resulting in an inevitable capacitor coupling between the components and the substrate. These parasitic capacitances limit the performance of the circuit at high frequencies. But being economical, this technique is commonly used for general purpose ICs.

Dielectric Isolation

Here a layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical. This isolating dielectric layer is thick enough so that its associated capacitance is negligible. Also, it is possible to fabricate both *pnp* and *npn* transistor within the same silicon substrate. Since this method requires additional fabrication steps, it becomes more expensive. The technique is mostly used for fabricating professional grade ICs required for specialised applications viz, aerospace and military, where higher cost is justified by superior performance. Figure 1.11 (b) shows such a structure.

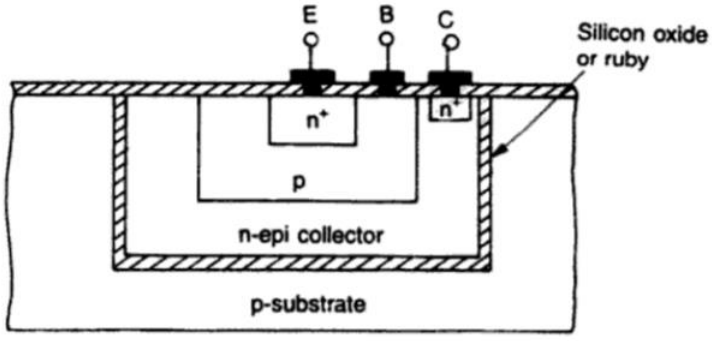

Fig. 1.11 (b) Dielectric isolation

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As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage. Ion implantation technique has two important advantages.

1. It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.

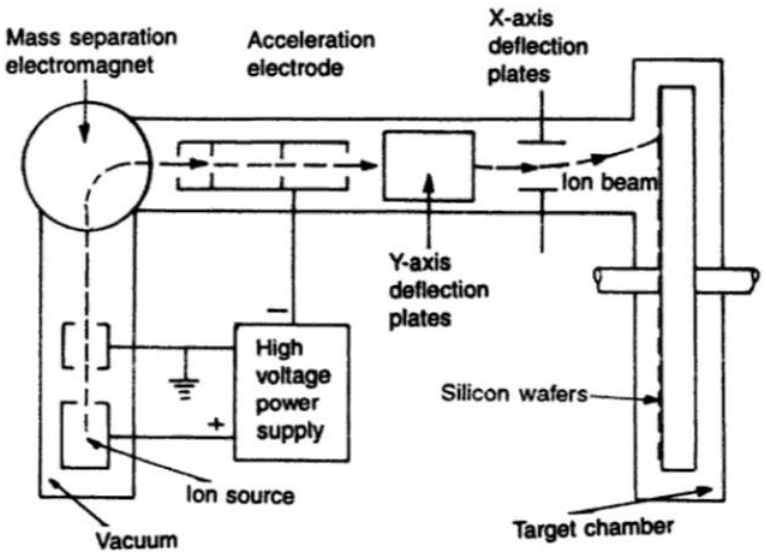

Fig. 1.10 Ion implantation system

1.5.7 Isolation Techniques

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques namely:

pn junction isolation
Dielectric isolation

p-n Junction Isolation

In this isolation technique, p^+ type impurities are selectively diffused into the *n*-type epitaxial layer so as to reach *p*-type substrate as shown in Fig. 1.11 (a). This produces islands surrounded by *p*-type moats. It can be seen that these regions are separated by two back-to-back *p-n* junction diodes. If the *p*-type substrate material is held at the most negative potential in the circuit, the diodes will be reverse

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With the advent of X-ray and electron beam lithography techniques, it has become possible to produce device dimensions down to submicron range (< 1 μm). This is due to much shorter wavelengths involved. With these techniques, MOSFET with gate length as small as 0.25 μm have been made. The cost of X-ray or electron beam equipment is very high and the exposure times very much longer than with UV photolithography. So this becomes a very expensive process and is used only when very small device dimensions (≤ 1 μm) are needed.

1.5.5 Diffusion

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the Silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20″ length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C. Impurities to be diffused are rarely used in their elemental forms. Normally, compounds such as B_2O_3 (Boron oxide), BCl_3 (Boron chloride) are used for Boron and P_2O_5 (Phosphorous pentaoxide) and $POCl_3$ (Phosphorous oxychloride) are used as sources of Phosphorous. A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.

The diffusion of impurities normally takes place both laterally as well as vertically. Therefore, the actual junction profiles will be curved as shown in Fig. 1.9. However, for the sake of simplicity, lateral diffusion will be omitted in all the drawings.

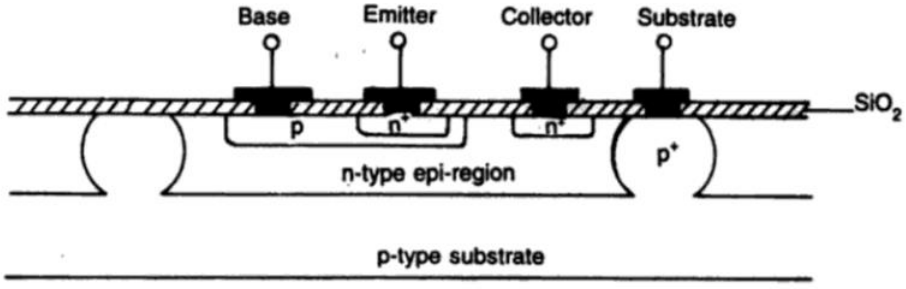

Fig. 1.9 The cross-section of an *npn* transistor showing curved junction profiles as a result of lateral diffusion

1.5.6 Ion Implatation

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high-energy dopant ions (borons for *p*-type and phosphorus for *n*-type) as shown in Fig. 1.10. These ions are accelerated by energies between 20 kV to 250 kV.

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Photo-etching is used for the removal of SiO_2 from desired regions so that the desired impurities can be diffused. The wafer is coated with a film of photosensitive emulsion (Kodak Photoresist KPR). The thickness of the film is in the range of 5000–10000 Å as shown in Fig. 1.8 (a). The mask negative of the desired pattern) as prepared by steps described earlier is placed over the photoresist coated wafer as shown in Fig. 1.8 (b). This is now exposed to ultraviolet light, so that KPR becomes polymerized beneath the transparent regions of the mask. The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed/ unpolymerized regions on the photoresist and leaves the pattern as shown in Fig. 1.8 (c). The polymerised photoresist is next fixed or cured, so that it becomes immune to certain chemicals called etchants used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the SiO_2 from the areas which are not protected by KPR as shown in Fig. 1.8 (d) After diffusion of impurities, the photoresist is removed with a chemical solvent (hot H_2SO_4) and mechanical abrasion.

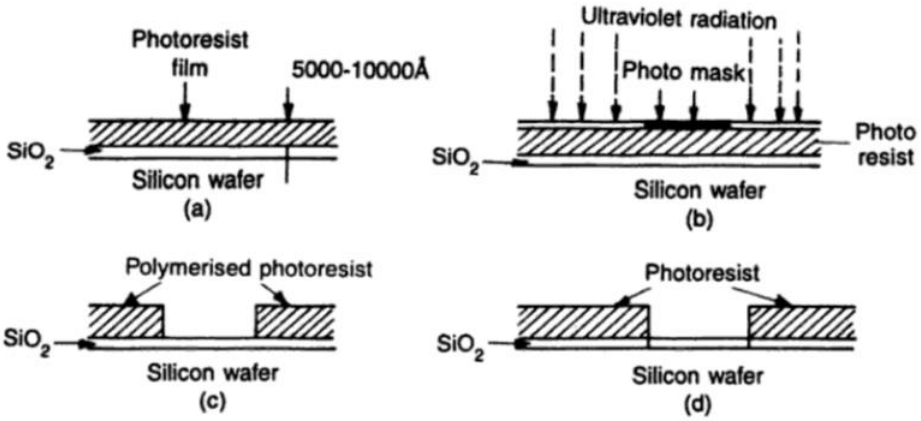

Fig. 1.8 Various steps for photo-etching

The etching process described is a wet etching process and the chemical reagents used are in liquid form. A new process used these days is a dry etching process called plasma etching. A major advantage of the dry etching process is that it is possible to achieve smaller line openings (≤ 1 μm) compared to wet process. Complete description of the plasma etching process is beyond the scope of this book.

X-Ray and Electron Beam Lithography

With conventional ultraviolet (UV) photolithography process in which the UV wavelengths used are in the range 0.3 to 0.4 μm, the minimum device dimensions or line widths are limited by diffraction effects to around five wavelengths or about 2 μm. This is what puts an upper limit on the IC device density using UV photolithography.

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conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2 μm can be obtained. However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become possible to produce device dimension down to submicron range (< 1 μm).

Photolithography involves two processes, namely:
Making of a photographic mask
Photo etching

The making of a photographic mask involves the following sequence of operations—first the preparation of initial artwork and secondly, its reduction. The initial layout or artwork of an IC is normally done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. This is because, for a tiny chip, larger the artwork, more accurate is the final mask. For example, it is often required to make an opening of width about 1 mil (25 μm). Obviously, this cannot be managed by any draftsman even with his thinnest of sketch pens. So the drawings are made magnified and often by a factor of 500. With this magnification, it is easy to see that a width of one mil is magnified to a width of 500 mils, that is, about 1.2 cm. Therefore, for a finished monolithic chip of area 50 mil × 50 mil, the artwork will be made on an area of about 60 cm × 60 cm.

This initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule, e.g., a mask for base diffusion, another for collector diffusion, another for metallization and so on.

For photographic purpose, artwork should not contain any line drawings but must be of alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque mylar (trade name-Rubylith). The red layer can be easily peeled off thus exposing clear areas with a knife edge from the regions where impurities have to be diffused. The artwork is usually produced on a precision drafting machine, known as coordinatograph. The coordinatograph has a cutting head that can be positioned accurately and moved along two perpendicular axes. The coordinatograph outlines the pattern cutting through the red mylar without damaging the clear layer underneath.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image also must be repeated many times in a matrix array, so that many ICs will be produced in one process. The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposure, the plate is moved in equal steps so that successive images form in an array. When the exposed plate is developed, it becomes a master mask. The masks, actually used in IC processing are made by contact printing from the master. These working masks wear out with use and are replaced as required.

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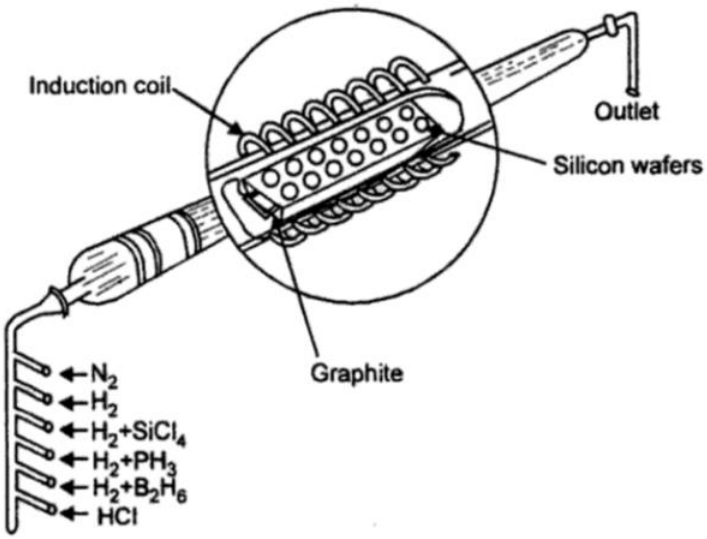

Fig. 1.7 A diagrammatic representation of a system for growing silicon epitaxial films

1.5.3 Oxidation

SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.
2. By selective etching of SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing O_2 or H_2O or both. The chemical reaction is

$$Si + 2H_2O \longrightarrow SiO_2 + 2H_2$$

This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.

1.5.4 Photolithography

With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers. As many as 10,000 transistors can be fabricated on a 1 cm × 1 cm chip. The

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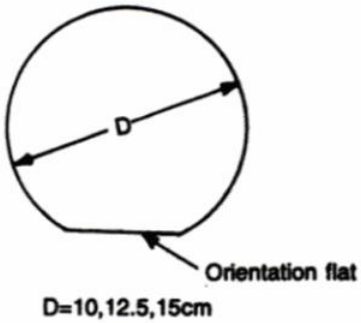

Fig. 1.6 Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit. After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

1.5.2 Epitaxial Growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiC_4 + 2H_2 \underset{}{\overset{1200°C}{\rightleftharpoons}} Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the n-type and bi-borane (B_2H_6) for p-type doping into the silicon-tetrachloride hydrogen gas stream.

The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C. The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

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is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.

Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter (D = 10, 12.5, 15 cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then sliced using a stainless

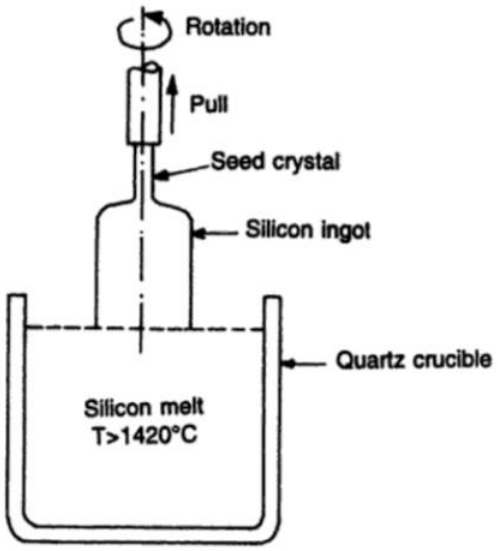

Fig. 1.5 Czochralski crystal growth

steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in Fig. 1.6. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23–40 mils produces wafers of 16–32 mils thickness after all the polishing steps.

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An IC in general, consists of four distinct layers, as follows:

Layer No. 1 (~ 400 μm)	is a *p*-type silicon substrate upon which the integrated circuit is fabricated.
Layer No. 2 (~ 5–25 μm)	is a thin *n*-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.
Layer No. 3 (0.02–2μm)	is a very thin SiO_2 layer for preventing diffusion of impurities wherever not required using photolithographic technique.
Layer No. 4 (~ 1μm)	is an aluminium-layer used for obtaining interconnection between components.

It may be pointed out that the drawings showing the cross-sectional view in this chapter are never scale drawings, but are distorted for the particular emphasis required.

1.5 BASIC PLANAR PROCESSES

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail

1.5.1 Silicon Wafer Preparation

The following steps are used in the preparation of Si-wafers

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant

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1.4 FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

A monolithic circuit, literally speaking, means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek word *monos* meaning 'single' and *lithos* meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

The most significant advantage of integrated circuit of reducing the cost of production of electronic circuits due to batch production can be easily visualized by a simple example. A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously. Many chips so produced will be faulty due to imperfection in the manufacturing process. Even if the yield (percentage of fault free chips/wafer) is only 20 percent, it can be seen that 16,000 good chips are produced in a single batch.

The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit of Fig. 1.3 when fabricated by silicon planar technology will have the cross-sectional view shown in Fig. 1.4.

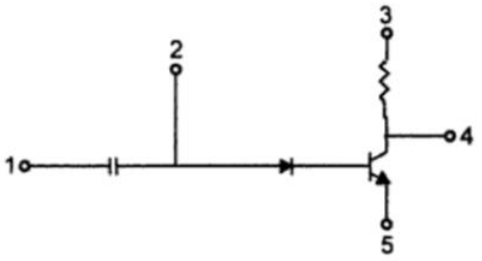

Fig. 1.3 A typical circuit

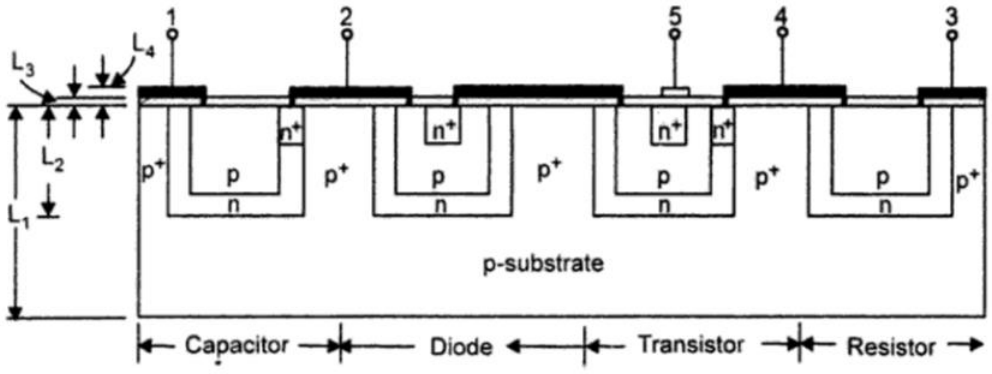

Fig. 1.4 Complete cross-sectional view of the circuit in Fig. 1.3 when transformed into monolithic form

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Invention of transistor (Ge)		1947
Development of Silicon transistor		1955–1959
Silicon Planar Technology	Junction transistor diode	1959
First ICs, Small Scale Integration (SSI)	3 to 30 gates/chip approx. or 100 transistors/chip (Logic gates, Flip-flops)	1960–65
Medium Scale Integration (MSI)	30 to 300 gates/chip or 100 to 1000 transistors/chip (Counters, Multiplexers, Adders)	1965–1970
Large Scale Integration (LSI)	300 to 3000 gates/chip or 1000–20,000 transistors/chip (8 bit microprocessors, ROM, RAM)	1970–1980
Very Large Scale Integration (VLSI)	More than 3000 gates/chip or 20,000–1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980–1990
Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$ transistors/chip (Special processors, Virtual reality) machines, Smart sensors	1990–2000
Giant-Scale Integration (GSI)	> 10^7 transistors/chip	

Over the years, the device density has increased together with some increase in the chip area. Figure 1.2 (a, b, c) show small (SSI), medium (MSI) and large (LSI or VLSI) IC chip size. The chip areas range from 1 mm^2 (1600 mil^2)* for the SSI chip to 1 cm^2 (160,000 mil^2) for the LSI chip.

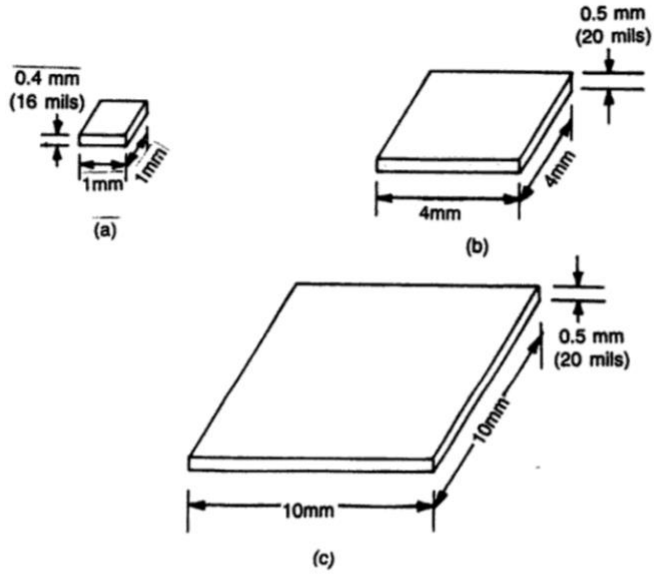

Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

* mil = 0.001 in = 25.4 μm = 0.0254 mm

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1.2 CLASSIFICATION

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.

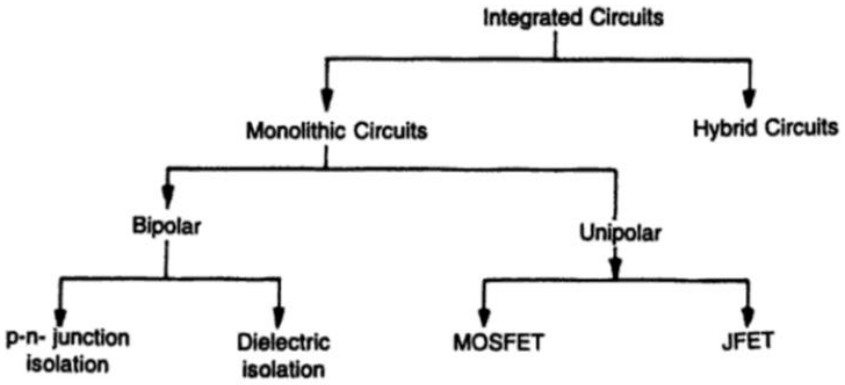

Fig. 1.1 Classification of ICs

1.3 IC CHIP SIZE AND CIRCUIT COMPLEXITY

UP until the 1950s, the electronic device technology was dominated by the vacuum tube. The present day electronics is the result of the invention of the transistor in 1947. The invention of the transistor by William B. Shockley, Walter H. brattain and John Bardeen of Bell Telephone Laboratories was followed by the development of the Integrated circuit (IC). The concept of IC was introduced at the beginning of 1960 by both Texas Instruments and Fairchild Semiconductors. Since that time, the size and complexity of ICs have increased rapidly as shown by the brief chronology.

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Unit II: Operational Amplifiers

Introduction toLinearICs– BJT differential amplifier-Operational amplifierIC741–Block diagramandCharacteristics-Inverting,non-invertinganddifferenceamplifier–Adder, Subtractor, Integrator,Differentiator-Comparator- Windowdetector-Regenerative comparator(Schmitttrigger)-Precisionrectifier-Currenttovoltageconverter– Voltagetocurrentconverter-Log and antilogamplifiers-Instrumentation amplifiers.

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2 Marks

1. **List characteristic of an ideal op-amp. (April-14), (Nov-15A)**

   - Infinite voltage gain
   - Zero output impedance
   - Infinite input impedance
   - Zero offset voltage
   - Infinite bandwidth
   - Infinite CMRR.
   - Infinite slew rate.

2. **Define CMRR. What is the ideal value of CMRR. (April-14), (Nov-15A)**

Common Mode Rejection Ratio is the figure of merit of a differential amplifier and is given by,

$$CMRR = \frac{gain\ of\ the\ amplifier\ for\ a\ difference\ mode\ input\ signal}{gain\ of\ the\ amplifier\ for\ a\ common\ mode\ input\ signal}$$

$$CMRR = \frac{A_{dm}}{A_{cm}}$$

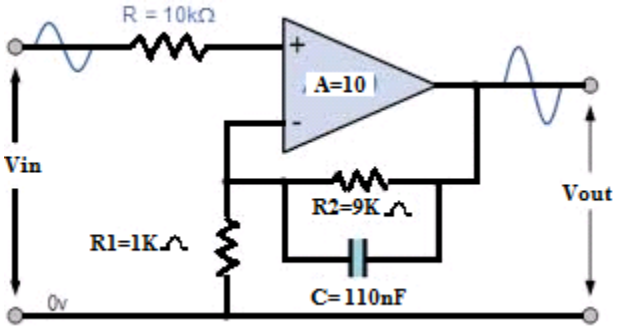
It is also defined as the ability of the differential amplifier to reject the common mode signal. An ideal differential amplifier would have infinite CMRR

3. **Define slew rate. What causes it? (Dec-14) (April-15)**

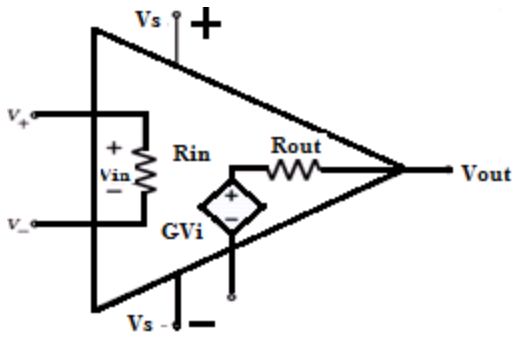
   - The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage

- There is a capacitor with-in or outside of an op-amp to prevent oscillation. This capacitor which prevents the output voltage from responding to a fast changing input. This is the causes for slew rate.

4. **Draw the circuit arrangement for a non-inverting amplifier for AC application. (Dec-14)**

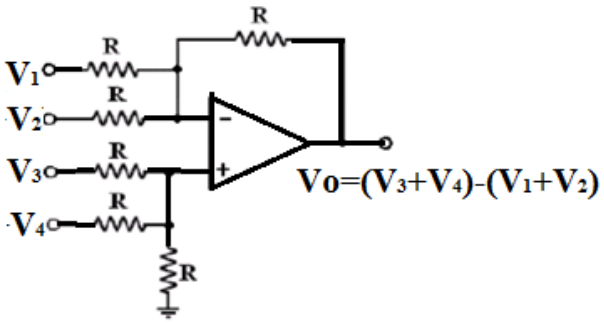


5. **Draw the equivalent circuit of practical op-amp. (April-15)**



An equivalent circuit of an operational amplifier that models some resistive non-ideal parameters

6. **Draw the op-amp adder-subtractor circuit to get the output voltage $V_o=(V_3+V_4)-(V_1+V_2)$. (Nov-15)**



7. What is a window detector? (Nov-15)

A window detector circuit, also called window comparator circuit or dual edge limit detector circuits is used to determine whether an unknown input is between two precise reference threshold voltages. It employs two comparators to detect over-voltage or under-voltage.

8. Define CMRR of op-amp. (Nov-13)

The op amp common-mode rejection ratio (CMRR) is the ratio of the common-mode gain to differential-mode gain. For example, if a differential input change of Y volts produces a change of 1 V at the output, and a common-mode change of X volts produces a similar change of 1 V, then the CMRR is X/Y

9. What is mean by Differential Amplifier?

A differential amplifier is a circuit that accepts two input signals and amplifies the difference between these input signals.

The output voltage is given as $V_o = A (V_{in1} – V_{in2})$

Where, V_o – Output voltage

A – Gain of differential amplifier

V_{in1} – First input signal or voltage

V_{in2} – Second input signal or voltage

10.Why we go for differential amplifier? (Or) What is the need of differential amplifier?

The need for differential amplifier arises in many physical measurements, in medical electronics and in direct coupled amplifier applications. In this amplifier, there will be no output voltage resulting from thermal drifts or any other changes provided and changes in both halves of the circuits are equal.

11.Define common mode signal.

When the input signals to differential amplifier are in phase and exactly equal in magnitude, they are called common mode signals. The common signals are rejected (not amplified) by the differential amplifier.
Eg: Noise Signal.

12. Define Differential mode signal.

When the input signals to differential amplifier are 180^0 out of phase and exactly equal in magnitude, they are called common mode signals. These signals are amplified by the differential amplifier.

13. What are the applications of a differential amplifier?

The applications of a differential amplifier are,
a. To measure many physical quantities,
b. Can be used as a direct coupled amplifier,
c. Used in operational amplifier.

14.Define an operational amplifier.

An operational amplifier is a direct-coupled, high gain amplifier consisting of one or more differential amplifier. By properly selecting the external components, it can be used to perform a variety of mathematical operations.

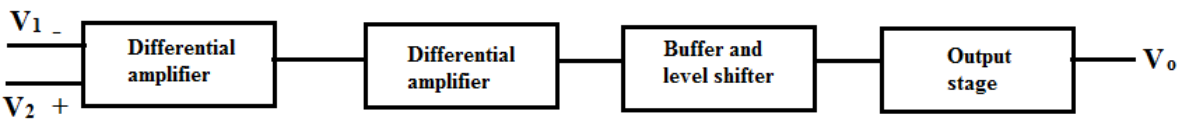
15. State the concept of virtual ground?

This means the differential input voltage V_d between the non inverting and inverting input terminals is essentially zero.

If the non-inverting terminal is grounded by the concept of virtual short, the inverting terminal is also at ground potential, though there is no physical connection between the inverting terminal and the ground. This is the principle of virtual ground.

16. List the four basic building blocks of an op amp.

The basic block diagram constitutes mainly four stages
1. Input stage
2. Intermediate Stage
3. Buffer and Level Shifting stage
4. Output Stage



17. What happens when the common terminal of V+ and V- sources is not grounded?

If the common point of the two supplies is not grounded, twice the supply voltage will get applied and it may damage the op-amp.

18. Define input offset voltage.

A small voltage is applied to the input terminals to make the output voltage as zero when the two input terminals are grounded is called input offset voltage.

19. Define input offset current. State the reasons for the offset currents at the input of the op-amp.

The difference between the bias currents at the input terminals of the op-amp is called as input offset current. The input terminals conduct a small value of dc current to bias the input transistors. Since the input transistors cannot be made identical, there exists a difference in bias currents.

20. Why IC 741 is not used for high frequency applications?

IC741 has a low slew rate because of the predominance of capacitance present in the circuit at higher frequencies. As frequency increases the output gets distorted due to limited slew rate.

21. What are the advantages of voltage follower?

a. Very large input resistance, of the order of mega ohms.
b. Low output impedance, almost zero. Hence it can be used to connect high impedance source to a low impedance load as a buffer.
c. It has large band width.
d. The output follows the input exactly without phase shift.

22.What is meant by integrator?

In an integrator circuit, the output voltage is the integration of the input voltage. The integrator circuit using active devices like op-amp is called active integrator. The integrator circuit can be obtained without using active devices like op amp, transistors is called passive integrator.

23.Write the applications of Practical Integrator.

1. Analog computers
2. In solving the differential equations
3. In analog to digital converters
4. In ramp generators

24.What is meant by differentiator?

The circuit which produces the differentiation of the input voltage at its output is called differentiator. The circuit using active devices like op-amp is called active differentiator. The circuit can be obtained without using active devices like op amp, transistors is called passive differentiator.

25. Write the applications of Practical differentiator.

- In the wave shaping circuits to detect the high frequency components in the input signal.
- As a rate- of-change detector in the FM demodulation.

26. Write down the condition for good differentiation?

For good differentiation the time period of the input signal must be greater than or equal to $R_F C_1 T > R_f C_1$.

Where R_f is the feedback resistance C_f is the input capacitance.

27.What is the need for an instrumentation amplifier?

The measurement of the physical quantities is generally carried out with the help of a device called as transducer, but most of the transducer outputs are generally of very low level signals such a low level signals are not sufficient to drive the next stage of the system, hence the special amplifier which is used for such a low level amplification with high CMRR, high input impedance to avoid loading, low power consumption is called instrumentation amplifier.

28. List the features of instrumentation amplifier.

- High gain accuracy
- High CMRR
- High gin stability with low temperature coefficient
- Low dc offset
- Low output impedance

29. What is a comparator?

A comparator is a circuit which compares a signal voltage applied at one input of an opamp with a known reference voltage at the other input. It is an open loop op - amp with output +Vsat.

30. What are the applications of comparator?

- Zero crossing detectors
- Window detector
- Time marker generator
- Phase detector.

31. What are the applications of op-amp?

Because of low cost, small size, versatility, flexibility and dependability op-amps are used in the fields of,

- Process control and instrumentation.
- Computers and communication systems.
- Power and signal sources
- Measuring and display systems.

32. Write any three characteristics of practical op-amp.?

- **Open loop gain:** it is the voltage gain of the op-amp when no feedback is applied. Practically it is several thousands.
- **Input impedance:** it is finite and typically greater than 1 M ohm.
- Output impedance: it is typically few hundred ohms. With the help of negative feedback, it can be reduced to a very small value like 1 or 2 ohms.
- **Bandwidth:** the bandwidth of practical op-amp in open loop configuration is very small. By application of negative feedback, it can be increased to a desired value.
- **Input offset voltage:** the dc voltage, which makes the output voltage zero, when the other terminal is grounded is called input offset voltage.

33. Define PSRR.

The power supply rejection ratio (PSRR) is defined as the ratio of the change in input offset voltage due to the change in supply voltage producing it, keeping other power supply voltage constant. It is also called power supply sensitivity (PSS)

34. Write the practical value of the following of IC 741.

s.no	**Parameter**	Practical value
1	Open loop voltage gain	$2*10^5$
2	Output impedance	75 ohms
3	Input impedance	2 m ohms
4	Input offset current	200 nano A
5	Input offset voltage	2 milli volt
6	Bandwidth	1 mega hertz

7	CMRR	90 dB
8	Slew rate	0.5 V/ micro sec
9	Input bias current	80 nano A
10	Power supply rejection ratio (PSRR)	30 micro volt / V

35. Why op amp cannot be used in open loop configuration?

Due to high open loop gain, op amp either shows +V sat or –V sat level. This indicates the inability of op amp to work as a linear small signal amplifier in the open loop mode. Hence, the op amp is generally not used as amplifier in the open loop configuration.

36. What is the advantage of negative feedback in op amp circuit?

- Reduced Open loop gain.
- Improves stability
- Reduces frequency distortion
- It reduces the non-linearity and noise in op amp
- Improves frequency response

37. Explain the principle of zero crossing detectors?

The basic comparator can be used as the zero crossing detector i.e., it compares the signal voltage applied at one input of an op amp with a known reference voltage at the other input, and produces either a high or a low output voltage, depending on which input is higher.

38. Define precision rectifier?

The major limitation of rectifier circuit using diodes is that they cannot rectify the voltages below cut-in voltage of diodes. A circuit which used for the rectification of voltage below the cut-in voltage and provides the ideal diode characteristics is called precision rectifier.

39. List out the practical application of the integrator and differentiator?

Integrator:

- In the analog computers.
- In solving the differential equations.
- In analog to digital converters.
- Various signal wave shaping circuits.
- In ramp generators.

Differentiator:

- In the wave shaping circuits to detect the high frequency components in the input signal.
- As a rate-of –change detector in the FM demodulators.

40. Why instrumentation amplifier should have high slew rate and input impedance?

The slew rate of the instrumentation amplifier must be as high as possible to provide maximum undistorted output voltage swing.

It should have high input impedance in order to avoid the loading of input sources.

41. Mention the advantages of instrumentation amplifier using op amp?

The advantages of this circuit are,

- The gain variation is easy and precise.
- Gain depends on external resistances and hence can be adjusted accurately and made stable by selecting high quality resistances.
- The input impedance depends on the input impedance of non inverting amplifiers which is extremely high.
- The CMRR of the op amp is very high and most of the common mode signal will be rejected.

42. Write some applications of instrumentation amplifier?

The instrumentation amplifier along with the transducer bridge can be used in many practical applications some of them are temperature controller, temperature indicator, light intensity meter, analog weight scale.

43. Define V – I and I – V converter?

V-I converter: It is the circuit in which the output load current is proportional to the input voltage. Depending upon the connection of load there are two types of V I converter namely floating load type and grounded load type

I-V converter: It is the circuit in which the output voltage is proportional to input current.

44. What are other names of V-I converter and I-V converter?

V-I converter is also known as Transresistance amplifier or voltage controlled current source.

I-V converter is also known as Transconductance amplifier or current controlled voltage source.

45. What are the application of V-I converter?

The various application of V-I converter are

- Low voltage dc voltmeter
- Low voltage ac voltmeter
- Diode tester and match finder
- Zener diode tester

46. What are the applications of I-V converter?

The I-V converters were used in photodiode detector, photoFET detector.

47. What is comparator and write the type of comparator?

A comparator is a circuit which compares a signal voltage applied at one input of an op amp with a known reference voltage at the other input.

There are two types of comparator namely inverting comparator and non-inverting comparator.

48. Write the limitations of the op-amp as comparator?

1. To have better comparator accuracy op amp must have CMRR, high gain, and negligible input offset current and input offset voltage.

2. To have better response time op amp output must switch rapidly, between saturation levels and also respond instantaneously to any change of condition at its input.

3. To have output compatibility with digital devices op amp output must swing between two logic levels suitable for certain logic family.

49. Application of the comparator?

The various application of the comparator are, Zero crossing detector ,Level detector, Window detector, Duty cycle controller, Pulse generator, Time marker generator, Phase detector.

50. Define log and antilog Amplifier?

Log amplifier: The circuit in which the output is obtained as the function of logarithm of the input voltage V_{in} is called log amplifier. The output obtained in this circuit is in natural logarithm to obtain the logarithm to base 10 proper scaling is to done.

Log10 X = 0.4343 ln (X).

Antilog amplifier: The log amplifier can be easily turned around to provide antilog or exponential function called as antilog amplifier. When compared to the log amplifier the position of diode and resistor are interchanged.

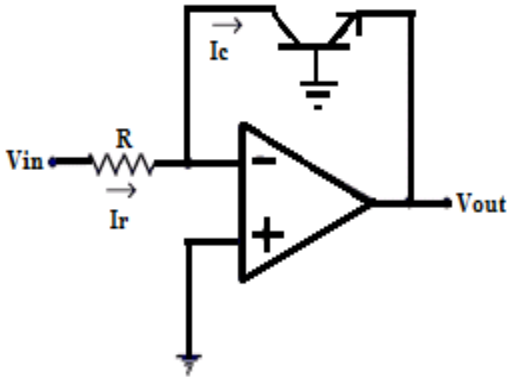
51. List the applications of log amplifiers?

- Analog computation may require functions such as lnx, logx, sinhx etc. These functions can be performed by log amplifiers
- Log amplifiers can perform direct db display on digital voltmeter and spectrum analyzer
- Log amplifier can be used to compress the dynamic range of a signal

52. What are the applications of the analog multiplier?

There is no. of applications of analog multiplier such as Frequency doublers, frequency shifting, and phase angle detection, real power computation, squaring of signals, dividing and multiplying two signals.

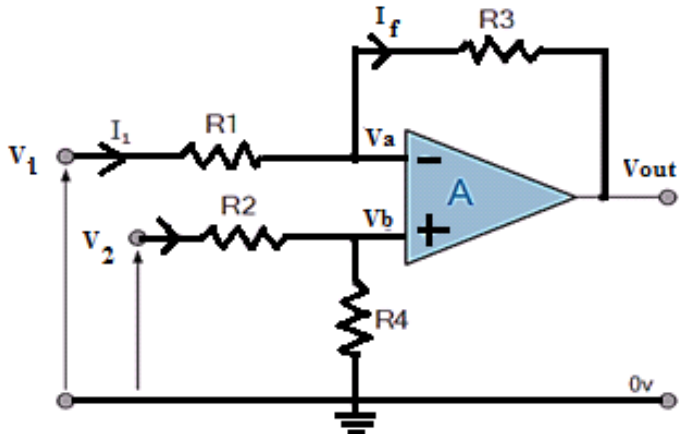
53. Draw a circuit of a log amplifier using op amp and a transistor.



54. Write short notes on Schmitt trigger

Schmitt trigger is a regenerative comparator. It converts sinusoidal input into a square wave output. The output of Schmitt trigger swings between upper and lower threshold voltages, which are the reference voltages of the input waveform. (Or) Schmitt trigger is an inverting comparator with positive feedback.

55. Drawop amp circuits that can be used as a subtractor circuit and write its output equation.



Output equation

By connecting each input in turn to 0V ground, by superposition to solve for the output voltage V_{out}.

$$I_1 = \frac{V_1 - V_a}{R_1}, \quad I_2 = \frac{V_2 - V_b}{R_2}, I_f = \frac{V_a - (V_{out})}{R_3}$$

Summing point $V_a = V_b$

$$V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

If $V_2 = 0$, then $V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$

If V_1=0, then: $V_{out(a)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$

$$V_{out(a)} = V_{out(a)} + V_{out(b)}$$

$$V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistor, $R_1=R_2$ and $R_3=R_4 V_{out}$ can be simplified:-

$$V_{out} = \frac{R_3}{R_1}(V_2 - V_1)$$

56. Applications of Schmitt trigger circuit?

- Squaring circuit
- Sine-to-Square comparator
- Amplitude comparator
- As flip flops

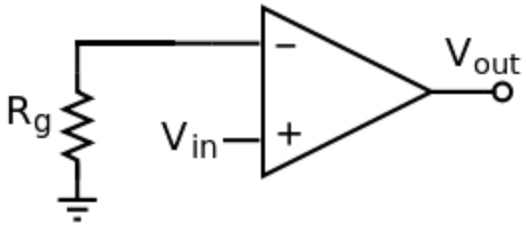
11 marks

1. Compare the ideal and practical characteristics of op-amp. (3) (Nov-13)

The amplifier's differential inputs consist of a non-inverting input (+) with voltage V_+ and an inverting input (–) with voltage $V_–$; ideally the op-amp amplifies only the difference in voltage between the two, which is called the *differential input voltage*. The output voltage of the op-amp V_{out} is given by the equation:

Open loop amplifier

The magnitude of AOL is typically very large—100,000 or more for integrated circuit op-amps—and therefore even a quite small difference between V+ and V− drives the amplifier output nearly to the supply voltage. Situations in which the output voltage is equal to or greater than the supply voltage are referred to as saturation of the amplifier. The magnitude of AOL is not well controlled by the manufacturing process, and so it is impractical to use an open loop amplifier as a stand-alone differential amplifier.

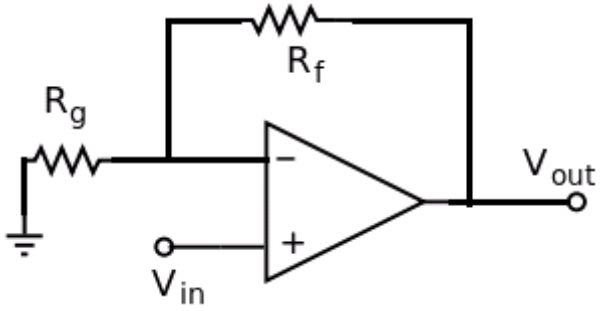


$$V_{out} = A_{OL}(V_+ - V_-)$$

whereA_{OL} is the open-loop gain of the amplifier

Closed loop

- The closed loop feedback greatly reduces the gain of the circuit. When negative feedback is used, the circuit's overall gain and response becomes determined mostly by the feedback network, rather than by the op-amp characteristics.



The input signal V_{in} appears at both (+) and (−) pins, resulting in a current i through R_{g} equal to $V_{\text{in}}/R_{\text{g}}$.

$$i = \frac{V_{\text{in}}}{R_g}$$

Since Kirchhoff's current law states that the same current must leave a node as enter it, and since the impedance into the (−) pin is near infinity, we can assume practically all of the same current i flows through R_{f}, creating an output voltage

$$V_{\text{out}} = V_{\text{in}} + i \times R_f = V_{\text{in}} + \left(\frac{V_{\text{in}}}{R_g} \times R_f\right) = V_{\text{in}} + \frac{V_{\text{in}} \times R_f}{R_g} = V_{\text{in}}\left(1 + \frac{R_f}{R_g}\right)$$

By combining terms, we determine the closed-loop gain A_{CL}:

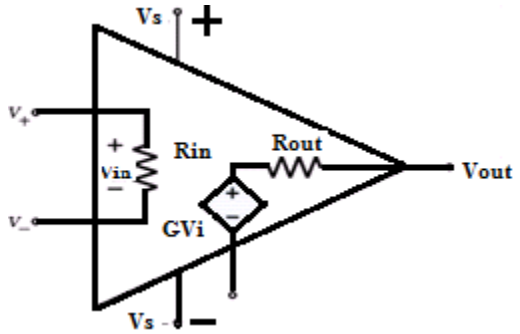
$$A_{\text{CL}} = \frac{V_{\text{out}}}{V_{\text{in}}} = 1 + \frac{R_f}{R_g}$$

Op-amp characteristics of Ideal op-amps

An ideal op-amp is usually considered to have the following properties:

- Infinite open-loop gain G = v_{out} / v_{in}
- Infinite input impedanceR_{in}, and so zero input current
- Zero input offset voltage
- Infinite output voltage range
- Infinite bandwidth with zero phase shift and infinite slew rate
- Zero output impedance R_{out}

- Zero noise
- Infinite common-mode rejection ratio (CMRR)
- Infinite power supply rejection ratio.



An equivalent circuit of an operational amplifier that models some resistive non-ideal parameters

These ideals can be summarized by the two rules:

I. **In a closed loop** the output attempts to do whatever is necessary to make the voltage difference between the inputs zero.
II. The inputs draw no current

The first rule only applies in the usual case where the op-amp is used in a closed-loop design (negative feedback, where there is a signal path of some sort feeding back from the output to the inverting input). These rules are commonly used as a good first approximation for analyzing or designing op-amp circuits

Op-amp characteristics of Real op-amps

Real op-amps differ from the ideal model in various aspects.

a) DC imperfections

i. Finite gain

Open-loop gain is infinite in the ideal operational amplifier but finite in real operational amplifiers. Typical devices exhibit open-loop DC gain ranging from 100,000 to over 1 million.

ii. Finite input impedances

The *differential input impedance* of the operational amplifier is defined as the impedance *between* its two inputs; the ***common-mode input impedance*** is the impedance from each input to ground. MOSFET-input operational amplifiers often have protection circuits that effectively short circuit any input differences greater than a small threshold, so the input impedance can appear to be very low in some tests. However, as long as these operational amplifiers are used in a typical high-gain negative feedback application, these protection circuits will be

inactive. The input bias and leakage currents described below are a more important design parameter for typical operational amplifier applications.

iii. Non-zero output impedance

Low output impedance is important for low-impedance loads; for these loads, the voltage drop across the output impedance effectively reduces the open loop gain. In configurations with a voltage-sensing negative feedback, the output impedance of the amplifier is effectively lowered; thus, in linear applications, op-amp circuits usually exhibit a very low output impedance indeed.

Low-impedance outputs typically require high quiescent (i.e., idle) current in the output stage and will dissipate more power, so low-power designs may purposely sacrifice low output impedance.

iv. Input current

Due to biasing requirements or leakage, a small amount of current (typically ~10 nanoamperes for bipolar op-amps, tens of picoamperes (pA) for JFET input stages, and only a few pA for MOSFET input stages) flows into the inputs. When large resistors or sources with high output impedances are used in the circuit, these small currents can produce large unmodeled voltage drops. If the input currents are matched, *and* the impedance looking *out* of *both* inputs are matched, then the voltages produced at each input will be equal. Because the operational amplifier operates on the *difference* between its inputs, these matched voltages will have no effect. It is more common for the input currents to be slightly mismatched. The difference is called input offset current, and even with matched resistances a small *offset voltage* (different from the input offset voltage below) can be produced. This offset voltage can create offsets or drifting in the operational amplifier.

v. Input offset voltage

This voltage is required across the op-amp's input terminals to drive the output voltage to zero. In the perfect amplifier, there would be no input offset voltage. However, it exists in actual op-amps because of imperfections in the differential amplifier that constitutes the input stage of the vast majority of these devices. Input offset voltage creates two problems: First, due to the amplifier's high voltage gain, it virtually assures that the amplifier output will go into saturation if it is operated without negative feedback, even when the input terminals are wired together. Second, in a closed loop, negative feedback configuration, the input offset voltage is amplified along with the signal and this may pose a problem if high precision DC amplification is required or if the input signal is very small.

vi. Common-mode gain

A perfect operational amplifier amplifies only the voltage difference between its two inputs, completely rejecting all voltages that are common to both. However, the differential input stage of an operational amplifier is never perfect, leading to

the amplification of these common voltages to some degree. The standard measure of this defect is called the common-mode rejection ratio (denoted CMRR). Minimization of common mode gain is usually important in non-inverting amplifiers (described below) that operate at high amplification.

vii. Power-supply rejection

The output of a perfect operational amplifier will be completely independent from its power supply. Every real operational amplifier has a finite power supply rejection ratio (PSRR) that reflects how well the op-amp can reject changes in its supply voltage.

viii. Temperature effects

All parameters change with temperature. Temperature drift of the input offset voltage is especially important.

ix. Drift

Real op-amp parameters are subject to slow change over time and with changes in temperature, input conditions, etc.

b) AC imperfections

The op-amp gain calculated at DC does not apply at higher frequencies. Thus, for high-speed operation, more sophisticated considerations must be used in an op-amp circuit design.

i. Finite bandwidth

All amplifiers have finite bandwidth. To a first approximation, the op-amp has the frequency response of an integrator with gain. That is, the gain of a typical op-amp is inversely proportional to frequency and is characterized by its **gain–bandwidth product (GBWP)**. For example, an op-amp with a GBWP of 1 MHz would have a gain of 5 at 200 kHz, and a gain of 1 at 1 MHz. This dynamic response coupled with the very high DC gain of the op-amp gives it the characteristics of a first-order low-pass filter with very high DC gain and low cutoff frequency given by the GBWP divided by the DC gain.

The finite bandwidth of an op-amp can be the source of several problems, including:

ii. *Stability*

Associated with the bandwidth limitation is a phase difference between the input signal and the amplifier output that can lead to oscillation in some feedback circuits. For example, a sinusoidal output signal meant to interfere destructively with an input signal of the same frequency will interfere constructively if delayed by 180 degrees forming positive feedback. In these cases, the feedback circuit can be stabilized by means of frequency compensation, which increases the gain or phase margin of the open-loop circuit. The circuit designer can implement this compensation externally with a separate circuit component. Alternatively, the

compensation can be implemented within the operational amplifier with the addition of a dominant pole that sufficiently attenuates the high-frequency gain of the operational amplifier.

iii. **Distortion, and Other Effects**

Limited bandwidth also results in lower amounts of feedback at higher frequencies, producing higher distortion, and output impedance as the frequency increases.

Typical low-cost, general-purpose op-amps exhibit a GBWP of a few megahertz. Specialty and high-speed op-amps exist that can achieve a GBWP of hundreds of megahertz. For very high-frequency circuits, a current-feedback operational amplifier is often used.

iv. Noise

Amplifiers generate random voltage at the output even when there is no signal applied. This can be due to thermal noise and flicker noise of the devices. For applications with high gain or high bandwidth, noise becomes a very important consideration.

v. Input capacitance

Most important for high frequency operation because it reduces input impedance and may cause phase shifts.

vi. Power-supply rejection

With increasing frequency the power-supply rejection usually gets worse. So it can be important to keep the supply clean of higher frequency ripples and signals, e.g. by the use of bypass capacitors.

c) Non-linear imperfections

i. Saturation

a. Output voltage is limited to a minimum and maximum value close to the power supply voltages. The output of older op-amps can reach to within one or two volts of the supply rails. The output of newer so-called "rail to rail" op-amps can reach to within millivolts of the supply rails when providing low output currents.

ii. Slewing

The amplifier's output voltage reaches its maximum rate of change, the slew rate, usually specified in volts per microsecond. When slewing occurs, further increases in the input signal have no effect on the rate of change of the output. Slewing is usually caused by the input stage saturating; the result is a constant current i driving a capacitance C in the amplifier (especially those capacitances used to implement its frequency compensation); the slew rate is limited by $dv/dt=i/C$.

iii. Non-linear input-output relationship

The output voltage may not be accurately proportional to the difference between the input voltages. It is commonly called distortion when the input signal is a waveform. This effect will be very small in a practical circuit where substantial negative feedback is used.

iv. Phase reversal

In some integrated op-amps, when the published common mode voltage is violated (e.g., by one of the inputs being driven to one of the supply voltages), the output may slew to the opposite polarity from what is expected in normal operation.[6][7] Under such conditions, negative feedback becomes positive, likely causing the circuit to "lock up" in that state.

d) Power considerations

a) Limited output current

a. The output current must be finite. In practice, most op-amps are designed to limit the output current so as not to exceed a specified level – around 25 mA for a type 741 IC op-amp – thus protecting the op-amp and associated circuitry from damage. Modern designs are electronically more rugged than earlier implementations and some can sustain direct short circuits on their outputs without damage.

b) Output sink current

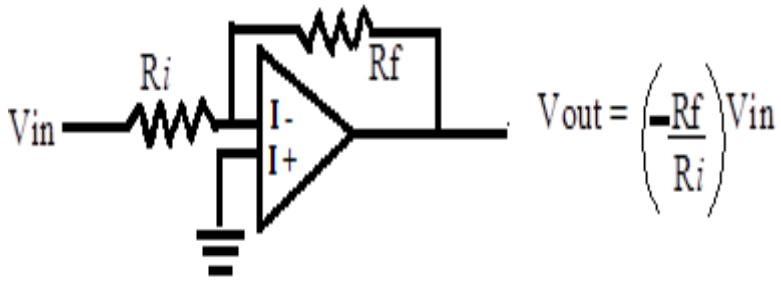
a. The output sink current is the maximum current allowed to sink into the output stage. Some manufacturers show the output voltage vs. the output sink current plot, which gives an idea of the output voltage when it is sinking current from another source into the output pin.

c) Limited dissipated power

a. The output current flows through the op-amp's internal output impedance, dissipating heat. If the op-amp dissipates too much power, then its temperature will increase above some safe limit. The op-amp may enter thermal shutdown, or it may be destroyed.

A. Inverting Amplifier

The inverting amplifier converts positive voltages on the inputs to a negative amplified voltages on the output and vice-versa.
The inverting amplifier is the simplest configuration for an op-amp.



$$I_- = I_+$$

$$I_{in} = \frac{V_{in}}{R_i} \qquad (Rule\,1)$$

$$V_{out} = -i_{in} R_f \qquad (Rule\,2)$$

$$= \frac{-V_{in} R_f}{R_i}$$

$$A = \frac{V_{out}}{V_{in}} = -\frac{R_f}{R_i}$$

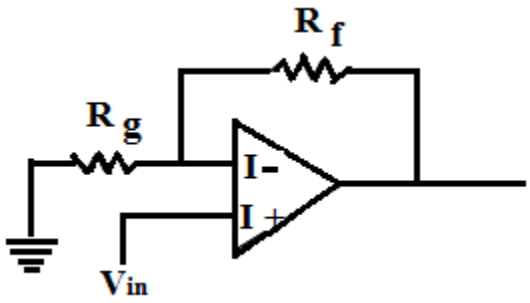
A variable gain amplifier can be created by replacing the feedback resistor, Rf, with a variable resistor.

Advantages and Disadvantages

The major advantage of the inverting amplifier is that it is very easy to select a particular gain and the gain will change linearly as we change R_f. There are two significant disadvantages, input impedance is low and a dual power supply is required. The input impedance of this circuit is approximately R_i. For normal components R_i is typically chosen to be a few kilo-ohms. This is not very high and can easily cause a loading problem for the sensor that is attached to it. The second problem is that this circuit also inverts all inputs, positive voltages become negative amplified voltages and vice-versa. In order to do this the amplifier must have a positive and negative voltage supply, typically +12 to -12V. This is not convenient as most modern circuits

are designned with a single positive supply. For these reasons the inverting op-amp configuration is not used very often in instrumentation applications. It is used in summing applications as will be shown later.

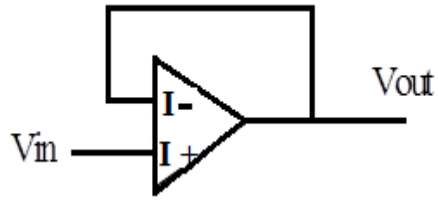
B. Non-Inverting



$$V_{out} = \left(1 + \frac{R_f}{R_g}\right) V_{in} \qquad , \qquad A = \frac{V_{out}}{V_{in}} = \left(1 + \frac{R_f}{R_g}\right)$$

Applications

Non-inverting amplifiers have very high input impedance and can be implemented with a single 0 to 5V supply. The gain can be controlled by replacingR_f with a variable resistor. Note that in this case the gain does not change linearly with changing R_f. A commonly used variation of this amplifier, called a follower, is as shown below.

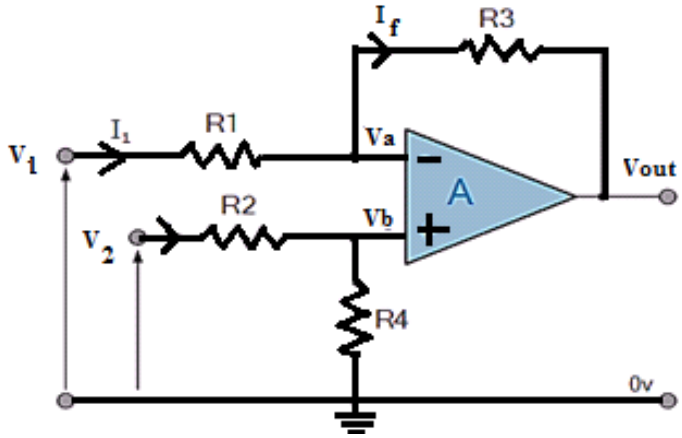


In this configuration Rf=0 and Rg=0, so the gain =1. The output of the amp simply follows the input, but the input impedance is very high. This is a commonly used circuit when you need to buffer the sensor from the rest of the system.

This amplifier can be used as shown but is often used as the input stage of a differential instrumentation amplifier.

2. Explain differential amplifier in detail. (Nov-15A)

Differential Input Amplifier



Output equation

By connecting each input in turn to 0V ground, **by superposition** to solve for the output voltage V_{out}.

$$I_1 = \frac{V_1 - V_a}{R_1}, \qquad I_2 = \frac{V_2 - V_b}{R_2}, \qquad I_f = \frac{V_a - (V_{out})}{R_3}$$

Summing point $V_a = V_b$

$$V_b = V_2\left(\frac{R_4}{R_2 + R_4}\right)$$

If $V_2 = 0$, then $\qquad V_{out(a)} = -V_1\left(\frac{R_3}{R_1}\right)$

If V_1=0, then: $V_{out(a)} = V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$

$$V_{out(a)} = V_{out(a)} + V_{out(b)}$$

$$V_{out} = -V_1\left(\frac{R_3}{R_1}\right) + V_2\left(\frac{R_4}{R_2 + R_4}\right)\left(\frac{R_1 + R_3}{R_1}\right)$$

When resistor, $R_1=R_2$ and $R_3=R_4 V_{out}$ can be simplified:-

$$V_{out} = \frac{R_3}{R_1}(V_2 - V_1)$$

This circuit can be analyzed by the ideal op-amp rules and the principle of superposition.

Set V_2 = 0 and the circuit becomes the equivalent of the Inverting Amplifier. (No current flows through I+ or the connected resistors so I+ is effectively at 0V.) (Rule 2)

Set V_1 = 0 (ground) and the circuit becomes equivalent to a non-inverting amplifier with the voltage at I+ given by

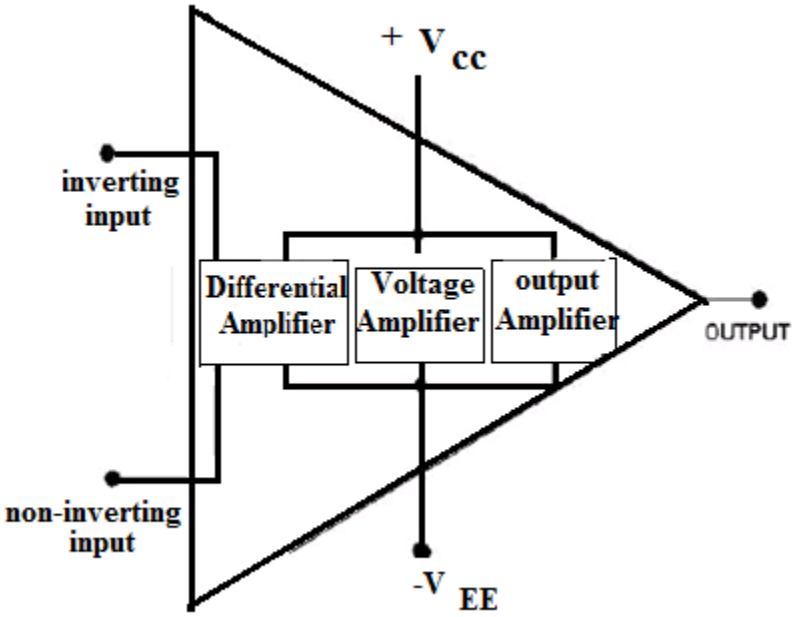
By superposition $V_{out(a)} = V_{out(a)} + V_{out(b)}$

Note that matching pairs of resistors R1 and R2 are needed for this simple equation to work. Vout can be calculated for other resistor values by adapting the above equations.

Applications of the differential amp

This circuit is the basis of the instrumentation amplifier. Non-inverting amplifiers are attached to each of the inputs. This ensures that the input impedance is very high. It is also possible to arrange these input stages so they share a common resistor Rg. This becomes the single resistor that controls the gain of the complete amplifier. All the other resistors and amplifiers are built onto a single chip where matched resistance pairs are easier to achieve and the entire amplifier gain is controlled from a single external resistor.

3. Draw the block diagram of operation amplifier and describe the various stage of block diagram. Also discuss the ideal characteristic of Op-amp. (7) (Nov-15)



a. The input stage is a differential amplifier. The differential amplifier used as an input stage providesdifferential inputs and a frequency response down to d.c. Special techniques are used to provide the highinput impedance necessary for the operational amplifier.

b. The second stage is a high-gain voltage amplifier. This stage may be made from several transistors toprovide high gain. A typical operational amplifier could have a voltage gain of 200,000. Most of this gaincomes from the voltage amplifier stage.

c. The final stage of the OP AMP is an output amplifier. The output amplifier provides low outputimpedance. The actual circuit used could be an emitter follower. The output stage should allow theoperational amplifier to deliver several milliamperes to a load.

- Notice that the operational amplifier has a positive power supply ($+V_{CC}$) and a negative powersupply ($-V_{EE}$). This arrangement enables the operational amplifier to produce either a positive or anegative output.The two input terminals are labeled "inverting input" (-) and "noninverting input" (+).
- Theoperational amplifier can be used with three different input conditions (modes). With differential inputs(first mode), both input terminals are used and two input signals which are 180 degrees out of phase witheach other are used.
- This produces an output signal that is in phase with the signal on the noninvertinginput. If the noninverting input is grounded and a signal is applied to the inverting input (second mode),the output signal will be 180 degrees out of phase with the input signal (and one-half the amplitude of thefirst mode output).

- If the inverting input is grounded and a signal is applied to the noninverting input(third mode), the output signal will be in phase with the input signal (and one-half the amplitude of thefirst mode output).

4. Draw the explain Half-wave rectifier and full wave rectifier using operation amplifier. (April-14)

Basic circuit of Precision Half Wave Rectifier using op-amp

A half wave rectifier using OP amp is also known as a Precision rectifier or super diode, is a configuration obtained with an operational amplifier in order to have a circuit behaving like an ideal diode and rectifier.

Figure 1 shows the circuit of a Precision rectifier .On positive voltage swings the diode conducts and a voltage is developed across the resistor. On negative swings, the diode turns off and the output voltage is zero (no current through the resistor).

The basic idea behind the superdiode is to use the high-gain of an op-amp to mask the finite turn-on voltage (and other nonlinearities) of the diode. This is done by placing it in the negative feedback path as shown in fig 1. Any positive voltage at the op-amp â€œ+â€• terminal is now sufficient to turn on the diode, and the negative feedback regulates the current through the load resistor to maintain an output voltage equal to the input voltage for these positive input voltages. For positive signals the circuit is a unity-gain buffer(fig 2). For negative signals, the output goes negative, and the diode turns off (fig 3).

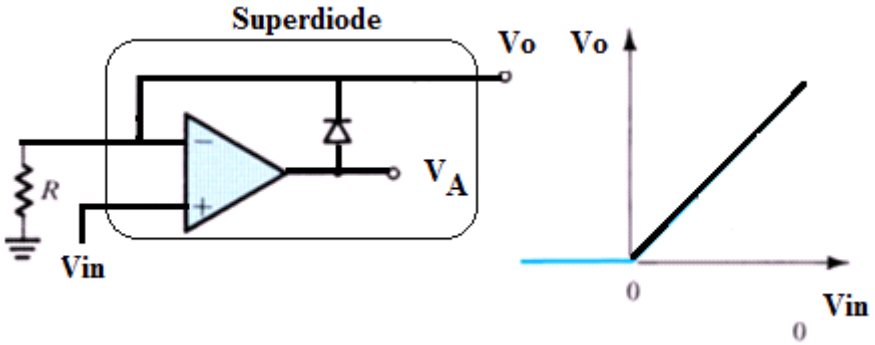


Fig 1. Circuit diagram of a precision rectifier and its input output relation.

When Diode is conducting: The feedback loop is closed, and the circuit looks like the buffer with small drop across diode. And Vo=Vin.

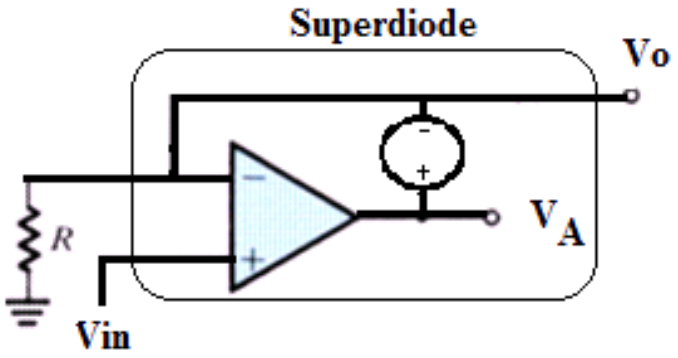


Fig 2. The circuit behaves as a buffer for positive input voltages.

When Diode is not conducting: : i.e. Vi<0 And Vo = 0V.

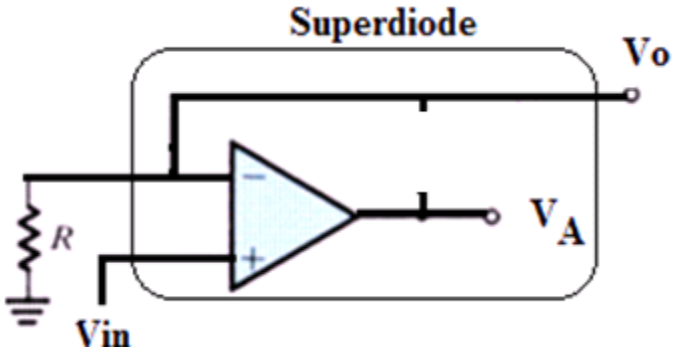


Fig 3. The diode acts as an open circuit for negative value of voltages.

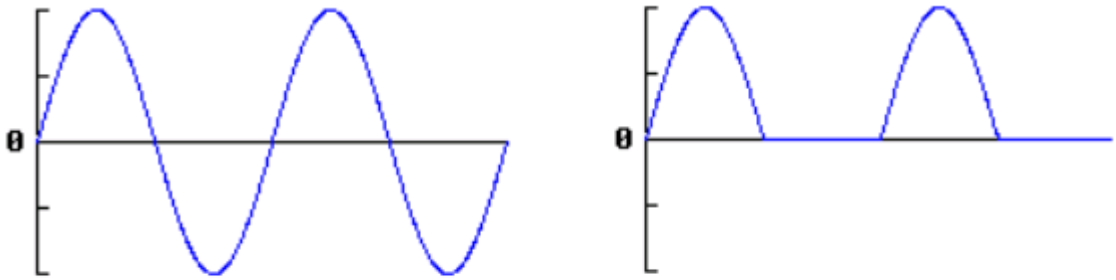


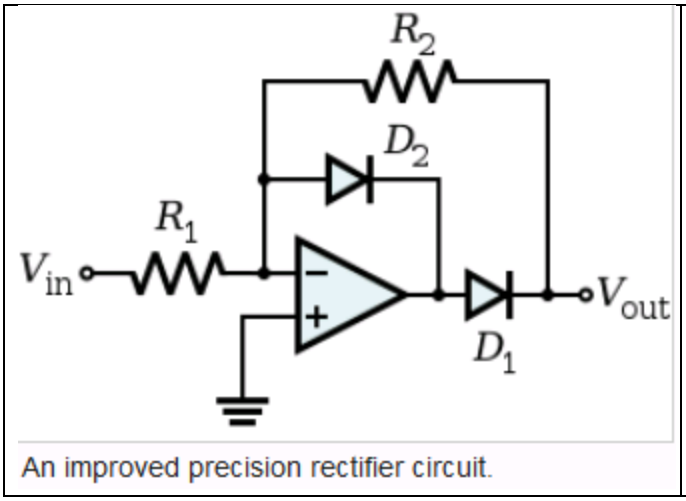
Fig 4. Input(a) and output (b) of a rectifier circuit.

Improved circuitof Half Wave Rectifier using op-amp

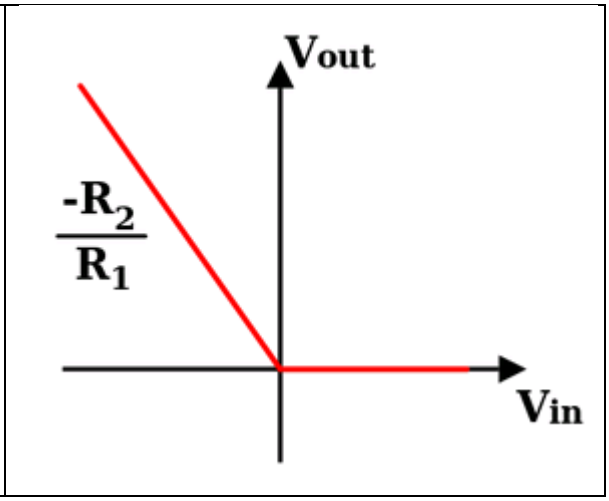
An alternative version is given on the right.

In this case, when the input is greater than zero, D1 is OFF and D2 is ON, so the output is zero because one side of is connected to the virtual ground, and there is no current through it. When

the input is less than zero, D1 is ON and D2 is OFF, and the output is like the input with an amplification of $-R_2/R_1$. Its input-output relationship is the following:

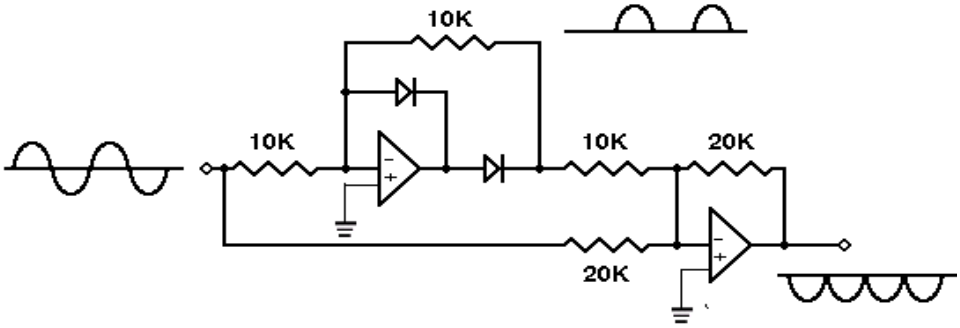


An improved precision rectifier circuit.



This circuit has the benefit that the op-amp never goes into saturation, but its output must change by two diode voltage drops (about 1.2 V) each time the input signal crosses zero. Hence, the slew rate of the operational amplifier, and its frequency response (gain-bandwidth product) will limit high frequency performance - especially for low signal levels - although an error of less than 1% at 100 kHz is possible.

Precision Full Wave Rectifier using op-amp



The circuit shown above performs full-wave rectification on the input signal, as shown. For positive instead of negative wave, simply reverse the two diodes in the half-wave rectifier section.

The full-wave rectifier depends on the fact that both the half-wave rectifier and the summing amplifier are precision circuits. It operates by producing an inverted half-wave-rectified signal and then adding that signal at double amplitude to the original signal in the summing amplifier. The result is a reversal of the selected polarity of the input signal.

The resistor values shown are reasonable; the resistors themselves must be of high precision in order to keep the rectification process accurate.

5. Explain how the op-amp can be used as a summing amplifier.(5) (Nov-15A)

This is an amplifier structure which is essentially a multiple version of the Inverting Amplifier, having several inputs as shown in Fig. Each input is connected via a corresponding resistor to the inverting input terminal of the op-amp. Since this input is considered to have a very high input resistance, it can be assumed that no current flows into the inverting input. This means that, applying Kirchoff's Current Law, all of the input currents from the sources, I_1 , I_2 and I_3 must combine at the inverting input terminal to flow out of this node through the feedback resistor, R_f . In this case the inverting input terminal of the op-amp is referred to as a current-summing node. It can still also be considered as a virtual earth, since $V_e \rightarrow 0V$ and the non-inverting input terminal is connected to ground.

Then:

$$I_f = I_1 + I_2 + I_3$$

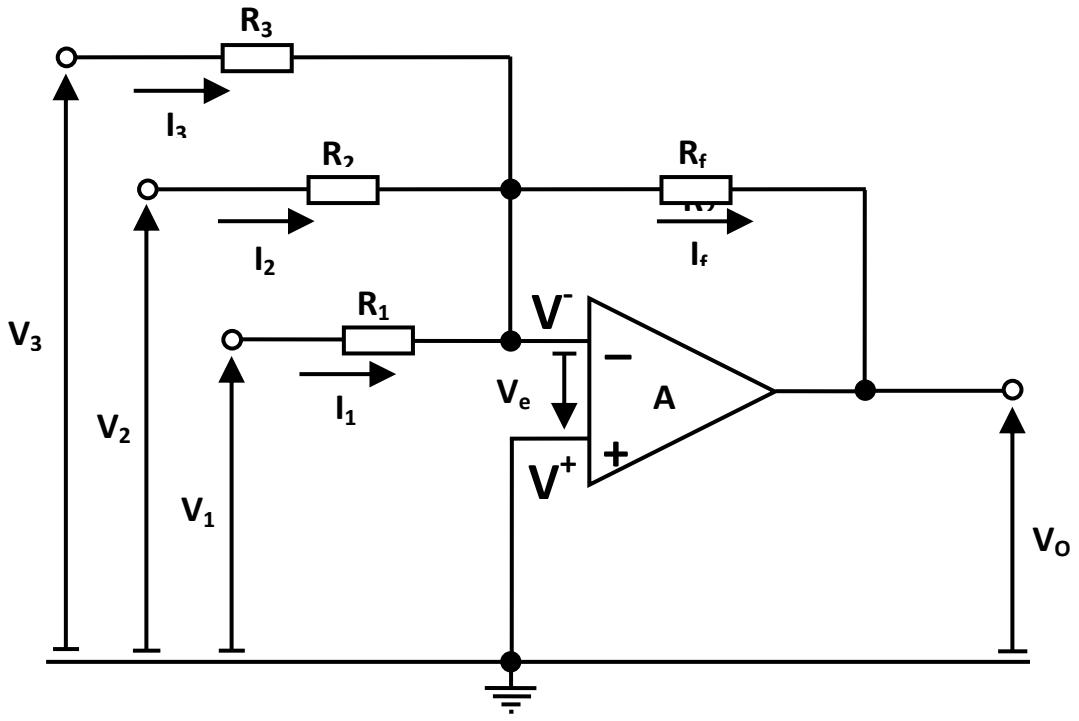


Fig. Schematic Diagram of the Inverting Summing Amplifier

so that:

$$\frac{V^- - V_O}{R_f} = \frac{V_1 - V^-}{R_1} + \frac{V_2 - V^-}{R_2} + \frac{V_3 - V^-}{R_3}$$

But since $V^- \rightarrow 0V$ then:

$$\frac{-V_O}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}$$

So that

$$V_O = -\left[\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right]$$

This shows that this circuit structure essentially adds or sums the input source voltages V_1 , V_2 and V_3. The overall output is inverted but this can easily be corrected by following this stage with a single inverting amplifier stage having unity gain. Each input source voltage is scaled by a coefficient which is determined by the associated input resistor so that individual input voltages can be scaled by different factors.

6. Explain the operation of instrumentation amplifier. (April-15)

Instrumentaion amplifier:

Basically it is a difference amplifier. It is employed to control the industrial parameters like pressure; temperature etc. A transducer converts these parameters into equivalent electrical voltage. This is then applied to the instrumentation amplifier, which boosts the signal level to drive the display devices.

An instrumentation amplifier must meet the following requirements.

(i)Low-level signal amplification:

The instrumentation amplifiers should amplify signals of very small amplitude. Hence they should have very high gain. Also, the gain should be stable.

(ii)Low noise:

As the signals involved are very weak, the instrumentation amplifiers must contribute minimum noise, otherwise, it may interfere with the signals. The instrumentation amplifier beng a differential amplifier they are capable of rejecting the noise common to both the inputs.

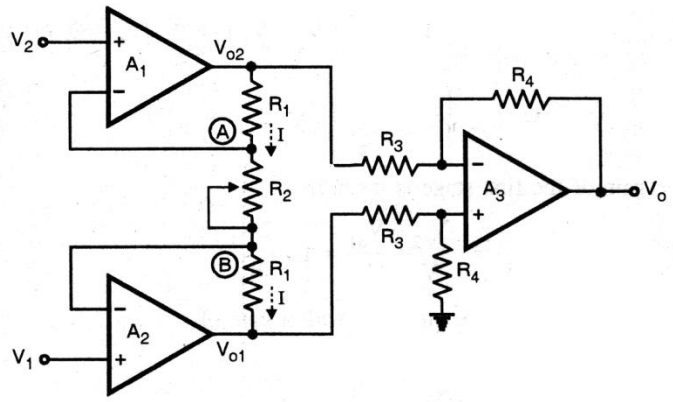
(iii)Low thermal drift.

The environment in which the instrumentation amplifiers are employed may have lot of temperature fluctuations. Hence the parameters of these amplifiers must be thermally stable.

(iv) High input impedance:

To avoid loading effect on the input source, the instrumentation amplifiers must have high input impedance.

THREE OPAMP INSTRUMENTATION AMPLIFIERS:



The three OP-AMP instrumentation amplifier

This is a high impedance amplifier using cross-coupled difference amplifiers. A_1&A_2 in the above figure are non-inverting amplifiers. As all the OPAMPS are assumed to have infinite Z_i ,theiri/p current is zero.

EXPRESSION FOR VOLTAGE GAIN:

From the above figure, we can write

$V_A = V_2 \;\&\; V_B = V_1$

$\therefore \qquad I = \dfrac{V_A - V_B}{R_2}$ ---------- (1)

But $V_A = V_2 \;\&\; V_B = V_1$

$\therefore I = \dfrac{V_2 - V_1}{R_2}$ ---------- **(2)**

But $V_1 = V_{01} \;\&\; V_2 = V_{02}$ Since A_1&A_2 are unity gain amplifiers.

$-I = \dfrac{V_1 - V_2}{R_2} = \dfrac{V_{01} - V_1}{R_1} = \dfrac{V_2 - V_{02}}{R_1}$ ---------- (3)

$\dfrac{V_{01}}{R_1} = \dfrac{V_1}{R_1} + \dfrac{V_1}{R_2} - \dfrac{V_2}{R_2} = \left[\dfrac{1}{R_1} + \dfrac{1}{R_2}\right]V_1 - \dfrac{V_2}{R_2}$ ----- (4)

$V_{01} = \left[1 + \dfrac{R_1}{R_2}\right]V_1 - \dfrac{R_1}{R_2}V_2$ ---------- (5)

Similarly,

$\dfrac{V_{02}}{R_1} = \dfrac{V_2}{R_1} - \dfrac{V_1}{R_2} + \dfrac{V_2}{R_2} = -\dfrac{V_1}{R_2} + \left[\dfrac{1}{R_1} + \dfrac{1}{R_2}\right]V_2$

$\therefore V_{02} = -\dfrac{R_1}{R_2}V_1 + \left[1 + \dfrac{R_1}{R_2}\right]V_2$ ---------- (6)

Output voltage of the first stage is

$V_{02} - V_{01} = -\dfrac{R_1}{R_2}V_1 + \left[1 + \dfrac{R_1}{R_2}\right]V_2 - \left[1 + \dfrac{R_1}{R_2}\right]V_1 + \dfrac{R_1}{R_2}V_2 = \left[1 + \dfrac{2R_1}{R_2}\right](V_2 - V_1)$ ----------(7)

Gain of the first stage

$A_{V1} = \dfrac{V_{02} - V_{O1}}{V_2 - V_1} = 1 + \dfrac{2R_1}{R_2}$ ---------- (8)

Second stage is a differential amplifier with a gain of

$A_{V2} = \dfrac{R_4}{R_3}$ ---------- (9)

Overall gain of the instrumentation amplifier is

$A_V = A_{V1} \times A_{V2} = \left(1 + \dfrac{2R_1}{R_2}\right) \times \dfrac{R_4}{R_3}$ ---------- (10)

Hence by varying R_2, the overall gain can be linearly varied.

Output voltage, $V_0 = A_V \times (V_1 - V_2)$ ---------- (11)

Advantages of instrumentation amplifiers:

The gain can be adjusted precisely by varying a single resistor.
Input impedance is very high as it depends on two unity gain buffers A_1&A_2
This circuit can reject any common mode signals such as noise due to high CMRR of the three amplifier stages A_1, A_2, &A_3.

P1. Calculate the gain of the configuration shown below.

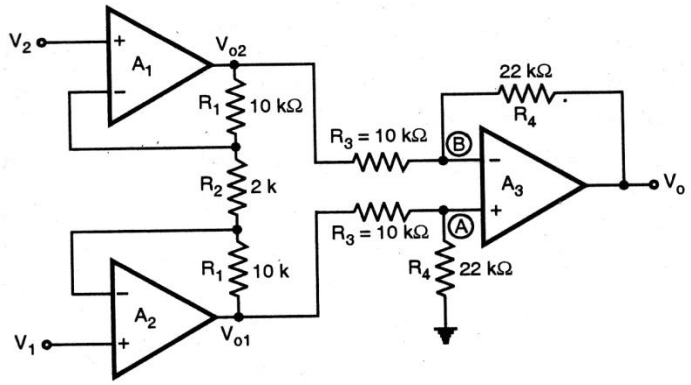


Fig. P. 10.3.1

SOLN: Overall gain of this circuit is

$$A_V = \left[1 + \frac{2R_1}{R_2}\right] \times \frac{R_4}{R_3}$$

Substituting the given values,

$$A_V = \left[1 + \frac{2 \times 10}{2}\right] \times \frac{22}{10} = 292$$

P2. For the instrumentation amplifier of p1 above, calculate the output voltage if
V_1 = 2mV & V_2 = 1mV.

SOLN: (i) Referring to above fig, output amplifier A_1 is

$$V_{02} = -\frac{R_1}{R_2} \times V_1 + \left[1 + \frac{R_1}{R_2}\right] V_2$$

Substituting the different values

$$V_{02} = -\frac{10}{2} \times 2mV + \left[1 + \frac{10}{2}\right] \times 1mV = -4mV \quad \text{---------- (1)}$$

(ii) Again from the above figure,

$$V_{01} = \left[1 + \frac{R_1}{R_2}\right] V_1 - \frac{R_1}{R_2} V_2$$

Substituting the values,

$$V_{01} = \left[1 + \frac{10}{2}\right] \times 2mV - \frac{10}{2} \times 1mV = 7mV$$

(iii) V_{01}&V_{02} are the inputs to the difference amplifier A_3.Output voltage can be calculated using superposition theorem.

(a)Assume V_{02} = 0 & calculate the output V_0' only

$$V_0' = \left[1 + \frac{R_4}{R_3}\right] \times \left[\frac{R_4}{R_3 + R_4}\right] V_{01} = \left[1 + \frac{22}{10}\right] \times \left[\frac{22}{10 + 22}\right] \times 7mV = 15.4mV.$$

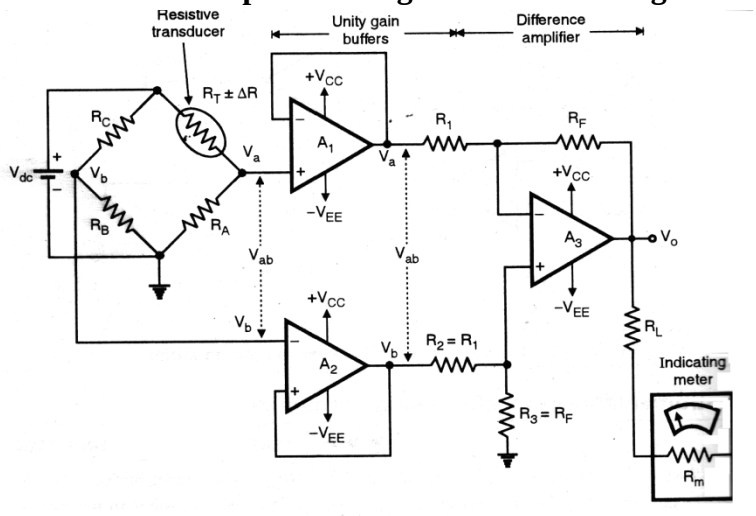
(b) Assume V_{01} = 0 & calculate the output V_0''due to V_{02} only.

$$V_0'' = -\frac{R_4}{R_3} \times V_{02} = -\frac{22}{10} \times (-4mV) = 8.8mV)$$

(iv) Total output voltage,

$$V_0 = V_0' + V_0'' = 15.4 + 8.8 = 29.2mV$$

Instrumentation Amplifier Using Transducer Bridge:



Differential instrumentation amplifier using a transducer bridge

Above figure shows a differential instrumentation amplifier using a transducer bridge. Resistance R_T is a resistance of which changes proportional with some physical quantity

Such as temperature, pressure, light intensity etc. R_T is the resistance of the transducer & ΔR is the change in the resistance R_T.

A DC or AC voltage source can excite the bridge. Under balanced conditions

$V_a = V_b$ ---------- (1)

But $V_a = \frac{R_A}{R_A + R_T} \times V_{dc}$

$V_b = \frac{R_B}{R_B + R_C} \times V_{dc}$

$\therefore \frac{R_A}{(R_A + R_T)} V_{dc} = \frac{R_B}{(R_B + R_C)} \times V_{dc}$

$R_A R_B + R_A R_C = R_A R_B + R_B R_T$

$\therefore R_A R_C = R_B R_T$

$\frac{R_C}{R_B} = \frac{R_T}{R_A}$ ---------- (2)

(Under balanced condition)

The values of R_A,R_B& R_C are such that they are equal to R_T at a particular value of the physical quantity being measured. This value is decided by the designer depending on the transducer characteristics.

7. Draw and explain the circuit of a voltage to current converter if the load is (April-14)

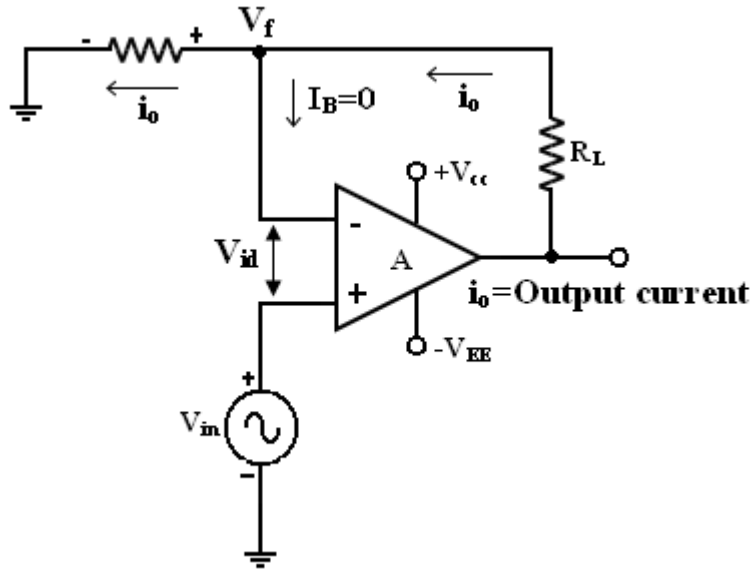
a) Floating

b) Grounded

Explain how the op-amp can be used as voltage to current converter.(6) (Nov-15A),

a) Voltage to Current Converter with floating loads (V/I):

1. Voltage to current converter in which load resistor R_L is floating (not connected to ground).
2. Vin is applied to the non inverting input terminal, and the feedback voltage across R_1 devices the inverting input terminal.
3. This circuit is also called as a current – series negative feedback amplifier.
4. Because the feedback voltage across R_1 (applied Non-inverting terminal) depends on the output current i_0 and is in series with the input difference voltage V_{id}.



Writing KVL for the input loop,

$$Vin = V_{id} + V_f$$

$$Vin = V_f$$

$$Vin = R_1 i_0$$

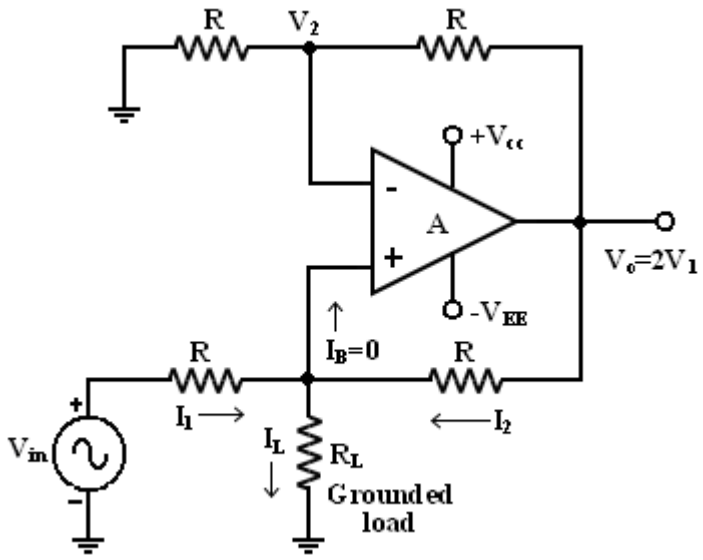
From the fig input voltage Vin is converted into output current of Vin/R_1 [Vin ->i_0] . In other words, input volt appears across R_1. If R_1 is a precision resistor, the output current ($i_0 = Vin/R_1$) will be precisely fixed.

Applications:

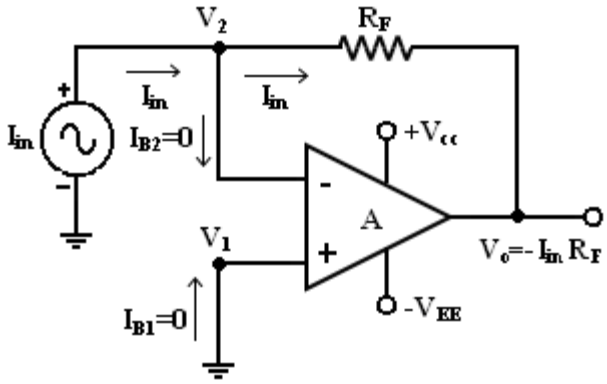
1. Low voltage ac and dc voltmeters
2. Diode match finders
3. LED
4. Zener diode testers.

b) Voltage – to current converter with Grounded load:

This is the other type V – I converter, in which one terminal of the load is connected to ground.



c) Current to Voltage Converter (I –V):



1. Open – loop gain a of the op-amp is very large.
2. Input impedance of the op-amp is very high. (i.e) the currents entering into the 2 input terminals is very small. $I_{B_1} = I_{B_2} = 0$ ---(2)
3. Gain of the inv-amp is given by

$V_1 = 0$ as the non-inve(+) terminal is connected to ground. $V_2 = 0$.

Thus the inv –terminal (-) also is at ground and the entire input volt appears across R_1 .

$I_{in} = Vin/R_1$ -----(3)

$V_{in} = Iin /R_1$

Sensitivity of the I – V converter:

1. The output voltage $V_0 = -R_F I_{in}$.

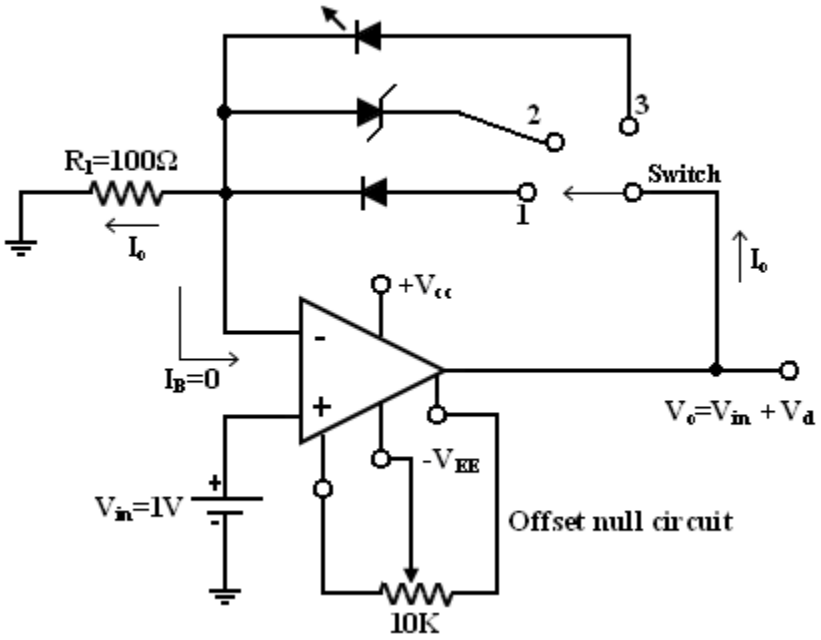
2. Hence the gain of this converter is equal to $-R_F$. The magnitude of the gain (i.e) is also called as sensitivity of I to V converter.

3. The amount of change in output volt ΔV_0 for a given change in the input current ΔIin is decide by the sensitivity of I-V converter.

4. By keeping R_F variable, it is possible to vary the sensitivity as per the requirements.

Applications of V-I converter with Floating Load:

1. Diode Match finder:



In some applications, it is necessary to have matched diodes with equal voltage drops at a particular value of diode current. The circuit can be used in finding matched diodes and is obtained from fig (V-I converter with floating load) by replacing R_L with a diode. When the switch is in position 1: (Diode Match Finder) Rectifierr diode (IN 4001) is placed in the f/b loop, the current through this loop is set by input voltage Vin and Resistor R_1 . For Vin = 1V and $R_1 = 100\Omega$, the current through this

$I_0 = Vin/R_1 = 1/100 = 10mA$.

As long as V_0 and R_1 constant, I_0 will be constant. The Voltage drop across the diode can be found either by measuring the volt across it or o/p voltage. The output voltage is equal to (Vin + V_D) V_0 = Vin + V_D . To avoid an error in output voltage the op-amp should be initially nulled. Thus the matched diodes can be found by connecting diodes one after another in the feedback path and measuring voltage across them.

2. Zener diode Tester:

(When the switch position 2)

when the switch is in position 2, the circuit becomes a zener diode tester. The circuit can be used to find the breakdown voltage of zener diodes. The zener current is set at a constant value by

Vinand R_1. If this current is larger than the knee current (I_{ZK}) of the zener, the zenerr blocks (V_z) volts.

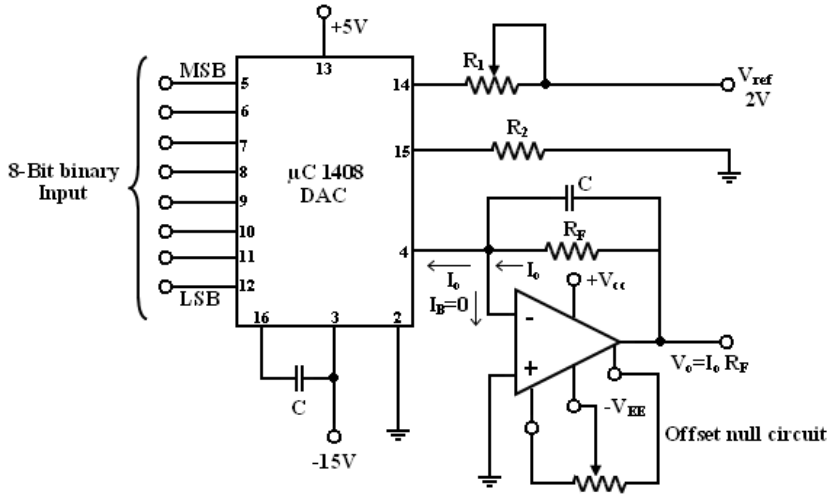
For Ex:

I_{ZK} = 1mA , V_Z = 6.2V, Vin = 1v , R_1 = 100Ω Since the current through the zener is , I_0 = Vin/R_1 = 1/100 =10mA > I_{ZK} the voltage across the zener will be approximately equal to 6.2V.

3. When the switch is in position 3: (LED)

The circuit becomes a LED when the switch is in position 3. LED current is set at a constant value by Vin and R_1. LEDs can be tested for brightness one after another at this current. Matched LEDs with equal brightness at a specific value of current are useful as indicates and display devices in digital applications.

Applications of I – V Converter:



One of the most common use of the current to voltage converter is

a)Digital to analog Converter (DAC)

b) Sensing current through Photodetector. Such as photocell, photodiodes and photovoltaic cells.

Photoconductive devices produce a current that is proportional to an incident energy or light (i.e) It can be used to detect the light.

a) DAC using I – V converter:

It shows a combination of a DAC and current to voltage converter. The 8 digit binary signal is the input to the DAC and V_0 is the corresponding analog output of the current to voltage converter. The outputu of the DAC is current I_0, the value of which depends on the logic state (0 or 1), of the binary inputs as indicated by the following eqn.

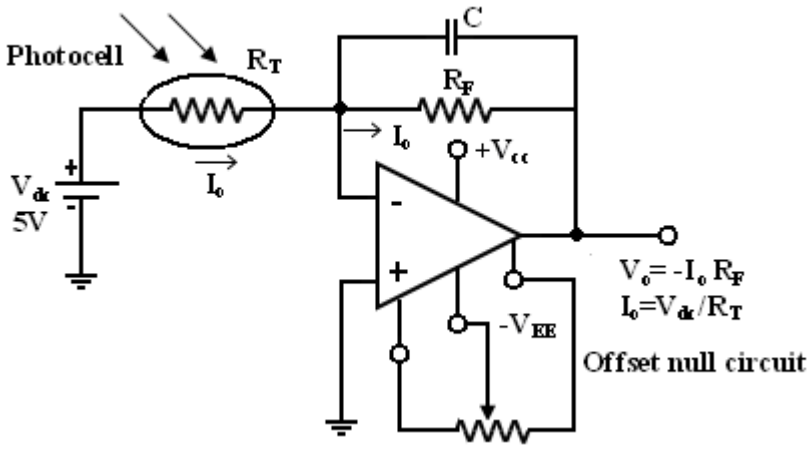
This means I_0 is zero when all inputs are logic 0.

I_0 is max when all inputs are logic 1.

The variations in I_0 can be converted into a desired o/p voltage range by selecting a proper value for R_F. since, $V_0 = I_0 R_F$

Where I_0 is given by eqn (1). It is common to parallel R_F with capacitance C to minimize the overshoot. In the fig the o/p voltage of the current to voltage converter is positive because the direction of input current I_0 is opposite to that in the basic I – V Converter.

b) Detecting current through photosensitive devices:

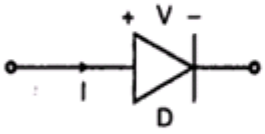


Photocells, photodiodes, photovoltaic cells give an output curren that depends on the intensity of light and independent of the load. The current through this devices can be converted to voltage by I – V converter and it can be used as a measure of the amount of light. In this fig photocell is connected to the I – V Converter. Photocell is a passive transducer, it requires an external dc voltage(Vdc). The dc voltage can be eliminated if a photovoltaic cell is used instead of a photocell. The Photovoltaic Cell is a semiconductor device that converts the radiant energy to electrical power. It is a self generating circuit because it doesnot require dc voltage externally. Ex of Photovoltaic Cell : used in space applications and watches.

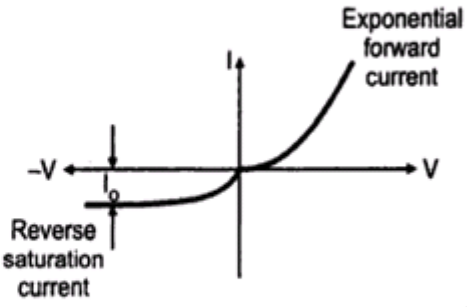
8. Explain in detail, the working of Log and antilog amplifier.(8) (Nov-13), Explain in details about working of log and Antilog Amplifiers. (Dec-14)

Fundamentals of Log Amplifiers:

Consider a diode as shown in the Fig. and the corresponding volt-ampere (V-I) characteristics in the Fig.



(a) Diode



(b) V-I Characteristics

The basic volt-ampere relationship for a diode is given as,

$$I = I_o \left(e^{V/\eta V_T} - 1\right) \quad \ldots (1)$$

where I = diode current

I_o = reverse saturation current

V = diode voltage

η = 1 for Ge diode, 2 for Si diode

V_T = kT = voltage equivalent of temperature

and k = Boltzmann's constant = 8.62×10^{-5} eV/°K

T = temperature in °K

It can be observed that at room temperature of 27°C i.e. T = 300°K, the voltage equivalent of temperature is,

$$V_T = 0.02586 \text{ V} = 26 \text{ mV at } 300°K$$

This value is frequently used in the diode circuits.

It can be seen from the V-I characteristics shown in the Fig. (b) that for a forward biased condition, the diode voltage V is positive and the exponential term $e^{V/\eta V_T}$ has a positive index. Hence we can say that $1 << e^{V/\eta V_T}$ and can be neglected. The corresponding diode current is its forward current I_f.

$$\therefore \quad I_f = I_o e^{V / \eta V_T} \quad \ldots (2)$$

This indicates that the forward current increases exponentially with respect to the bias voltage V.

Taking natural logarithm of both sides,

$$ln [I_f] = ln [I_o e^{V / \eta V_T}] \quad \ldots (3)$$

$$\therefore \quad ln [I_f] = ln [I_o] + ln [e^{V / \eta V_T}] \quad \ldots (4)$$

$$\therefore \quad ln [I_f] = ln [I_o] + \frac{V}{\eta V_T} \quad \ldots (5)$$

$$\therefore \quad V = \eta V_T [ln (I_f) - ln (I_o)] \quad \ldots (6)$$

This equation (6) is the basic equation used in Log and Antilog amplifiers.

The equation (6) can be expressed as,

$$V = \eta V_T ln \left[\frac{I_f}{I_o}\right] \quad \ldots (7)$$

Similar to the diode, the equation for the collector current in BJT can be written as,

$$I_C = \alpha I_s (e^{V_{BE} / V_T} - 1) \quad \ldots (8)$$

where I_C = collector current

I_s = emitter saturation current

V_{BE} = base emitter voltage

$\alpha \approx 1$ and constant

$$\therefore \quad \frac{I_C}{I_s} = e^{V_{BE} / V_T} - 1 \quad \ldots (9)$$

Now emitter saturation current is very small of the order of 10^{-13} A.

$$\therefore \quad e^{V_{BE} / V_T} = \frac{I_C}{I_s} + 1 = \frac{I_C}{I_s} \quad \ldots (10)$$

As I_s is very small, $1 << (I_C / I_s)$.

$$\ln (e^{V_{BE} / V_T}) = ln \left(\frac{I_C}{I_s}\right) \quad \ldots (11)$$

$$\therefore \quad \frac{V_{BE}}{V_T} = ln\left(\frac{I_C}{I_s}\right) \qquad \ldots (12)$$

$$\therefore \quad \boxed{V_{BE} = V_T\, ln\left(\frac{I_C}{I_s}\right)} \qquad \ldots (13)$$

This equation forms the basis of Log and Antilog amplifier circuits where BJT is used instead of a diode.

In the equation (8), V_{BE} represents voltage across transistor, similar to the V in the equation (1), representing voltage across diode.

Now voltage across BJT is actually $V_{CB} + V_{BE}$. But in op-amp circuits when BJT is used in the feedback path as a diode, V_{CB} voltage becomes zero. Hence V is replaced by V_{BE} while writing the equation for the BJT.

For BJT used as a diode, $V_{CB} = 0$.

Basic Logarithmic Amplifier:

With the background of diode and current equations, let us study the basic logarithmic amplifier circuit using op-amp. The fundamental log amplifier is formed by placing a diode or a transistor in the negative feedback path of the op-amp.

Basic Log Amplifier Using Diode:

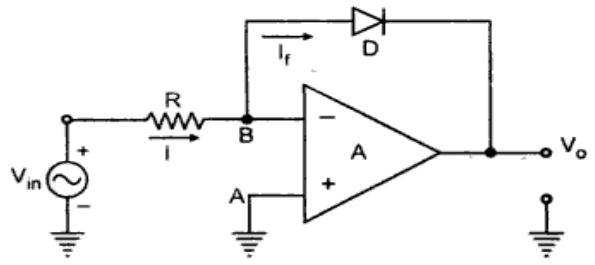
The circuit diagram of basic log amplifier using a diode is shown in the Fig.

The diode D is used in the negative feedback path. The node A is grounded hence node B is at virtual ground. Hence $V_B = 0$.

$$\therefore \quad I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R} \qquad \ldots (1)$$

Figure

Basic log amplifier



As the op-amp input current is zero,

$I = I_f$ = diode current ... (2)

Now I_f is the current through diode and voltage across diode is $V_B - V_o$ i.e. $-V_o$.

Hence using equation (7) we can write,

$$-V_o = \eta V_T\, ln\left[\frac{I_f}{I_o}\right] \qquad \ldots (3)$$

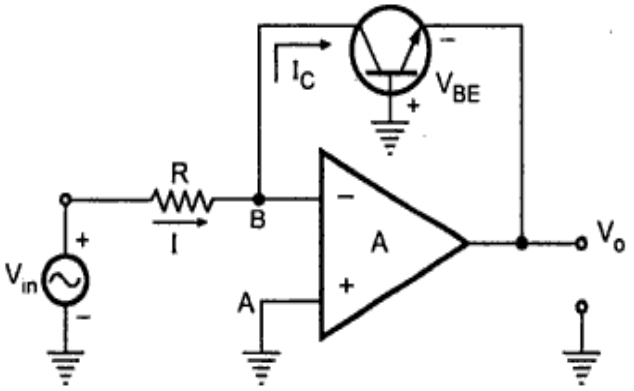
substituting $I_f = I = \frac{V_{in}}{R}$

$$\therefore \quad V_o = -\eta V_T\, ln\left[\frac{V_{in}}{R\, I_o}\right] \qquad \ldots (4)$$

As I_o R is constant d.c. voltage, let us denote it as V_{ref}.

Basic Log Amplifier Using Transistor:

The basic log amplifier can be obtained by using a transistor as a diode in the negative feedback path of an op-amp, as shown in the Fig.



Basic log amplifier

The node B is at virtual ground hence $V_B = 0$.

$$\therefore I = \frac{V_{in} - V_B}{R} = \frac{V_{in}}{R} \quad \ldots (7)$$

As the op-amp input current is zero

$$I = I_C = \text{collector current} \quad \ldots (8)$$

The voltage $V_{CB} = 0$ as the collector is at virtual ground and base is grounded. Hence we can write the equation of I_C as,

$$V_{BE} = V_T \, ln\left(\frac{I_C}{I_s}\right) \quad \ldots (9)$$

Applying to the output side we get,

$$V_o + V_{BE} = 0 \quad \ldots (10)$$

$$\therefore \quad V_{BE} = -V_o \quad \ldots (11)$$

and $$I_C = I = \frac{V_{in}}{R}$$

substituting in the equation (9),

$$-V_o = V_T \, ln\left(\frac{V_{in}}{R\, I_s}\right) \quad \ldots (12)$$

Let $$V_{ref} = R\, I_s,$$

$$\therefore \quad \boxed{V_o = -V_T \ln\left[\frac{V_{in}}{V_{ref}}\right]} \qquad \ldots (13)$$

The equation is similar to the equation (5) of section **1.3** , which gives the output, proportional to the logarithm of the input voltage V_{in}.

Disadvantages of Basic Circuit:

Hence it is very difficult to set the term V_{ref} for the circuit.

The term V_T which is kT also changes with temperature, which appears in both the equations.

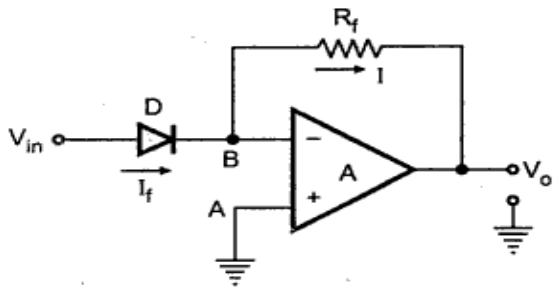
Thus temperature affects the performance and accuracy of the basic logarithmic amplifier circuit. Hence it is must to provide some sort of temperature compensation to reduce the errors.

Antilog Amplifier:

The log amplifier can easily be turned around to provide the antilog or exponential function which is called antilog amplifier. The basic antilog amplifier can be obtained by using a diode or a transistor.

Basic Antilog Amplifier Using Diode:

The circuit diagram of basic antilog amplifier using diode is shown in the Fig.



Basic antilog amplifier

The positions of diode and resistance are exchanged as compared to log amplifier circuit. The node A is grounded and hence node B is at virtual ground. Hence $V_B = 0$.

Now the current flowing through the diode is I_f and the voltage across diode is V_{in} itself, as B is at virtual ground. Hence from the diode current equation we can write,

$$I_f = I_o \, e^{V_{in}/\eta V_T} \qquad \ldots (1)$$

As op-amp input current is zero, the current I must be same as I_f.

$$\therefore \quad I = I_f = \frac{V_B - V_o}{R_f} = \frac{-V_o}{R_f} \quad \ldots (2)$$

$$\therefore \quad \frac{-V_o}{R_f} = I_o \, e^{V_{in}/\eta V_T}$$

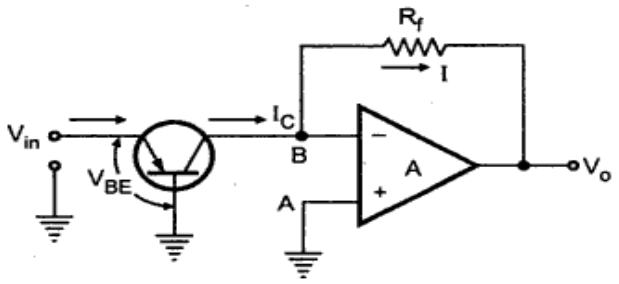
$$\therefore \quad V_o = -(I_o \, R_f) \, e^{V_{in}/\eta V_T} \quad \ldots (3)$$

The product $I_o \, R_f$ can be assumed to be V_{ref}, so we get,

$$\therefore \quad \boxed{V_o = -V_{ref} \, e^{V_{in}/\eta V_T}} \quad \ldots (4)$$

Thus the output voltage is proportional to the exponential function of V_{in}. The exponential function is nothing but the antilog and thus circuit works as an antilog amplifier.

Basic Antilog Amplifier Using Transistor:



Basic antilog amplifier

The same circuit providing antilog of the input can be obtained by using a transistor instead of a diode. This is shown in the Fig.

The node B is at virtual ground hence $V_B = 0$. Thus both collector and base of the transistor are at ground potential and $V_{CB} = 0$. Hence the voltage across the transistor is V_{BE} and we can write the expression for its collector current as,

$$I_C = I_s \, e^{V_{BE}/V_T} \quad \ldots (5)$$

But as seen from the Fig. , $V_{BE} = V_{in}$

$$\therefore \quad I_C = I_s \, e^{V_{in}/V_T} \quad \ldots (6)$$

Now the current I_C and current I are same as op-amp input current is zero.

$$\therefore \quad I = I_C \doteq \frac{V_B - V_o}{R_f} = \frac{-V_o}{R_f} \quad \ldots (7)$$

$$\therefore \quad \frac{-V_o}{R_f} = I_s\, e^{V_{in}/V_T}$$

$$\therefore \quad V_o = -I_s\, R_f\, e^{V_{in}/V_T} \qquad \ldots (8)$$

Assuming $I_s\, R_f$ as V_{ref}, we can write

$$\therefore \quad \boxed{V_o = -V_{ref}\, e^{V_{in}/\eta V_T}} \qquad \ldots (9)$$

Thus the output voltage is proportional to the exponential of V_{in} i.e. antilog of V_{in}. Thus circuit works as basic antilog amplifier.

In both the above circuits, it can be seen that the terms I_o, I_s and V_T are present in the output equation. All these are the function of temperature. Hence as temperature changes, these parameters also change and cause serious errors at the output. So the basic antilog circuits also face the same limitations as that of basic log amplifier circuits. And hence temperature compensation is must for the antilog amplifier circuits as well.

IIIANALOG IC APPLICATIONS

Series op-amp regulator – IC voltage regulator – Switching regulator – Digital to analog converters–specifications–weightedresistortype– R-2Rladdertype – Analogto digital converter – specifications–counterramp,flash,successiveapproximation,dualslope types – Voltageto frequencyconverter–Frequencyto voltage converter– Analog multiplier.

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2 marks

1. **Define switching regulator. (April-14)**

   Switching regulators are those which operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulators

2. **Calculate the value of LSB and MSB for an 8-Bit DAC for 0 to 10v range. (Dec-14)**

$$LSB = \frac{1}{2^8} = \frac{1}{256}$$

For 10V range, $LSB = \frac{10V}{256} = 39mv$

$$MSB = \left(\frac{1}{2}\right) fullscale = 5V$$

Full scale output=(full scale voltage -1 LSB)

= 10V – 0.039V =9.961 V

3. **What is meant by IC voltage regulator? (Dec-14)**

A voltage regulator is designed to automatically maintain a constant voltage levels. Its an electronic integrated circuit that provides a stable DC voltage independent of the load current, temperature and AC line voltage variations.

4. **Define series regulator. (April-15)**

   The series regulator works by providing a path from the supply voltage to the load through a variable resistance (the main transistor is in the "top half" of the voltage divider). The power dissipated by the regulating device is equal to the power supply output current times the voltage drops in the regulating device.

5. **Write the application of analog multipliers. (Nov-15)**

- Variable-gain amplifier
- Ring modulator
- Product detector
- Analog signal processing
- Automatic gain control
- True RMS converter
- Analog filters
- PAM-pulse amplitude modulation
- Frequency mixer
- It is used in frequency converters and to solve non-linear equations

6. **Which is the fastest ADC? Write the disadvantage of this types of ADC. (Nov-15)**

Flash type A/D converter is the fastest ADC because the fast conversion speed is accomplished by providing 2n-1comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

Disadvantage of Flash Type:

- Needs many parts (255 comparators for 8-bit ADC)
- Lower resolution
- Expensive
- Large power consumption

7. **Define the resolution of D/A converter. (Nov-15A)**

The resolution of either a digital-to-analog converter (DAC) or an analog-to-digital converter (ADC) is the measure of how finely its output may change between discrete, binary steps. For instance, an 8-bit DAC with an output voltage range of 0 to 10 volts will have a resolution of 39.22 mV

8. **Define ADC. (Nov-15A)**

An analog-to-digital converter is any device that converts analog signals (continuous quantity) into digital signals (discrete time digital representation). The analog signal is a continuous sinusoidal wave form that cannot be read by a computer, hence the need for conversion. By converting the analog signal to digital signal, data can be amplified, added or taken from the original signal.

9. **What do you mean by line regulation in IC voltage regulator? (Nov-13)**

Line regulation is defined as the percentage change in the output voltage for a change in the input voltage. It is expressed in millivolts or as a percentage of the output voltage.

10. **What is a voltage regulator?**

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

11. **Give the classification of voltage regulators:**

(i). Series / Linear regulators
(ii). Switching regulators.

12. What is a linear voltage regulator?

Series or linear regulator uses a power transistor connected in series between the unregulated dc input and the load and it conducts in the linear region .The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor.

13. What are the advantages of IC voltage regulators?

- low cost
- high reliability
- reduction in size
- excellent performance

14. Define load regulation.

Load regulation is defined as the change in output voltage for a change in load current. It is expressed in millivolts or as a percentage of the output voltage.

15. What is meant by current limiting?

Current limiting refers to the ability of a regulator to prevent the load current from increasing above a preset value.

16. What is the function of a series pass transistor in a voltage regulator?

The function of a voltage regulator circuit is basically this - maintain a precise voltage regardless of the current drawn by the load.

17. Give the drawbacks of linear regulators:

- The input step down transformer is bulky and expensive because of low line frequency.
- Because of low line frequency, large values of filter capacitors are required to decrease the ripple.
- Efficiency is reduced due to the continuous power dissipation by the transistor as it operates in the linear region.

18. What is the advantage of switching regulators?

- Greater efficiency is achieved as the power transistor is made to operate as low impedance switch. Power transmitted across the transistor is in discrete pulses rather than as a steady current flow.
- By using suitable switching loss reduction technique, the switching frequency can be increased so as to reduce the size and weight of the inductors and capacitors.

19. Differentiate between linear and switching regulators.

S.No	Linear regulator	Switching Regulator
1.	In series regulator the transistor is used	In switching regulator transistor is used as a

		controlled switch is used
2.	It is operated in linear region. Therefore it is called linear regulator	It is operated in cut off or saturation region
3.	It dissipates more power	The device is operated at cut off there is no current and dissipates no power
4.	The efficiency is less than 70%	The efficiency is 70-90%

20. List the broad classification of ADCs?

- Direct type ADC
- Integrating type ADC

21. List out the direct type ADC$_s$?

- Flash (comparator)type converter
- Counter type converter
- Tracking or servo converter
- Successive approximation type converter

22.List out some integrating type converters?

- Charge balancing ADC
- Dual slope ADC

23. What is integrating type converter?

An ADC converter that perform conversion in an indirect manner by first changing the analog I/P signal to a linear function of time or frequency and then to a digital code is known as integration type A/D converter.

24. Explain in brief the principle of operation of successive approximation ADC?

The circuit of successive approximation ADC consists of a successive approximation register (SAR) to find the required value of each bit by trail & error. With the arrival of START command, SAR sets the MSB bit to 1. The o/P is converted into an analog signal & it is compared with I/P signal. This o/P is low or high. This process continues unit all bits are checked

25. What are the main advantages of integrating type ADC?

- The integrating type ADC's do not need a sample/Hold circuit at the input.
- It is possible to transmit frequency even in noisy environment or in isolated form.

26. Whereis the successive approximation type ADC's used?

The successive approximation ADC's are used in applications such as data loggers & instrumentation where conversion speed is important.

27. What is the main drawback of a dual-slop ADC?

The dual slope ADC has long conversion time. This is the main drawback of dual slope ADC.

28. State the advantages of dual slope ADC?

It provides excellent noise rejection of as signals whose periods are integral multiples of the integration time T.

29. Define conversion time?

It is defined as the total time required to convert an analog signal into its digital output. It depends on the conversion technique used & the propagation delay of circuit components. The conversion time of successive approximation type ADC is given by T=(n+1) Where T clock period Tc Conversion time N no. of bits

30. Define resolution of a data converter?

The resolution of a converter is the smallest change in voltage which may be produced at the output or input of the converter.

31.What are the limitations of Flash type ADC?

Flash type ADC employs 2n-1 comparators for conversion which makes it costlier which tradeoffs in the speed of conversion.

32.What are the advantages and disadvantages of R-2R ladder DAC?

Advantage:

- Easier to build accurately as only two precisions metal film resistors are required
- Number of bits can be expanded by adding more sections of same R/2R values.
- In inverted R/2R ladder DAC node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

Disadvantages:

- Wide range of resistor values are required
- The finite resistance of the switches disturbs the binary weighted relationship among various currents.

33. Whatare analog multipliers?

An analog multiplier is a circuit in which the output is proportional to the multiplication of the two input voltages.

34. Mention the parts of series regulators?

- Reference voltage circuit
- Error amplifier
- Series pass transistor
- Feedback network

35. What voltage options are available in 78XX/79XX voltage regulators?

There are 7 options available, such as 5V,6V,8V,12V,15V,18V,24V.

36.What are the characteristics of three terminal of IC regulators?

1.V_0 : the regulated output voltage is fixed at the value as specified by the manufacturer.
2. the unregulated input voltage must be atleast 2V more than the regulated output voltage.

3.I_{0max} : the load current may vary from zero to rated maximum output current.

4. thermal shutdown: the IC has the temperature sensor which turns OFF the IC when it becomes too hot.

37. Define load regulation?

The change in the output voltage for a change in load current and it is expressed in mV or percentage of V0.

38.What is the need of adjustable regulator?

In the laboratory one may need variable regulated voltage or voltage that is not available as standard fixed voltage regulator.this can be achieved by using a fixed three terminal regulator.

39. Limitations of IC 723?

- It has no in-built thermal protection
- it has no short circuit current limits

40. Limitations of linear voltage regulator?

- The input step-down transformer is bulky and the most expensive component of linear RPS mainly because of low line frequency.
- Due to low line frequency, large values of filter capacitors are required to decrease the ripple.
- Efficiency is very low

41. What are the 2 techniques used in DAC converter?

- Binary weighted resistor type
- R/2R ladder type.

42. What is meant by current driven DAC?

In this, the shunt resistors are used to generate n binary weighted currents which are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage.

43. Define dual slope ADC?

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrated and then measured by a counter.

44. Define voltage-to-frequency converter?

It produces a pulse train whose frequency is linearly proportional to an analog input voltage.

45. Typical specifications of VFC?

- Wide dynamic range
- Ability to operate to relatively high frequency
- Low linearity error
- High scale factor accuracy

1. Explain in detail about Series opamp regulator.

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Figure 6.1 shows a regulated power supply using discrete components. The circuit consists of following four parts:

1. Reference voltage circuit
2. Error amplifier
3. Series pass transistor
4. Feedback network.

It can be seen from Fig. 6.1 that the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o. So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o occurs. The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the $R_1 - R_2$ divider and fed back to the (–) input terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o' of the error amplifier drives the series transistor Q_1.

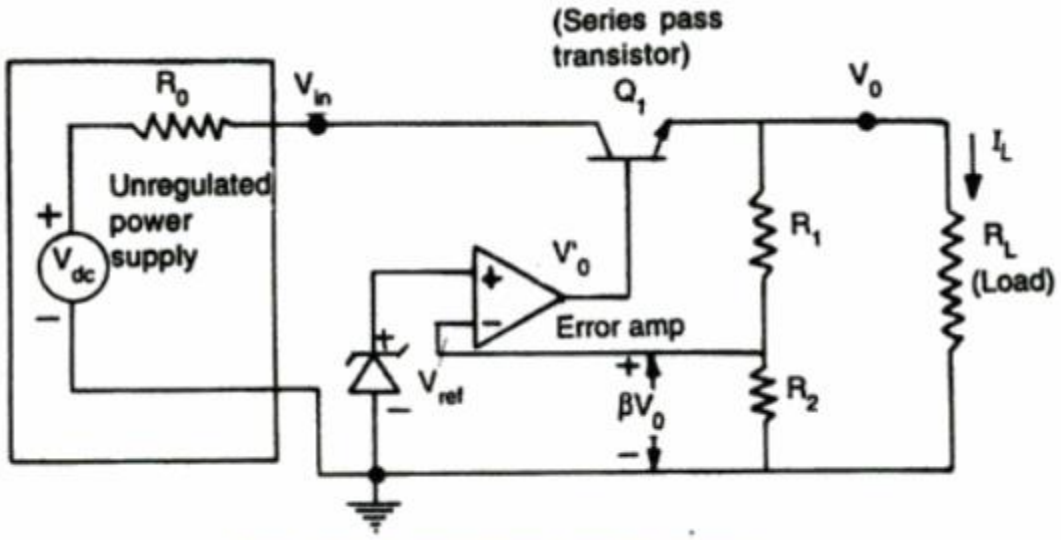


Fig. 6.1 A regulated power supply

If the output voltage increases, say, due to variation in load current, the sampled voltage βV_o also increases where

$$\beta \cong \frac{R_2}{R_1 + R_2} \tag{6.1}$$

This, in turn, reduces the output voltage V_o' of the diff-amp due to the 180° phase difference provided by the op-amp amplifier. V_o' is applied to the base of Q_1, which is used as an emitter follower. So V_o follows V_o', that is V_o also reduces. Hence the increase in V_o is nullified. Similarly, reduction in output voltage also gets regulated.

2. Explain in detail about IC Voltage regulator.

INRODUCTION:

- IC volage regulators gives
  - ✓ low cost,
  - ✓ high reliability,
  - ✓ reduction in size and
  - ✓ excellent performance.
- Examples of monolithic reglators are 78XX/79XX series and 723 general purpose regulators.

Fixed Voltage Series Regulator

78XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. In 78XX, the last two numbers (XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79XX series of fixed output, negative voltage regulators which are complements to the 78XX series devices. There are two extra voltage options of – 2 V and – 5.2 V available in 79XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)
Plastic package (TO – 220 type)

Figure 6.2 shows the standard representation of monolithic voltage regulator. A capacitor C_i (0.33 μF) is usually connected between input terminal and ground to cancel the inductive effects due to long distribution leads. The output capacitor C_o (1 μF) improves the transient response.

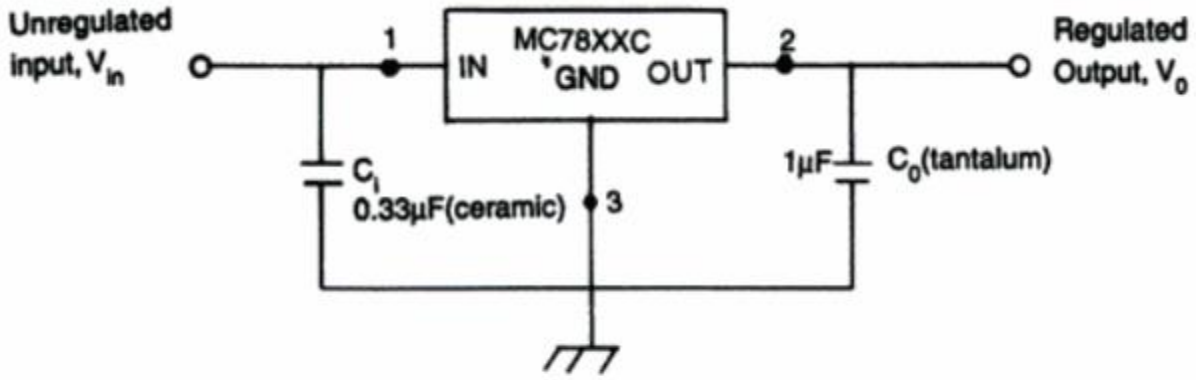


Fig. 6.2 Standard representation of a three terminal positive monolithic regulator

Characteristics

There are four characteristics of three terminal IC regulators which must be mentioned.

1. V_o : The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltages, for example, 78XX series has output voltage at 5, 6, 8 etc.
2. $|V_{in}| \geq |V_o| + 2$ volts: The unregulated input voltage must be atleast 2 V more than the regulated output voltage. For example, if $V_o = 5$ V, then $V_{in} = 7$ V.
3. $I_{o(max)}$: The load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.
4. Thermal shutdown: The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125° C to 150°C). The output current will drop and remain there until the IC has cooled significantly.

Applications of IC 78XX and 79XX

These ICs are regulator ICs and are basically used to provide constant d.c. voltages to various components in complex electronic circuits.

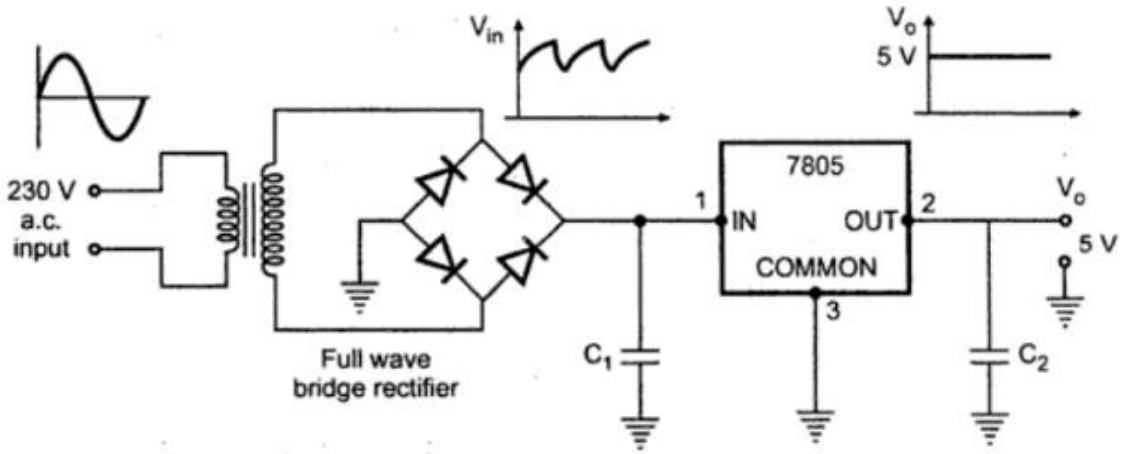
The IC 7805 is typically used to provide constant 5 V supply to the digital circuits.

The IC 7812 and 7912 are used to provide dual supply of ± 12 V to operational amplifiers used in the electronic circuits.

Device type	Output Voltage	Device type	Output Voltage
7805	5.0 V	7905	–5.0 V
7806	6.0 V	7906	–6.0 V
7808	8.0 V	7908	–8.0 V
7812	12.0 V	7912	–12.0 V
7815	15.0 V	7915	–15.0 V
7818	18.0 V	7918	–18.0 V
7824	24.0 V	7924	–24.0 V

Positive 5 V Power Supply using IC 7805

A 5 V output voltage supply system using full wave bridge rectifier, capacitor filter and IC regulator 7805 is shown in the Fig. 8.31. The a.c. line voltage is 230 V which is stepped down to 15 V using a transformer. A full wave rectifier alongwith the capacitor voltage provides the unregulated voltage input to IC 7805 regulator. This input contains a.c. ripple of few volts. The IC 7805 regulator provides the regulated output of 5 V.



5V Positive power supply

3. Explain in detail about Switching regulator.(Nov-13)

Limitations of Linear Voltage Regulators

1) The required input step down transformer is bulky and expensive.
2) Due to low line frequency (50 Hz), large values of filter capacitors are required.
3) The efficiency is very low.
4) Input must be greater than the output voltage.
5) As large is the difference between input and output voltage, more is the power dissipation in the series pass transistor.
6) For higher input voltages, efficiency decreases.
7) The need for dual supply, is not economical and feasible to achieve with the help of linear regulators.

The switching regulators overcome all these limitations.

Block Diagram of SMPS

The Fig. shows the functional block diagram of basic switching voltage regulator, which uses transistor Q_1 as a switch.

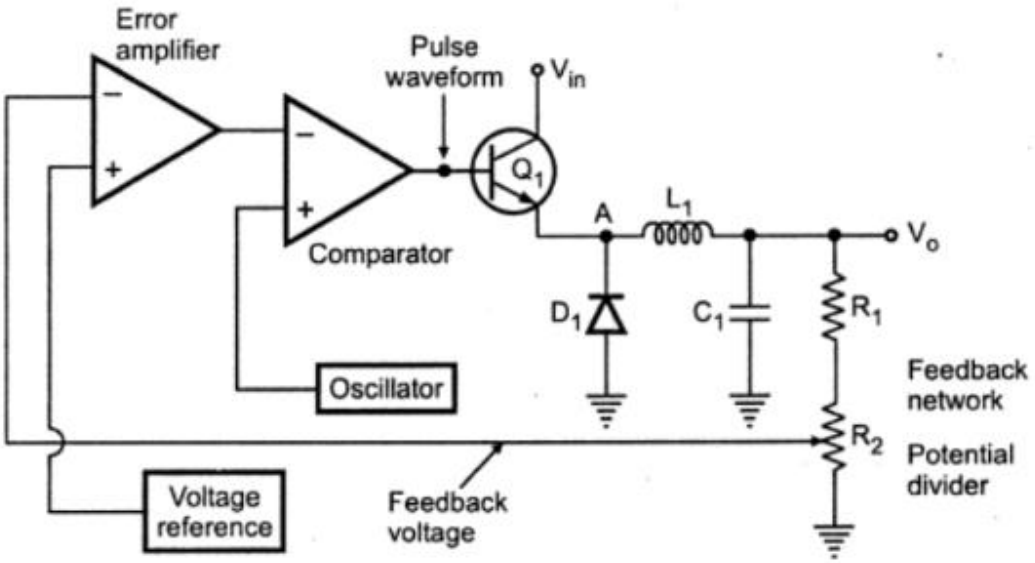


Fig. Functional block diagram of switching regulator

The part $R_2/R_1 + R_2$ of the output is fedback to the inverting input of error amplifier. It is compared with the reference voltage. The difference is amplified and given to the comparator inverting terminal.

The oscillator generates a triangular waveform at a fixed frequency. It is applied to the non-inverting terminal of the comparator. The output of the comparator is high when the triangular voltage waveform is above the level of the error amplifier output. Due to this the transistor Q_1 remains in cut-off state. **Thus the output of the comparator is nothing but a required pulse waveform.**

The period of this pulse waveform is same as that of oscillator output say T. The duty cycle is denoted as $\delta = t_{on}/T$ or t_{on} f as mentioned earlier. This duty cycle is controlled by the difference between the feedback voltage and the reference voltage.

When Q_1 is on in saturation state, $V_{CE(sat)}$ for Q_1 is zero. Hence entire input voltage V_{in} appears at point A. Thus the current flows through inductor L_1.

When Q_1 is off, L_1 still continue to supply current through itself to the load. The diode D_1 provides the return path for the current.

The capacitor C_1 acts to smooth out the voltage and the voltage at the output is almost d.c. in nature. The output voltage V_o of the switching regulator is a function of duty cycle and the input voltage V_{in}. Mathematically it is expressed as,

$$V_o = \frac{t_{on}}{T} V_{in} = \delta V_{in} \quad \ldots (1)$$

Thus when T is constant, output is proportional to t_{on}. This method is called **pulse width modulation (PWM)**. When t_{on} is constant, the output is inversely proportional to the period T i.e. proportional to frequency of the pulse waveform. This method is called **frequency modulation**.

A high switching frequency allows small values of L_1 and C_1 and thus reduces size, cost and weight. It also reduces the ripple at the output. But the efficiency decreases and electrical noise increases. On the other hand, low switching frequency improve efficiency and reduce noise but require large filtering components. As a result of this, the range of operating frequency to get maximum efficiency, is 10 to 50 kHz.

Types of Switching Regulators

There are three basic configurations of the switching regulators.

1. Step down or Buck switching regulator
2. Step up or Boost switching regulator.
3. Inverting type switching regulator.

Disadvantages:

- Noise is high
- More complex
- Switching regulator is slower than linear regulator

4. What is the basic technique of digital to analog converter? Explain any one type of DAC converter. (April-14),(April-15)

D/A Converters

A DAC (Digital to Analog Converter) accepts an n-bit input word b_1, b_2, b_3, ... b_n in binary and produce an analog signal proportional to it. Fig. 6.2(a) shows circuit symbol and input-output characteristics of a 4-bit DAC. There are four digital inputs, indicating 4-bit DAC. Each digital input requires an electrical signal representing either a logic 1 or a logic 0. The b_n is the least significant bit, LSB, whereas b_1 is the most significant bit, MSB.

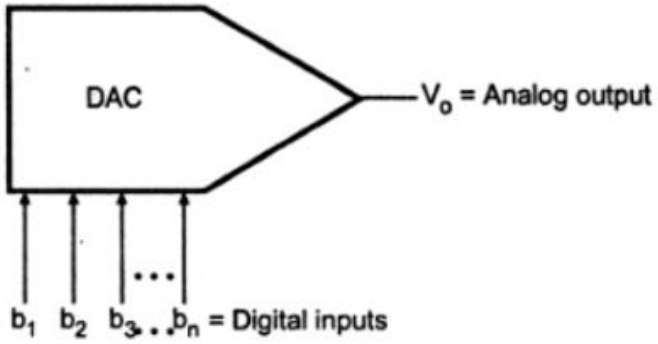


Fig. DAC circuit symbol

Basic Conversion Techniques

There are mainly two techniques used for analog to digital conversion

- Binary weighted resistor D/A converter
- R/2R ladder D/A converter

In these techniques, the shunt resistors are used to generate n binary weighted currents. These currents are added according to switch positions controlled by the digital input and then converted into voltage to give analog voltage equivalent to the digital input. Therefore, such digital to analog converters are called **current driven DACs**.

Binary Weighted Resistor D/A Converter

The binary weighted resistor DAC uses an op-amp to sum n binary weighted currents derived from a reference voltage V_R via current scaling resistors 2R, 4R, 8R, ..., 2^n R, as shown in the Fig. 6.3.

As shown in the Fig. 6.3, switch positions are controlled by the digital inputs. When digital input is logic 1, it connects the corresponding resistance to the reference voltage V_R; otherwise it leaves resistor open. Therefore,

For ON-switch, $I = \frac{V_R}{R}$ and

For OFF-switch, $I = 0$

Here, operational amplifier is used as a summing amplifier. Due to high input impedance of op-amp, summing current will flow through R_f. Hence the total current through R_f can be given as

$$I_T = I_1 + I_2 + I_3 + \cdots + I_n$$

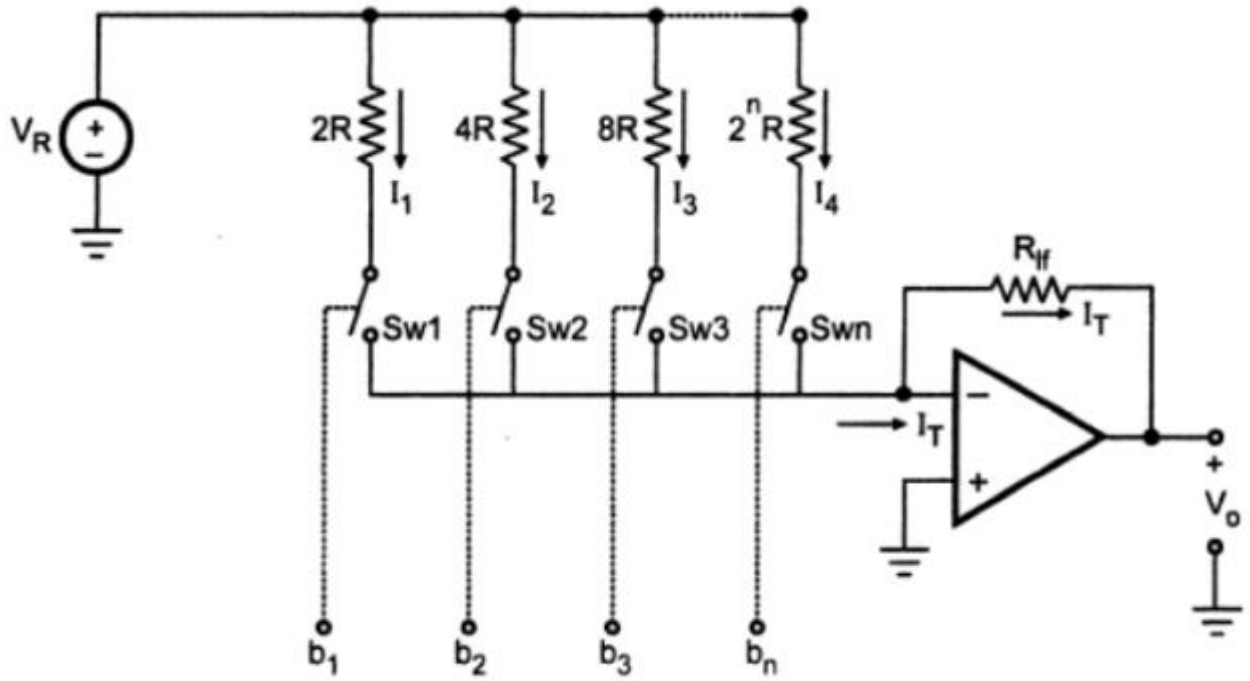


Fig. 6.3 Binary weighted resistor DAC

The output voltage is the voltage across R_f and it is given as

$$V_o = -I_T R_f = -(I_1 + I_2 + I_3 + \cdots + I_n) R_f$$

$$= -\left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R}\right) R_f$$

$$= -\frac{V_R}{R} R_f (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n}) \quad \ldots (4)$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n}) \quad \ldots (5)$$

The equation (4) indicates that the analog output voltage is proportional to the input digital word.

The simplicity of the binary weighted DAC is offset by drawbacks associated with it.

Drawbacks :

1. Wide range of resistor values are required. For 8-bit DAC, the resistors required are 2^1 R, 2^2 R, 2^3 R,... and 2^8 R. Therefore, the largest resistor is 128 times the smallest one.
2. This wide range of resistor values has restrictions on both, higher and lower ends. It is impracticable to fabricate large values of resistor in IC, and voltage drop across such a large resistor due to the bias current also affects the accuracy. For smaller values of resistors, the loading effect may occur.
3. The finite resistance of the switches disturbs the binary-weighted relationship among the various currents, particularly in the most significant bit positions, where the current setting resistances are smaller.

All these drawbacks, especially the requirement of wide range of resistors restricts the use of binary weighted resistor DACs below 8-bits.

Inverted R/2R Ladder D/A Converter

R/2R ladder D/A converter uses only two resistor values. This avoids resistance spread drawback of binary weighted D/A converter. Fig. 6.4 shows R/2R ladder DAC. Like binary weighted resistor DAC, it also uses shunt resistors to generate n binary weighted currents ; however it uses voltage scaling and identical resistors instead of resistor scaling and common voltage reference used in binary weighted resistor DAC. Voltage scaling requires an additional set of voltage dropping series resistances between adjacent nodes, as shown in the Fig. 6.4.

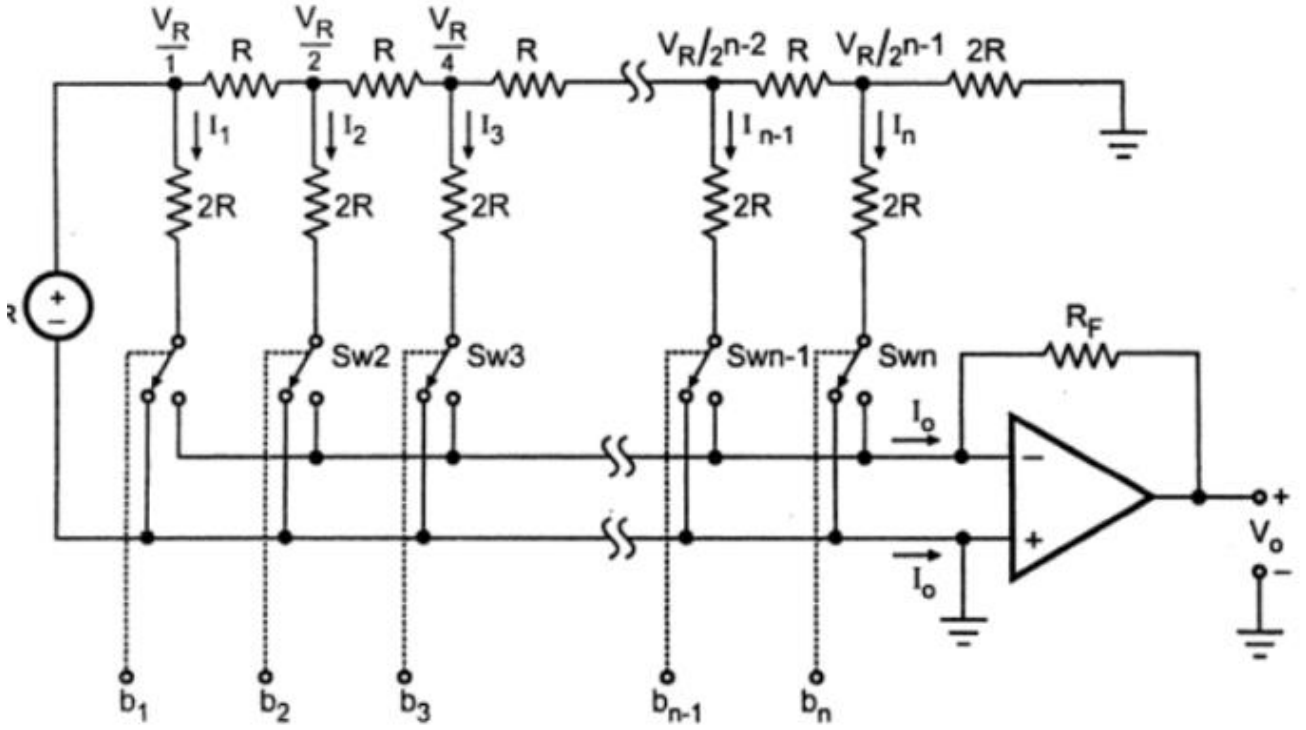


Fig. 6.4 Inverted R/2R ladder DAC

Here, each bit of the binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is at the virtual ground. Since both the positions of switches are at ground potential, the current flowing through resistances is constant and it is independent of switch position. These currents can be given as

$$I_1 = \frac{V_R}{2R} \qquad \ldots (6)$$

$$I_2 = \frac{V_R/2}{2R} = \frac{V_R}{4R} = \frac{I_1}{2}$$

$$I_3 = \frac{V_R/4}{2R} = \frac{V_R}{8R} = \frac{I_1}{4}$$

$$I_n = \frac{V_R/2^n - 1}{2R} = \frac{I_1}{2^n - 1} \qquad \ldots (7)$$

We know that, V_o is given as

$$V_o = -I_T R_f \qquad \ldots (8)$$

$$V_o = -R_f (I_1 + I_2 + I_3 + \cdots + I_n)$$

$$= -R_f \left(b_1 \frac{V_R}{2R} + b_2 \frac{V_R}{4R} + b_3 \frac{V_R}{8R} + \cdots + b_n \frac{V_R}{2^n R} \right)$$

$$= \frac{-V_R R_f}{R} (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n}) \quad \ldots (9)$$

When $R_f = R$, V_o is given as

$$V_o = -V_R (b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \cdots + b_n 2^{-n}) \quad \ldots (10)$$

Let us consider 4-bit binary DAC with binary input 1001 and $R_f = R$, as shown in the Fig. 6.5.

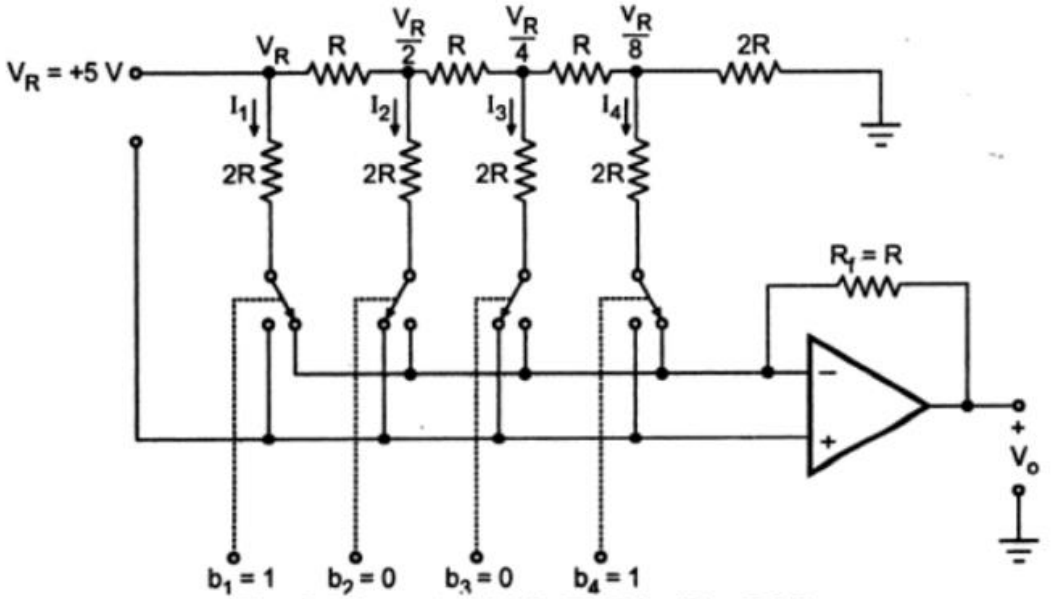


Fig. 6.5 Inverted 4-bit R/2R ladder DAC

Here, output voltage is given as

$$V_o = -V_R (1 \times 2^{-1} + 0 \times 2^{-2} + 0 \times 2^{-3} + 1 \times 2^{-4})$$

$$= -V_R \left(\frac{1}{2} + 0 + 0 + \frac{1}{16} \right) = -0.5625\ V_R = 2.8125\ V$$

The inverting R/2R ladder DAC works on the principle of summing currents and it is also said to operate in the **current mode**. An important advantage of the current mode is that all ladder node voltages remain constant with changing input codes, thus avoiding any shutdown effects by stray capacitances.

R/2R Ladder D/A Converter

In this type, reference voltage is applied to one of the switch positions, and other switch position is connected to ground, as shown in the Fig. 6.6.

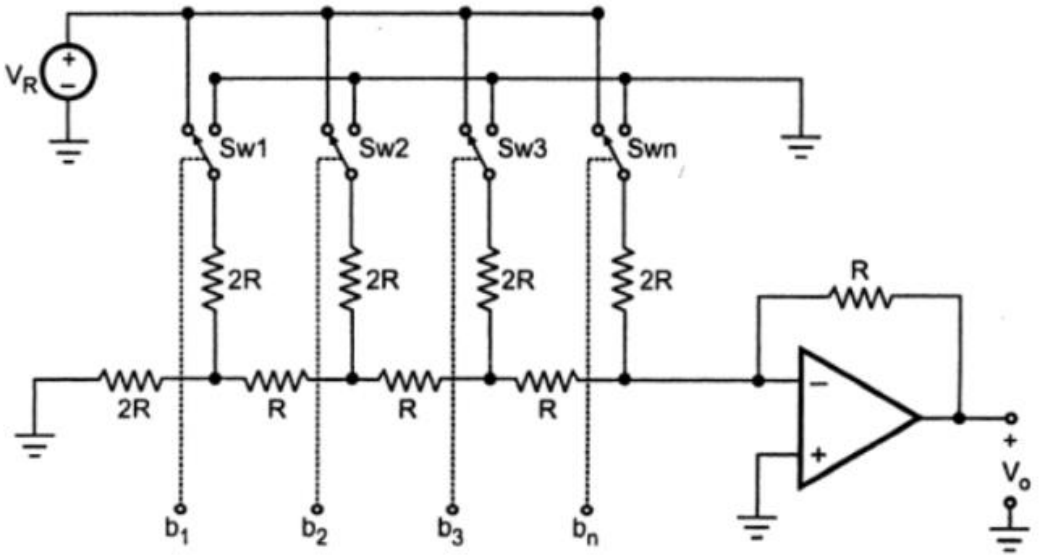


Fig. 6.6 R/2R ladder D/A converter

Let us consider 3-bit R/2R ladder DAC with binary input 001, as shown in the Fig. 6.7.

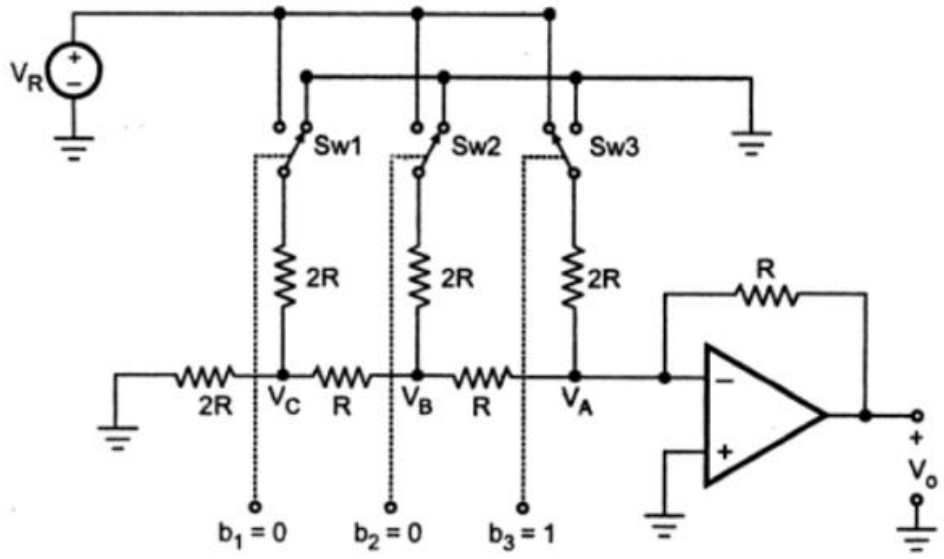


Fig. 6.7 3-bit R/2R ladder DAC

Reducing above network to the left by Thevenin's theorem we get,

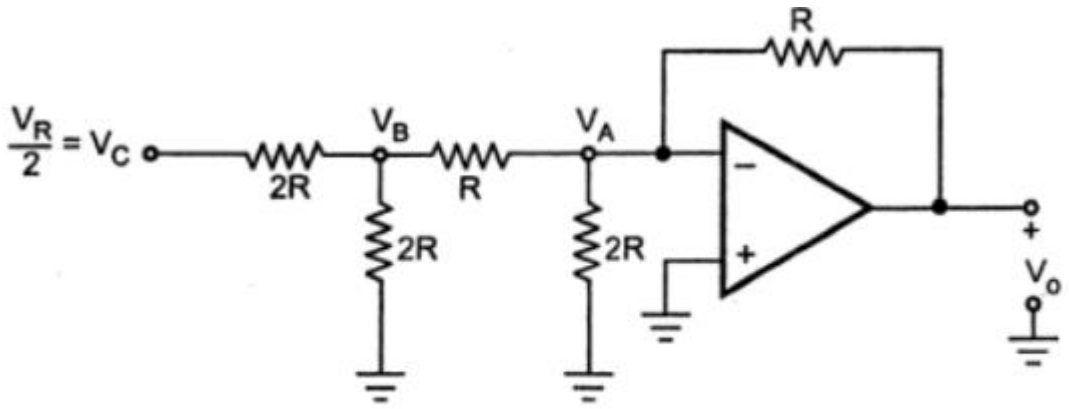


Fig. 6.8 (a)

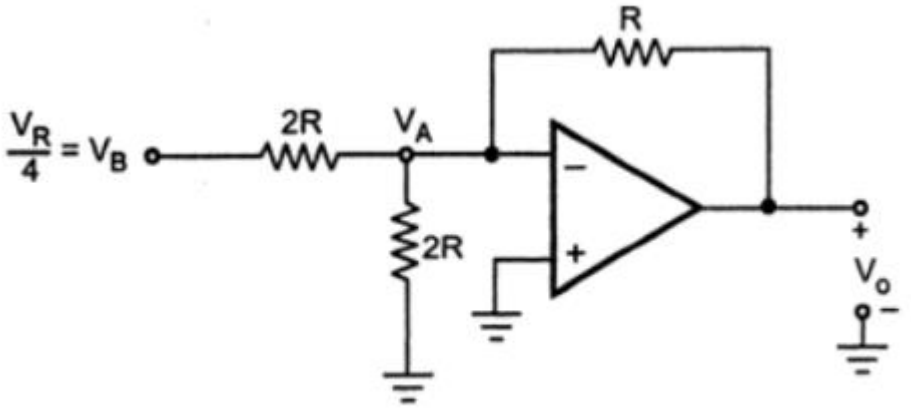


Fig. 6.8 (b)

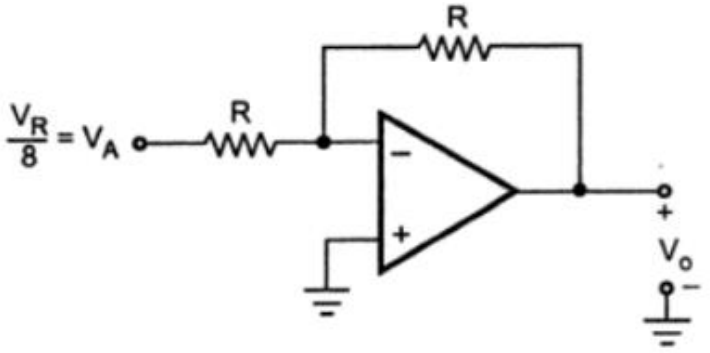


Fig. 6.8 (c)

Therefore, the output voltage is $V_R/8$ which is equivalent to binary input 001.

For binary input 100 the network can be reduced as follows :

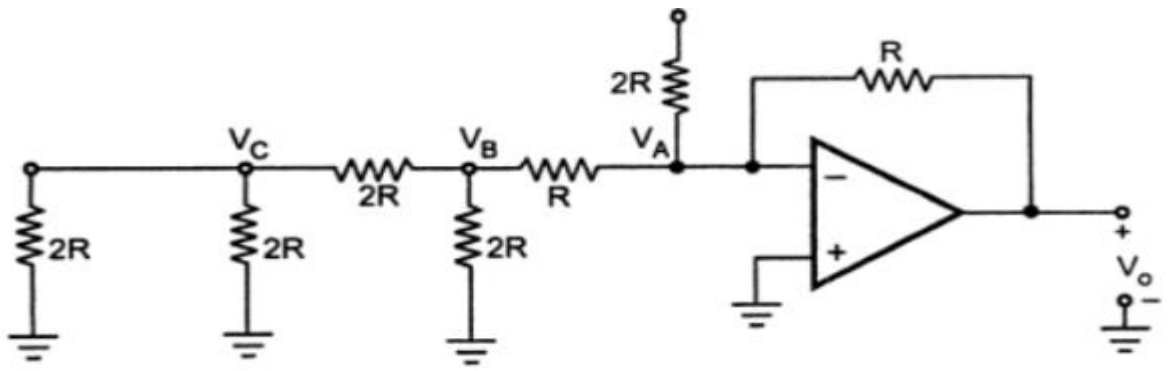


Fig. 6.9 (a)

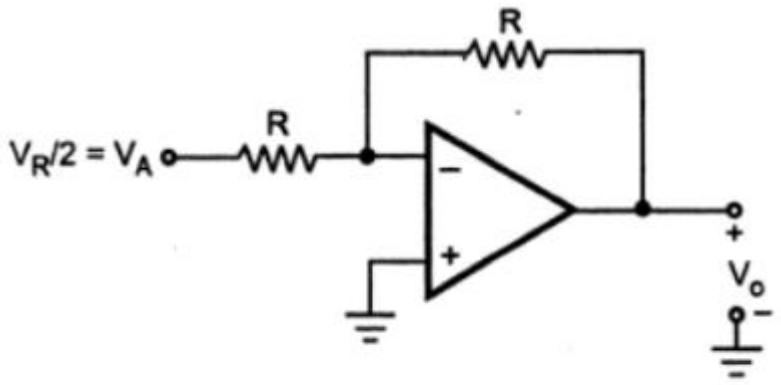


Fig. 6.9 (b)

Therefore, the output voltage is $V_R/2$, which is equivalent to binary input 100.

In general, the expression for V_o can be obtained as,

Let I_{out} = Output current

R_f = feedback resistance of op-amp

$\therefore \quad V_o = -I_{out} R_f$

Now I_{out} = current resolution × D

$\therefore \quad V_o = -$ (current resolution × D) R_f

$\therefore \quad V_o = -$ (current resolution × R_f) × D ... (11)

The coefficient of D is the voltage resolution and can be called as simple resolution.

$\therefore \quad V_o = -$ resolution × D ... (12)

In terms of actual circuit elements, output can be written as,

$$V_o = -\left(\frac{V_R}{R} \times \frac{1}{2^n} R_f\right) \times D \qquad ...(13)$$

The resolution of R/2R ladder type DAC with current output is,

$$\text{resolution} = \frac{1}{2^n} \times \frac{V_R}{R} \qquad ... (14)$$

while the resolution fo R/2R ladder type DAC with voltage output is,

$$\text{resolution} = \left(\frac{1}{2^n} \times \frac{V_R}{R}\right) \times R_f \qquad ...(15)$$

Advantages of R/2R ladder DACs :

1. Easier to build accurately as only two precision metal film resistors are required.
2. Number of bits can be expanded by adding more sections of same R/2R values.
3. In inverted R/2R ladder DAC, node voltages remain constant with changing input binary words. This avoids any slowdown effects by stray capacitances.

5. What is the basic technique of analogtodigital converter? Explain any one type of ADC converter. (Nov-13)

A/D Converters

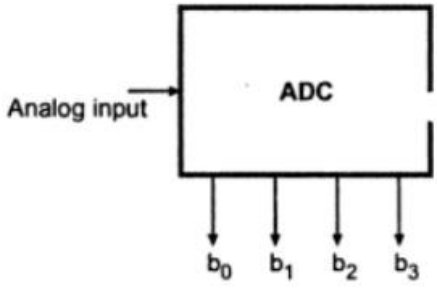


Fig. 6.16 Symbol for 4 bit ADC

The A/D conversion is a quantizing process whereby an analog signal is converted into equivalent binary word. Thus the A/D converter is exactly opposite function that of the D/A converter.

Fig. 6.16 shows symbol for A/D converter.

Basic Conversion Techniques

Analog to digital converter are classified into two general groups based on the conversion techniques. One technique involves comparing a given analog signal with the internally generated reference voltages. This group includes successive approximation, flash, delta modulated (DM), adaptive delta modulated and flash type converters. The another technique involves changing an analog signal into time or frequency and comparing these new parameters against known values. This group includes integrator converters and voltage-to-frequency converters.

The various types of ADC converters are as follows:

1. Single ramp or single slope
2. Dual slope
3. Successive approximation
4. Flash
5. Delta modulation
6. Adaptive delta modulation

Single Slope ADC

It consists of a ramp generator and BCD or binary counters. The Fig. 6.18 shows th single slope ADC.

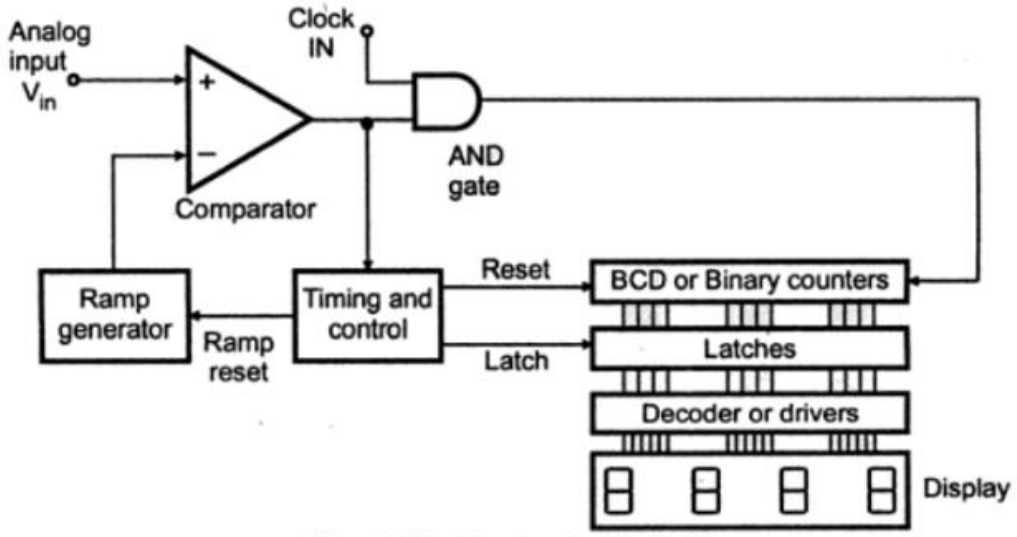


Fig. 6.18 Single slope ADC

At the start, the reset signal is provided to the ramp generator and the counters. Thus counters are resetted to 0's. The analog input voltage V_{in} is applied to the positive terminal of the comparator. As this is more positive than the negative input, the comparator output goes high. The output of ramp generator is applied to the negative terminal of the comparator. The high output of the comparator enables the AND gate which allows clock to reach to the counters and also this high output starts the ramp.

The ramp voltage goes positive until it exceeds the input voltage. When it exceeds V_{in}, comparator output goes low. This disables AND gate which inturn stops the clock to the counters. The control circuitry provides the latch signal which is used to latch the counter data. The reset signal resets the counters to 0's and also resets the ramp generator. The latched data is then displayed using decoder and a display device.

Let us consider the practical example to understand the working. Assume that the clock frequency is 1 MHz. There are four BCD counters and the input V_{in} is 2.000 V.

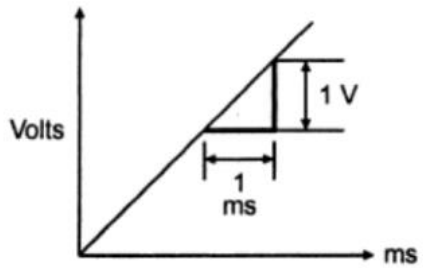


Fig. 6.19

Now let ramp has a slope of 1V/ms as shown in the Fig. 6.19. As the input is 2.000 V, the ramp will take 2 ms to reach to 2 V and to stop the clock to the counters.

Now how many pulses will reach to the counters during 2 ms ? It can be calculated from the frequency of the clock. The number of pulses reaching to the counter in 2 ms is $\frac{2ms}{(1/1MHz)}$ = 2000. The comparator output going high will strobe. The latches and send the count to the displays. Inserting a decimal point at the proper point in the seven segment display gives a reading of 2.000. But we want binary output. In such case instead of BCD counters, binary counters must be used, where output will be straight binary coded.

Drawbacks:

The main **limitations** of this circuit are,

i) Its resolution is less. Hence for applications which require resolution of 9 part in 20,000 or more, this ADC is not stable.

ii) Variations in ramp generator due to time, temperature or input voltage sensitivity also cause a lot of problems.

Dual Slope ADC

Dual slope conversion is an indirect method for A/D conversion where an analog voltage and a reference voltage are converted into time periods by an integrator, and then measured by a counter. The speed of this conversion is slow but the accuracy is high.

Fig. 6.20 shows a typical dual slope converter circuit. It consists of integrator (ramp generator), comparator, binary counter, output latch and reference voltage. The ramp generator input is switched between the analog input voltage V_i and a negative reference voltage, $-V_{REF}$. The analog switch is controlled by the MSB of the counter. When the MSB is a logic 0, the voltage being measured is connected to the ramp generator input. When MSB is logic 1, the negative reference voltage is connected to the ramp generator.

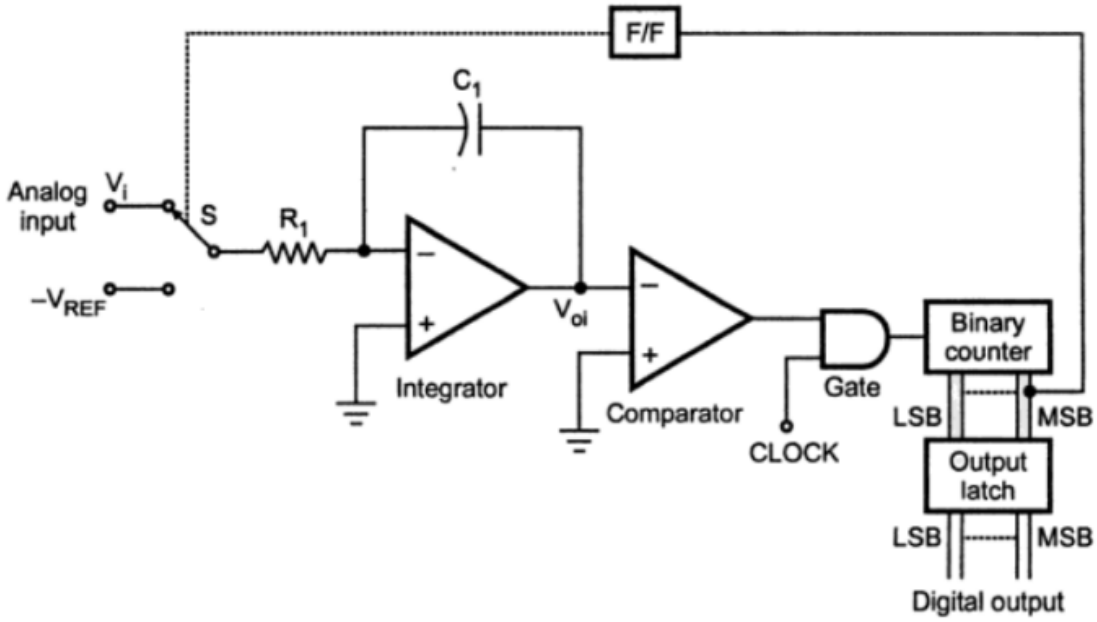


Fig. 6.20 Dual slope A/D converter

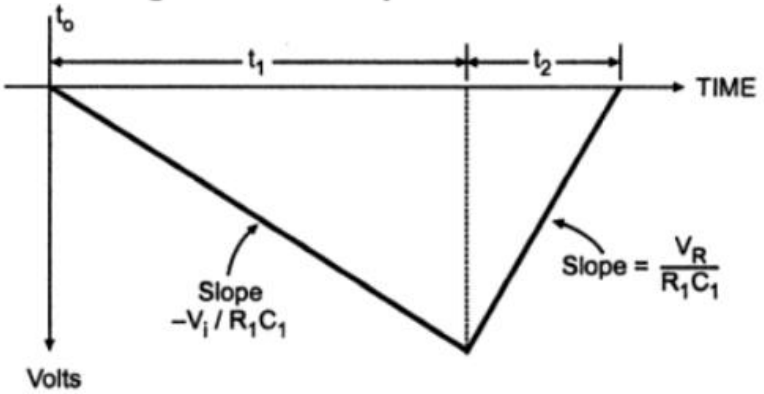


Fig. 6.21 Integrator output voltage

At time t = 0, analog switch S is connected to the analog input voltage V_i, so that the analog input voltage integration begins. The output voltage of the integrator can be given as,

$$V_{oi} = \frac{-1}{R_1 C_1} \int_0^t V_i \, dt$$

$$= \frac{-V_i\, t}{R_1\, C_1} \qquad \ldots (20)$$

where $R_1\, C_1$ is the integrator time constant and V_i is assumed constant over the integration time period. At the end of 2^N clock periods MSB of the counter goes high. At a result the output of the flip-flop goes high, which causes analog switch S to be switched from V_i to $-V_R$. At this very same time the binary counter which has gone through its entire count sequence is reset.

The negative input voltage ($-V_R$) connected to the input of integrator causes the integrator output to ramp positive. When integrator output reaches zero, the comparator output voltage goes low, which disables the clock AND gate. This stops the clock pulses reaching the counter, so that the counter will be stopped at a count corresponding to the number of clock pulses in time t_2.

The integrator output ramp down to a voltage V and get back upto 0. Therefore, the charge voltage is equal to discharge voltage and we can write,

$$\frac{V_i\, t_1}{R_1\, C_1} = \frac{V_R\, t_2}{R_1\, C_1}$$

$$\therefore \quad V_i\, t_1 = V_R\, t_2$$

$$\therefore \quad t_2 = \frac{V_i\, t_1}{V_R} \qquad \ldots (21)$$

The above equation shows that t_2 is directly proportional only to the V_i, since V_R and t_1 are constants. The binary digital output of the counter gives corresponding digital value for time period t_2 and hence it is also directly proportional to input signal V_i.

The actual conversion of analog voltage V_{in} into a digital count occurs during t_2. The control circuit connects the clock to the counter at the beginning of t_2. The clock is disconnected at the end of t_2. Thus the counter contents is digital output. Hence we can write,

$$\text{digital output} = \left(\frac{\text{counts}}{\text{second}}\right) t_2 \qquad \ldots(22)$$

But from (21) we can write,

$$\text{digital output} = \left(\frac{\text{counts}}{\text{second}}\right) t_1 \left(\frac{V_i}{V_R}\right) \qquad \ldots(23)$$

The counter output can then be connected to an appropriate digital display.

The advantages of dual slope ADC are

1. It is highly accurate.
2. Its cost is low.
3. It is immune to temperature caused variations in R_1 and C_1.

The only disadvantage of this ADC is its speed which is low.

Successive Approximation ADC

In this technique, the basic idea is to adjust the DAC's input code such that its output is within ± ½ LSB of the analog input V_i to be A/D converted. The code that achieves this represents the desired ADC output.

The successive approximation method uses very efficient code searching strategy called binary search. It completes searching process for n-bit conversion in just n clock periods.

Fig. 6.22 shows the block diagram of successive approximation A/D converter. It consists of a DAC, a comparator, and a successive approximation register (SAR).

The external clock input sets the internal timing parameters. The control signal start of conversion (SOC) initiates an A/D conversion process and end of conversion signal is activated when the conversion is completed.

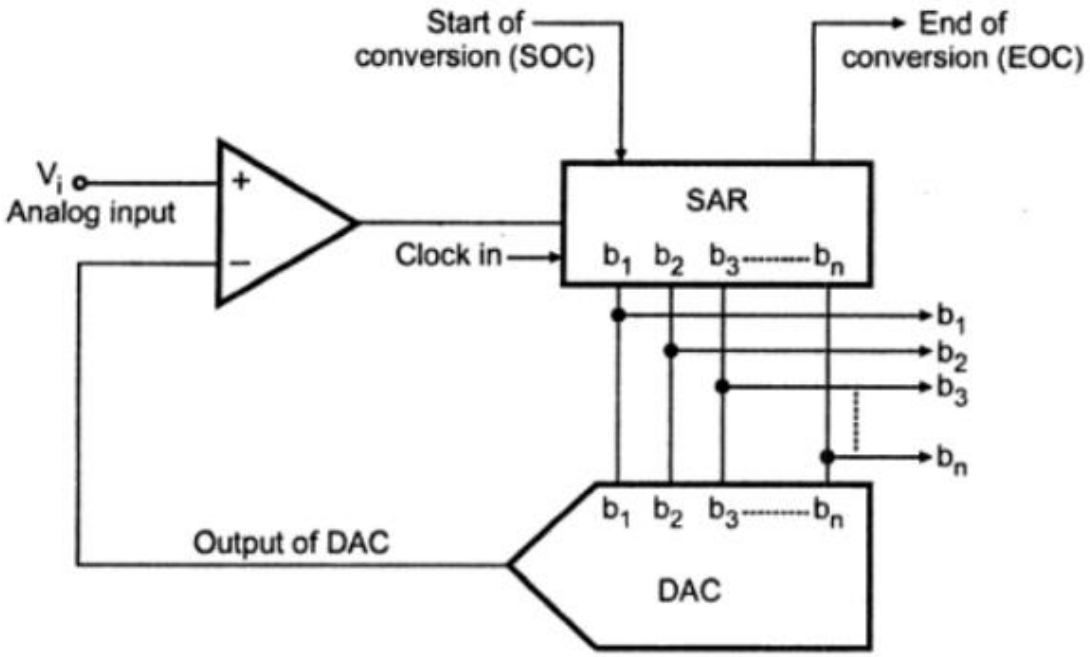


Fig. 6.22 Block diagram of successive approximation A/D converter

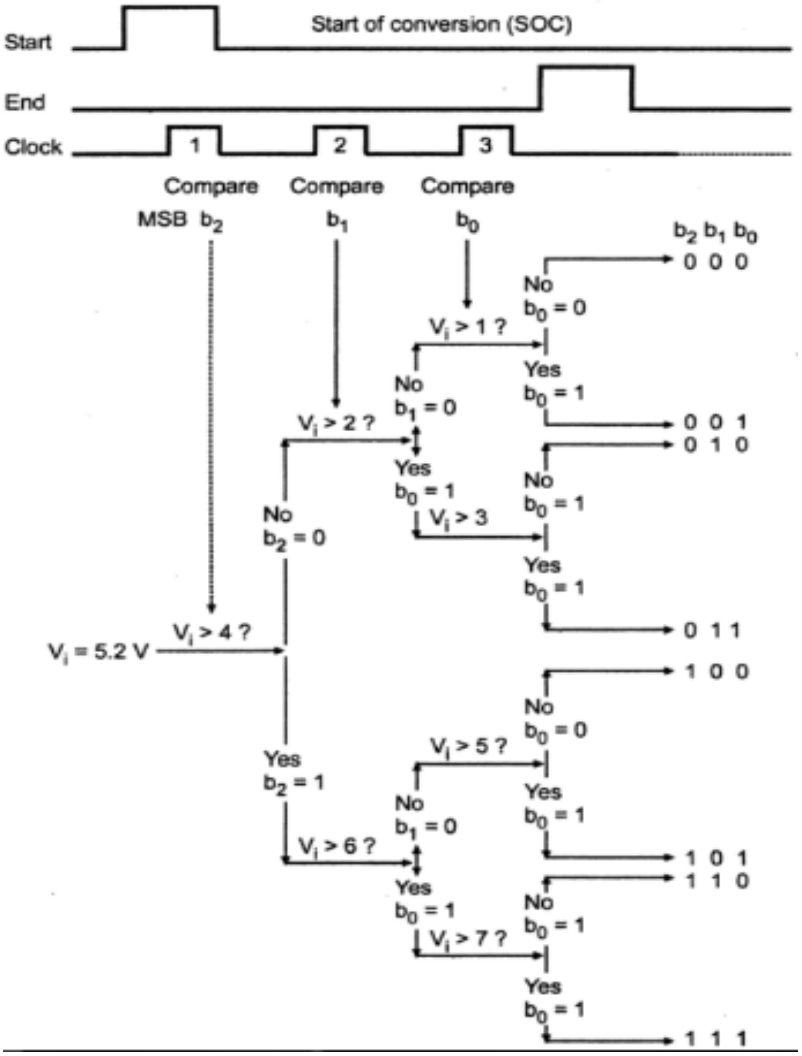
Operation :

The searching code process in successive approximation method is similar to weighing an unknown material with a balance scale and a set of standard weights. Let us assume that we have 1 kg, 2 kg and 4 kg weights (SAR) plus a balance scale (comparator and DAC). Now we will see the successive approximation analogy for 3-bit ADC.

Refer Fig. 6.22 and 6.23. The analog voltage V_{in} is applied at one input of comparator. On receiving start of conversion signal (SOC) successive approximation register sets 3-bit binary code 100_2 (b_2 = 1) as an input of DAC. This is similar process of placing the unknown weight on one platform of the balance and 4 kg weight on the other. The DAC converts the digital word 100 and applies its equivalent analog output at the second input of the comparator. The comparator then compares two voltages just like comparing unknown weight with 4 kg weight with the help of balance scale. If the input voltage is greater than the analog output of DAC, successive approximation register keeps b_2 = 1

and makes $b_1 = 1$ (addition of 2 kg weight to have total 6 kg weight) otherwise it resets $b_2 = 0$ and makes $b_1 = 1$ (replacing 2 kg weight). The same process is repeated for b_1 and b_0. The status of b_0, b_1 and b_2 bits gives the digital equivalent of the analog input. Fig. 6.23 illustrates the process we have just discussed.

The dark lines in the Fig. 6.23 shows setting and resetting actions of bits for input voltage 5.2 V, on the basis of comparison. It can be seen from the Fig. 6.23 that one clock pulse is required for the successive approximation regsiter to compare each bit. However an additional clock pulse is usually required to reset the register prior to performing a conversion.



The time for one analog to digital conversion must depend on both the clock's period T and number of bits n. It is given as,

$$T_C = T (n + 1) \quad \ldots(24)$$

where T_C = conversion time

T = clock period

n = number of bits

Flash ADC or Parallel Comparator ADC

When system designs call for the highest speed available, flash-type A/D converters (ADCs) are likely to be the right choice. They get their names from their ability to do the conversion very rapidly. Flash A/D converters, also known as a simultaneous or parallel comparator ADC, because the fast conversion speed is accomplished by providing $2^n - 1$

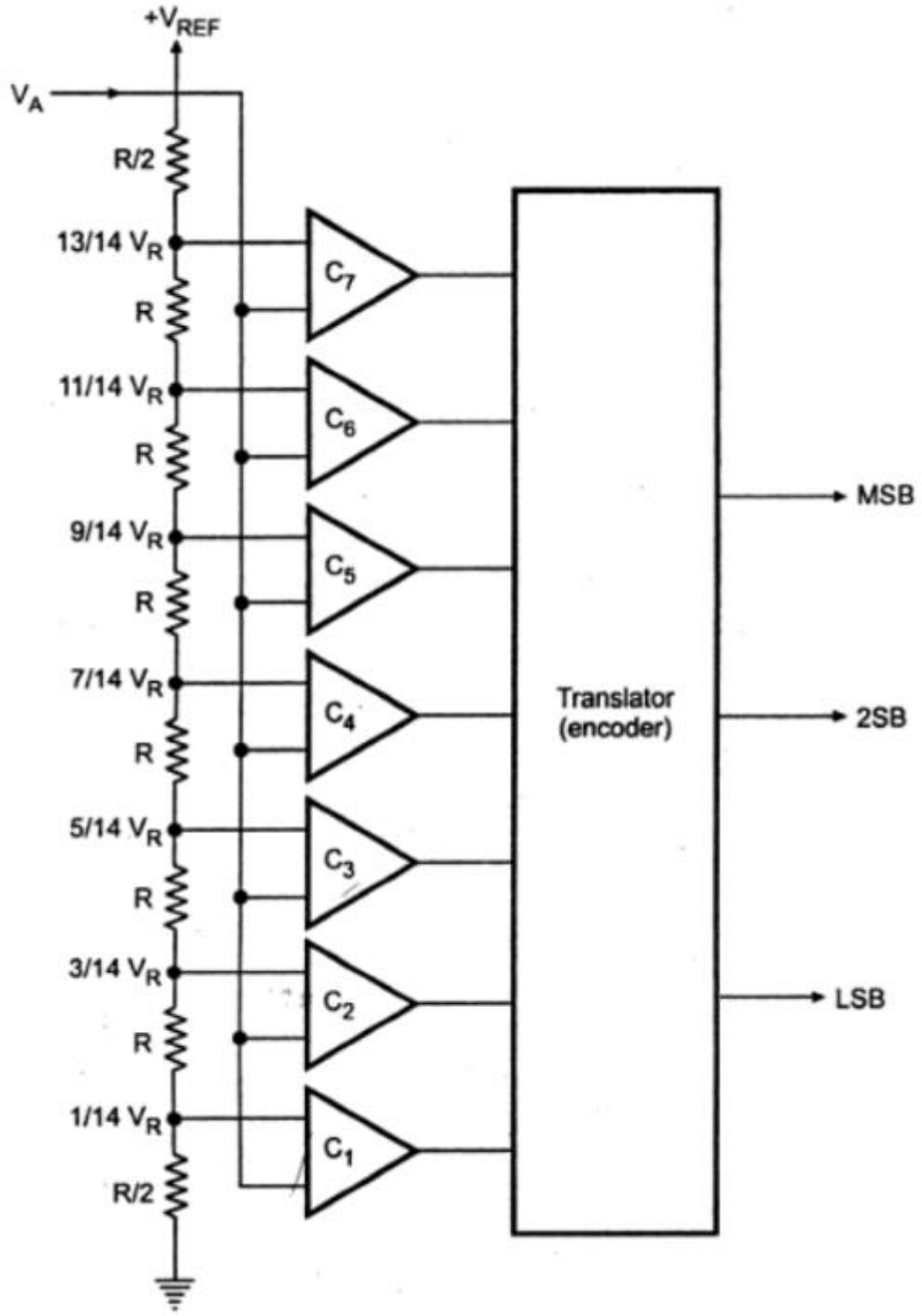


Fig. 6.24 3-bit flash converter

comparators and simultaneously comparing the input signal with unique reference levels spaced 1 LSB apart.

Fig. 6.24 shows 3-bit flash A/D converter. For this ADC, seven $(2^3 - 1)$ comparators are required. As shown in the Fig. 6.24, one input of each comparator is connected to the input signal and other input to the reference voltage level generated by the reference voltage divider. The reference voltage (V_{REF}) is equal to the full scale input signal voltage. The manner in which the flash A/D converter performs a quantization is relatively simple.

The comparators give output "1" or "0" state depending on whether the input signal is above or below the reference level at that instant. Those comparators referred above the input signal, remain turned-off, representing a "0" state. The comparators at or below the input signal conversely become a "1" state. The code resulting from this comparator is converted to a binary code by the encoder.

The number of comparators required for n bit resolution is,

$$\text{number of comparators} = 2^n - 1 \qquad \ldots(25)$$

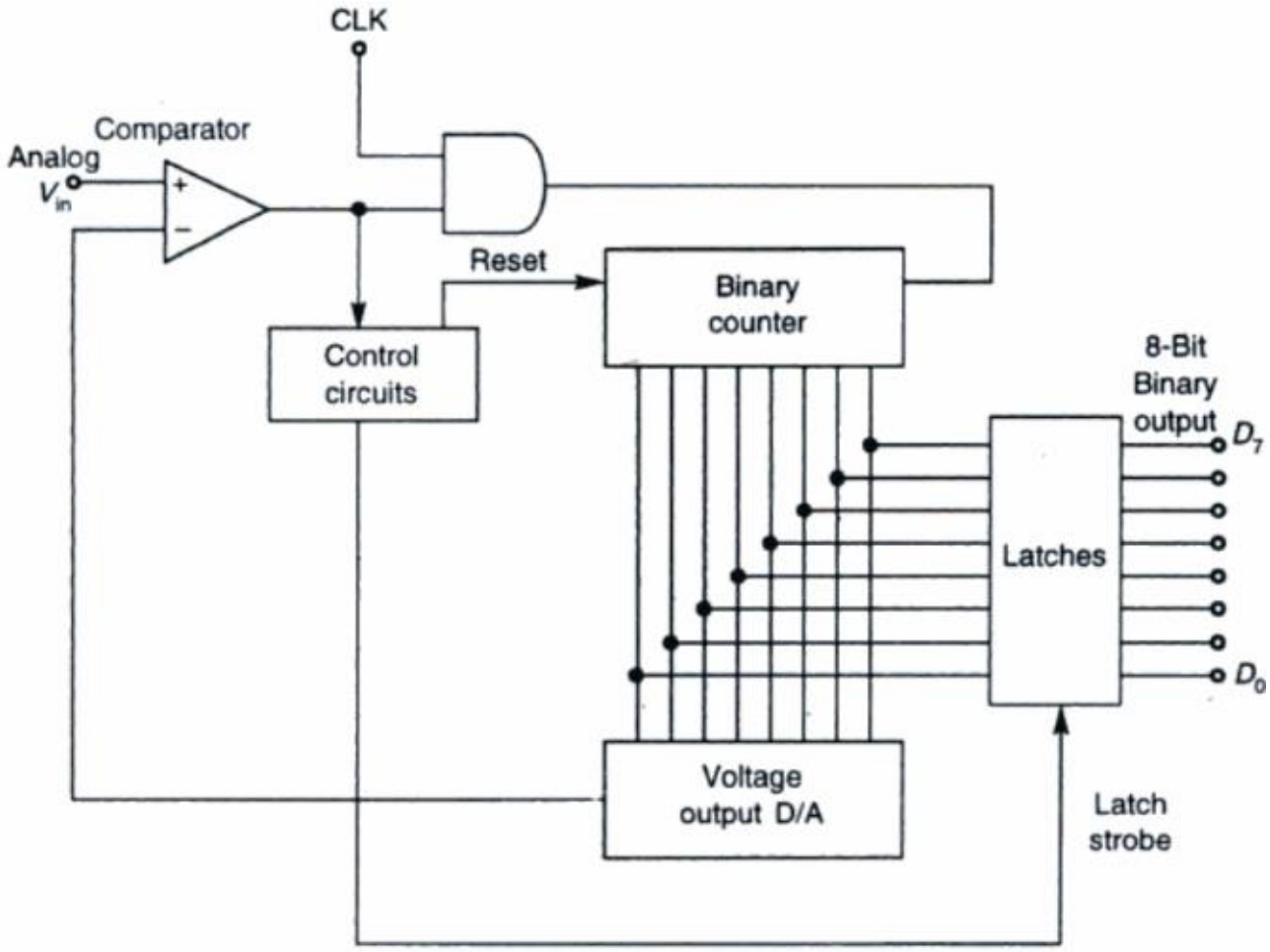
As seen earlier the quantization error is $\pm \frac{1}{2}$ LSB. Thus for an ADC, the maximum frequency for a sine wave V_{in} to be digitised within an accuracy of $\pm \frac{1}{2}$ LSB is,

$$f_{max} \cong \frac{1}{2\pi(T_C)2^n} \qquad \ldots (26)$$

where f_{max} = maximum input frequency
T_C = conversion time
n = number of bits

COUNTER TYPE A\D CONVERTER:

In this system, a continuous sequence of equally spaced pulses is passed through a gate. At the start of a conversion cycle, the counters are reset to 0, so the output of the D/A is at 0 V. A positive unknown voltage applied to



the input of the converter will cause the output of the comparator to go high and enable the AND gate. This will let the clock pulses into the counter. Each clock pulse increments the counter by 1 and increases the voltage on the output of the D/A converter by one step. When the voltage on the output of the D/A converter passes the voltage on the unknown V input, the output of the comparator will go low and shut off the clock pulses to the counters. The count accumulated on the counters is proportional to the input voltage. The control circuitry then strobes the latches to transfer the count to the output and resets the counters to start another conversion cycle.

The counter method is slower than flash type converter. The drawback of this type is that it requires a precision D/A converter. Another drawback of this type is that the counter has to start at 0 and count up until the D/A output passes the input voltage. For an 8-bit converter, then, conversion, may take as long as 255 clock cycles and for a 10-bit converter, a conversion may take as many as 1024 clock pulses.

6. Explain the working of Voltage to Frequency converter.

DEFENITION:

A *Voltage-to-Frequency* (V/F) converter produces an output signal whose frequency at any instant is a function of the external control input voltage. The output signal may be a sine-wave, a square-wave or a train of pulses. The ideal characteristic of V/F converter is shown in Fig. 12.1(a), and it is represented by $f_o = k_v V_i$ where k_v is the *sensitivity* of V/F converter in Hertz per Volt. The V/F converter provides a simple form of *analog-to-digital* conversion

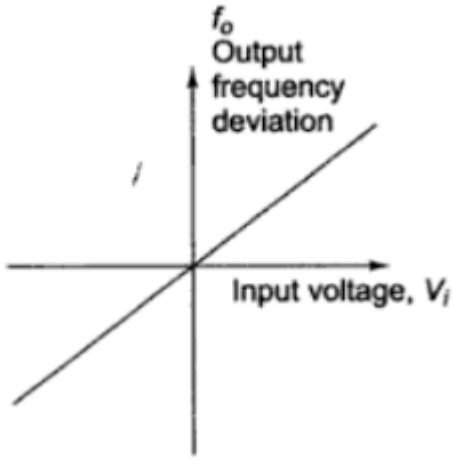


Fig. 12.1 *Ideal characteristics of (a) V/F Converter*

Voltage-to-Frequency Converter using VFC32

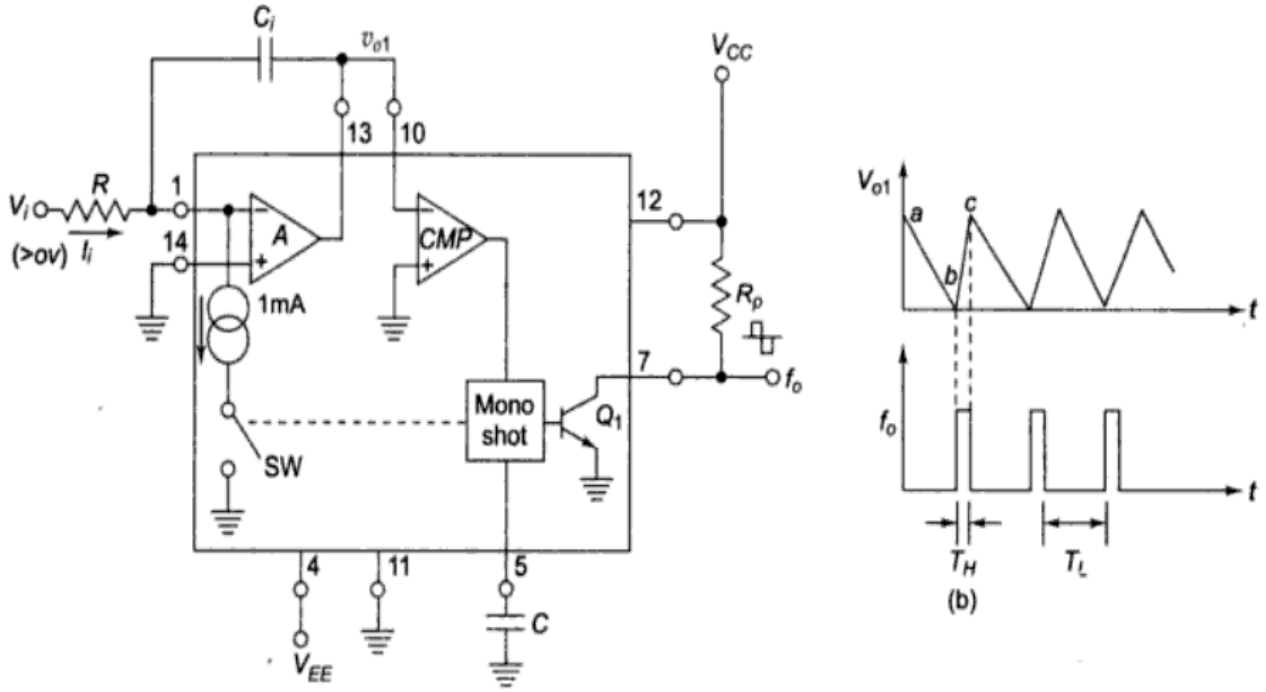


Fig. 12.3 *(a) Voltage-to-frequency Converter using VFC32, (b) Input and output characteristics*

VFC32 can be used for *Voltage-to-Frequency* conversion. This IC uses *charge balancing* technique. The process of charging and discharging results in a train of charge pulses, whose frequency is directly proportional to the input signal as given by $f_o = kV_i$.

A basic block diagram with the external connections for V/F conversion is shown in Fig. 12.3(a). The op-amp *A* converts the input V_i to a current as given by $I_i = V_i/R$ which flows into its summing junction. The value of R is selected such that I_i is always less than 1mA. When the switch SW is *open*, the current I_i flows into the capacitor C_i and charges it, causing the node v_{o1} to ramp downward as shown by line *ab* of Fig.12.3(b). When v_{o1} reaches zero, the comparator *CMP* triggers and sends a triggering signal to one-shot multivibrator that closes the switch *SW* and also turns the transistor *Q* ON for a time interval T_H set by capacitor *C*. The monostable multivibrator uses a threshold of 7.5V and a charging current of 1mA, thus giving

$$T_H = \frac{7.5 \times C}{1 \times 10^{-3}} \tag{12.3}$$

When the switch SW closes, a net current of magnitude $(1\text{mA} - I_i)$ flows out of the summing junction of op-amp *A*. Therefore, during the time T_H, the v_{o1} ramps upward by an amount given by

$$\Delta v_{oI} = (1\text{mA} - I_i)T_H/C_i \tag{12.4}$$

This is shown as line *bc* in Fig.12.3 (b). When the one-shot times out, the switch *SW* is again opened, and v_{o1} continues ramping downward at a rate determined by input current I_i. The time duration T_L taken for v_{o1} to return to zero is given by

$$T_L = C_i \Delta v_{o1}/I_i \tag{12.5}$$

T_L and T_H are related as given by

$$I_i T_L = (1\text{mA} - I_i)T_H$$

That is,
$$T_L + T_H = (1\text{mA})T_H/I_i \tag{12.6}$$

Combining Eqs. (12.3) with (12.6), and letting $I_i = V_i/R$ and $f_o = 1/(T_L + T_H)$ gives

$$f_o = \frac{V_i}{7.5RC} \tag{12.7}$$

where f_o is in Hertz, V_i in Volts, *R* in Ohms and *C* in Farads. Equation (12.7) shows that f_o is linearly proportional to V_i.

The duty cycle $D\,(\%) = 100 \times \frac{V_i}{R \times 1\text{mA}}$ which shows that the duty cycle *D* is proportional to V_i. For good linearity, the datasheets recommend a maximum duty cycle of 25%, which corresponds to an $I_i(max)$ of 0.25mA. Therefore, the capacitance C_i can be chosen arbitrarily.

The VFC32 offers 6-decades of dynamic range with typical linearity errors of 0.005%, 0.025% and 0.05% of full scale reading for corresponding frequencies of 10 kHz, 100 kHz and 500 kHz.

7. Explain the working of Frequencyto Voltage converter.

DEFENITION:

A *Frequency-to-Voltage* (F/V) converter produces an output voltage, whose amplitude is a function of frequency of the input signal. The input may be a sine-wave, a square-wave or a pulse train. The F/V converter is essentially an *FM detector* or *discriminator*.

An ideal F/V converter produces an analog signal represented by the relation

$$V_o = k_f f_i$$

where k_f is the *sensitivity* of F/V converter in Volts per Hertz. The ideal conversion characteristic of an F/V converter is shown in Fig. 12.1 (b).

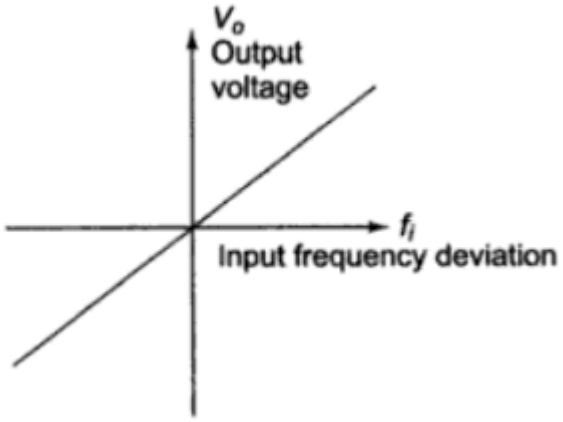
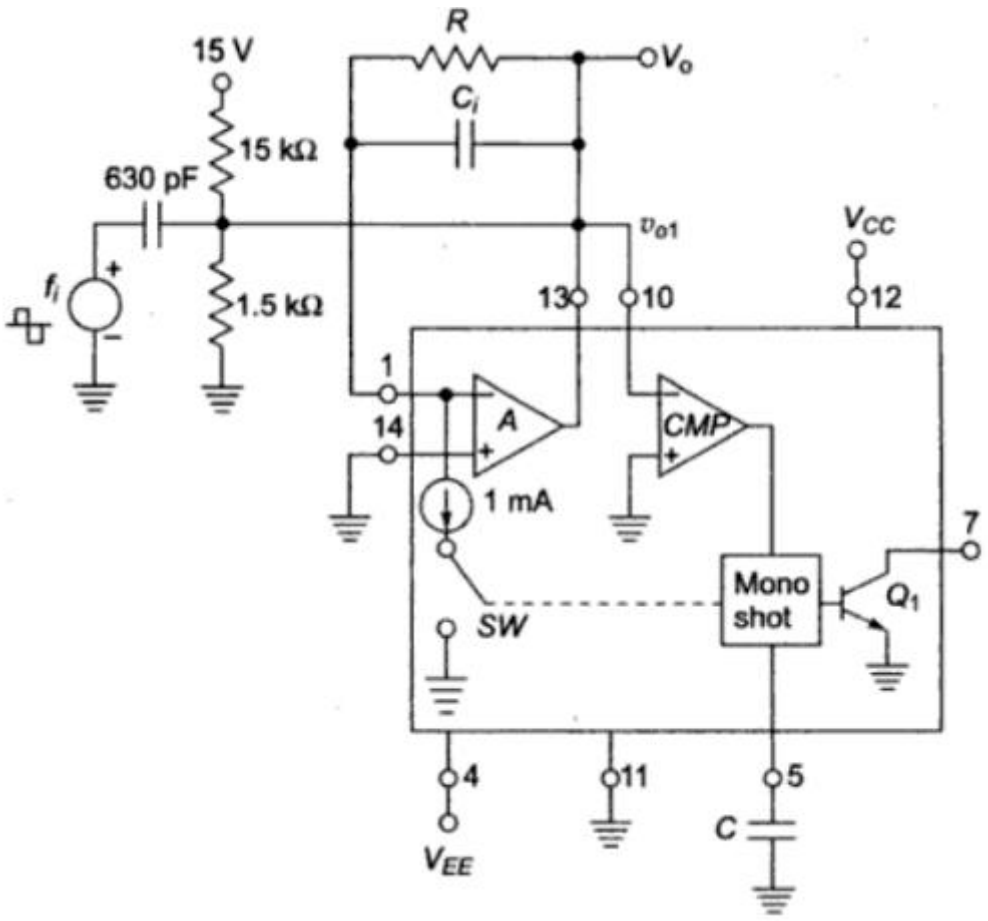


Fig. 12.1 *Ideal characteristics of (b) F/V Converter*

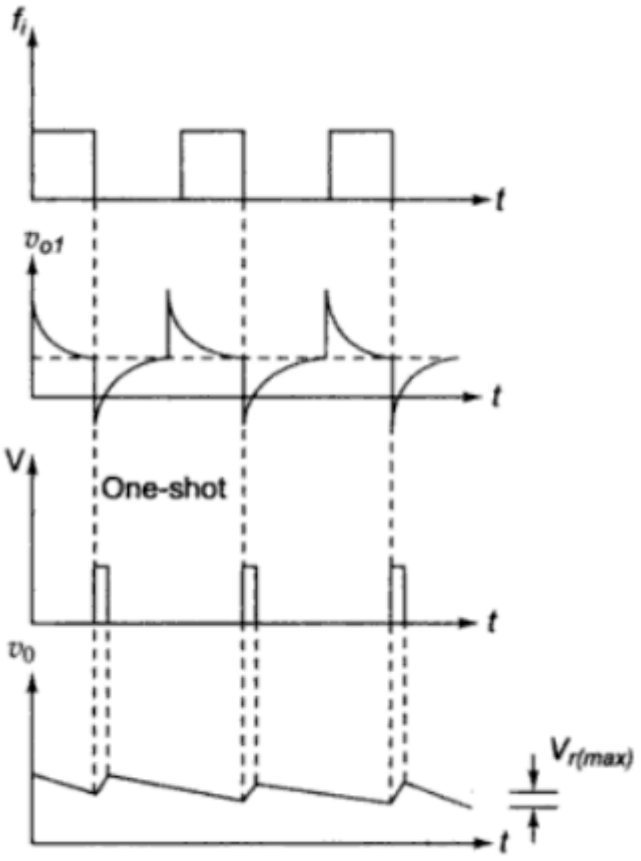
IC VFC32 Frequency-to-Voltage Converter

Figure 12.2(a) shows the circuit of F/V converter using the VFC32 V/F converter from Burr Brown. The input frequency is applied to the comparator *CMP* and the output is derived from the op-amp *A*. The resistor *R* acts as a feedback resistor. The capacitor C_i enables *charge-balancing*.

A *high-pass* network is connected at the input to accommodate TTL and CMOS compatible signals. It provides proper conditioning for the input signal and helps in accommodating inputs of TTL and CMOS type. For each negative spike of v_{o1}, the comparator *CMP* triggers the one-shot multivibrator, which has a threshold of 7.5 V and a charging current of 1 mA. The output of multivibrator closes the switch *SW*, pulling 1 mA out of C_i for a duration T_H, where $T_H = \frac{Cv_i}{I} = \frac{C \times 7.5}{1 \times 10^{-3}}$. This action causes V_o to build up and inject via *R*, and it continues until the current pulled out of the summing input of op-amp *OA* in 1 mA packets is exactly counter-balanced by that injected by V_o through *R* continuously.



(a)



(b)

(a) F/V converter using VFC32 and
(b) Input and output characteristics

Assume f_i to be the input frequency. Then the pulsed current is given by $f_i \times 1\text{mA} \times T_H$ and the continuous counter balancing current is given by $\frac{V_o}{R}$. That is,

$$V_o = 10^{-3} \times T_H \times R \times f_i \qquad (12.1)$$

Since $T_H = \frac{C \times 7.5}{1 \times 10^{-3}}$, the output voltage $V_o = 7.5RCf_1$

where f_i is in Hertz, V_o in Volts, R in Ohms and C in Farads. This indicates that the output V_o is proportional to the input frequency f_i. The waveforms at various nodes of *frequency-to-voltage* converter are shown in Fig. 12.2(b).

The maximum duty cycle recommended by the datasheet is 25% and this determines the value of C. The value of R determines the full scale value of V_o. Input offset voltage of op-amp A is to be nulled and this avoids the degradation of the conversion efficiency at low frequency ranges.

It is to be pointed out that, between successive closures of switch SW, the resistor R will cause C_i to discharge to a certain value. This creates ripples in output voltage v_o. The maximum ripple voltage is

$$v_{r(max)} = \frac{(1\text{mA})T_H}{C_i} \qquad (12.2)$$

Therefore, $v_{r(max)} = \frac{7.5 \times C}{C_i}$.

This shows that increasing the value of C_i reduces the magnitude of ripple voltage. But very large C_i degrades the circuit response to a rapid change in f_i, since the response is determined by the time constant $\tau = RC_i$. Hence, an optimum value of C_i is to be chosen to meet the conflicting demand.

8. Explain in detail about analog multiplier.

DEFENITION:

A multiplier produces an output V_o, which is proportional to the product of two inputs V_1 and V_2

That is, $V_o = K V_1 V_2$

where K is the scaling factor that is usually maintained as (1/10) V^{-1}.

ANALOG MULTIPLIER

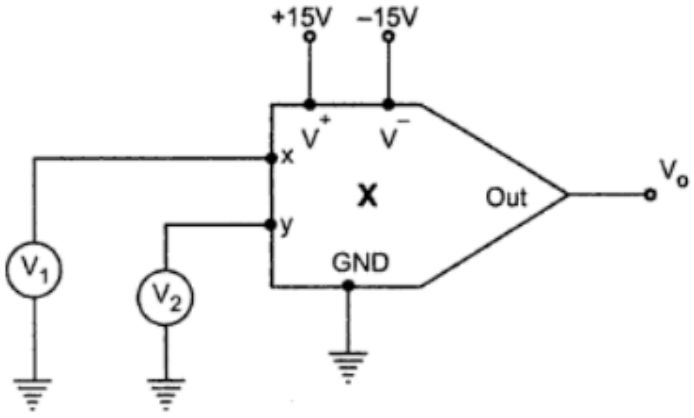


Fig. 4.3 Multiplier IC symbol

A basic multiplier is an active circuit in which the output voltage is proportional to the product of the two input signals. A schematic symbol of such basic multiplier IC is shown in the Fig. 4.3.

The terminals V^+ and V^- are supply terminals for IC where dual supply is to be connected, generally ± 15 V as shown. The x and y are the two input terminals where two inputs V_1 and V_2 are connected.

The output of such basic multiplier is

$$V_o = K V_1 V_2 \quad \ldots (1)$$

where K is constant and is equal to $1/V_{ref}$. Usually V_{ref} is set to 10 V internally and hence,

$$V_o = \frac{V_1 V_2}{10} \quad \ldots (2)$$

As long as it is ensured that both the input voltages are below the reference voltage, ($V_1 V_2 < V_{ref}$), the output of the basic multiplier will not saturate.

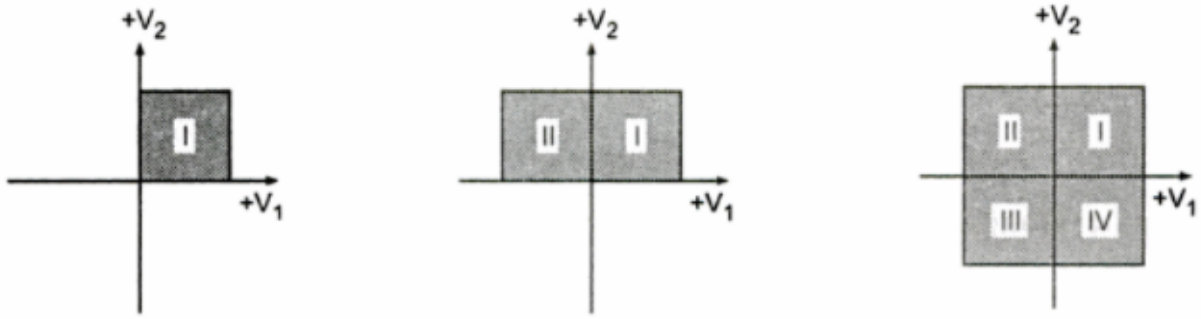
Depending on the use of the basic multiplier, it is necessary to restrict the polarity of one or both the inputs. Depending upon the polarity restriction, the IC operation is called as,

i) **One quadrant multiplier :** In such operation, the polarities of both the inputs must always be positive.

ii) **Two quadrant multiplier :** A two quadrant multiplier functions properly if one input is held positive and the other is allowed to swing in both positive and negative.

iii) **Four quadrant multiplier :** If both the inputs are allowed to swing in both positive and negative directions, the operation is four quadrant multiplier operation.

These operations are shown in the Fig. 4.4.



(a) One quadrant **(b) Two quadrant** **(c) Four quadrant**

Fig. 4.4 Multiplier modes of operation

There are various techniques availablr for analog muliplier:

Multiplier Techniques

The various techniques which are used for the multipliers are

i) Logarithmic multipliers.

ii) Quarter square multipliers

iii) Pulse width / height modulation multipliers

iv) Variable transconductance multipliers

v) Current rating multipliers

vi) Triangle averaging multipliers.

Applications of Multiplier

The multiplier is used in many practical applications. Some of these applications are:

1. In communication it is used in amplitude modulation, phase modulation, frequency modulation, phase detection, suppressed carrier modulation etc.
2. In instrumentation and control used to measure velocity, acceleration, instantaneous power, automatic gain control, etc.
3. For voltage controlled attenuators and for voltage controlled amplification.
4. It is used for voltage divider, true r.m.s calculation, rectifier phase shift detection etc.
5. It is used for frequency converters, frequency doubling and frequency shifting etc.
6. It is used for squaring and square root calculations.
7. It is used to solve nonlinear equations.

Voltage Divider Using Multiplier

The circuit in which output is the division of the two input signals, is called as a **voltage divider**. The use of multiplier as a voltage divider is shown in the Fig. 4.5.

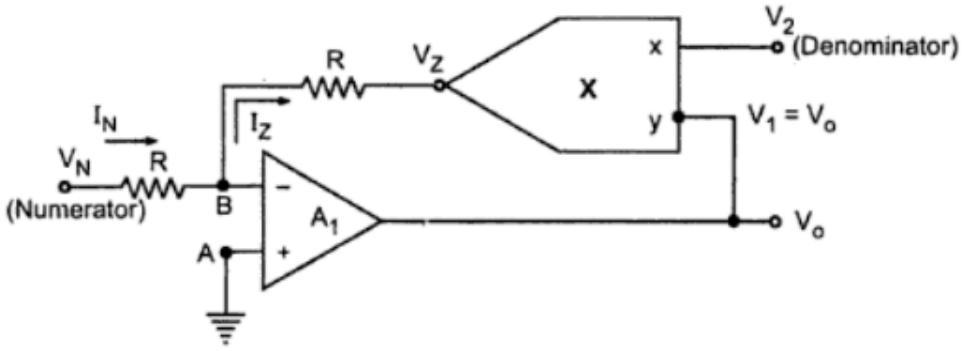


Fig. 4.5 Voltage divide

The multiplier is used in the feedback loop. The denominator is applied at the x input of the multiplier which is the voltage V_2. The numerator is applied at the input terminal of op-amp A_1.

As node A is grounded, node B is also at virtual ground, hence $V_B = 0$. As op-amp input current is zero,

$$I_N = I_Z = \frac{V_N}{R} = -\frac{V_Z}{R} \quad \text{... (1)}$$

Now $$V_Z = K V_1 V_2 = K V_o V_2 \quad \text{... (2)}$$

$\therefore$ $$\frac{V_N}{R} = -\frac{K V_o V_2}{R}$$

$\therefore$ $$\boxed{V_o = -\frac{V_N}{K V_2}} \quad \text{... (3)}$$

Thus the output is proportional to the division of the two input voltages V_N and V_2. The only requirement is that the input voltage V_2 must be negative. Hence divider circuits are at best two quadrant circuits.

UNIT –IV ACTIVE FILTERS AND WAVEFORM GENERATOR

First and second order Active filters - Low pass, high pass, band pass and band reject filters - State variable filter – Switched capacitor filter–Waveform generator – RC Phase shift and Wien-bridge oscillators – Multivibrators– triangular and sawtoothwavegenerator.

---

2 marks

1. Why are active filters preferred? (April-14)

Active filters are not heavy and size is also small because it does not use inductor. Also it much faster than passive filter. On the other hand it is easy to design and easy to tune, also it produces less loss.

Active filters have a number of desirable characteristics. They are easier to design, construct, and adjust. They perform almost ideally. They also have nearly zero output impedance, making their performance independent of the load. Active filters typically have gain associated with them.

2. Define a state variable filter. (April-15)

It uses three or four op amps & provides low pass, high pass, band pass & notch filter characteristics simultaneously.

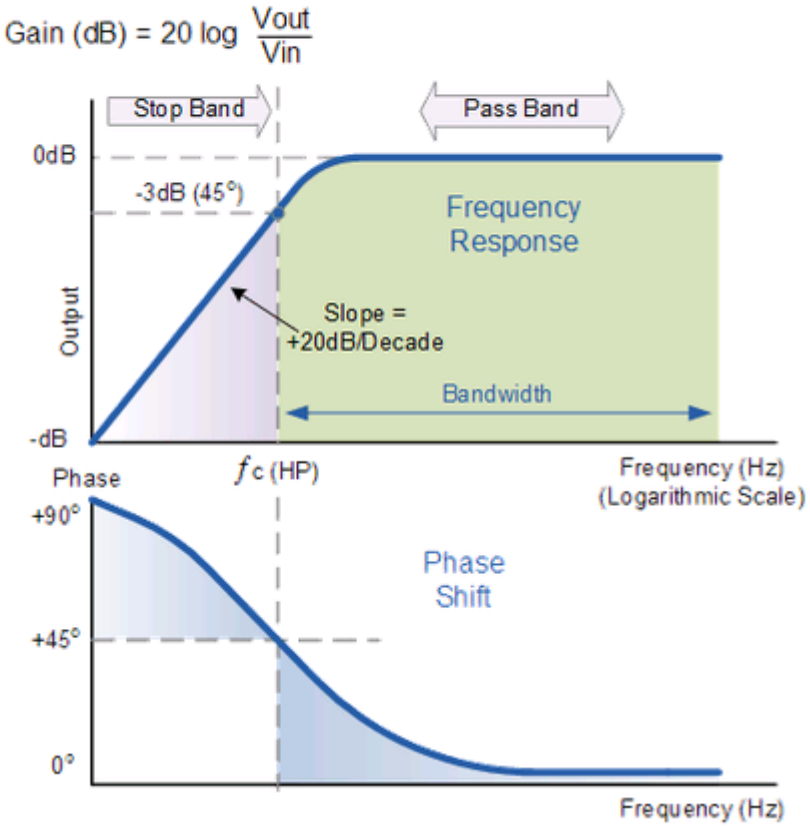
A state variable filter is a type of active filter. It consists of one or more integrators, connected in some feedback configuration. Any LTI system can be described as a state-space model, with n state variables for an nth-order system.

3. What are the modes of operation of a timer? (April-15)

- **Astable mode**
  An Astable Circuit has no stable state - hence the name "astable". The output continually switches state between high and low without any intervention
- **Monostable mode**
  A Monostable Circuit produces one pulse of a set length in response to a trigger input such as a push button. The output of the circuit stays in the low state until there is a trigger input, hence the name "monostable" meaning "one stable state".
- **Bistable Mode (or Schmitt Trigger)**
  A Bistable Mode or what is sometimes called a Schmitt Trigger, has two stable states, high and low. Taking the Trigger input low makes the output of the circuit go into the high state. Taking the Reset input low makes the output of the circuit go into the low state.

4. Draw the frequency response curve of a fist order high pass filter. (Nov-15)

Frequency Response of a 1st Order High Pass Filter.



5. What is a switched capacitor? Write its importance. (Nov-15)

- A switched capacitor is an electronic circuit element used for discrete time signal processing. It works by moving charges into and out of capacitors when switches are opened and closed.
- Filters implemented with these elements are termed "switched-capacitor filters," and depend only on the ratios between capacitances

6. What is FSK technique? (Nov-13)

Frequency-shift keying (FSK) is a frequency modulation scheme in which digital information is transmitted through discrete frequency changes of a carrier signal. The technology is used for communication systems such as amateur radio, caller ID and emergency broadcasts. The simplest FSK is binary FSK (BFSK).

7. Define filter?

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the frequency signals outside the band is called electric filter.

- **Passive Filters** : A passive filter is built with passive components such as resistors, capacitors and inductors.
- **Active Filters** : An active filter makes use of active elements such as transistors, op-amps in addition to resistor and capacitors

8. When does the flattest pass band occurs in low pass filters?

It occurs for damping coefficient of 1.414.

9. What is the damping coefficient for bessels filter?

It is heavily damped and has a damping coefficient of 1.73.

10. What are the demerits of passive filters?

Passive filters works well for highfrequencies. But at audio frequencies, the inductors become problematic, as they become large, heavy and expensive. For low frequency applications, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance ie, low Q, resulting in high power dissipation.

11. Mention some commonly used active filters :

- Low pass filter
- High pass filter
- Band pass filter
- Band reject filter.

12. What are the advantages of active filters?

- Active filters used op- amp as the active element and resistors and capacitors as passive elements.
- By enclosing a capacitor in the feedback loop , inductor less active filters can be obtained
- Op-amp used in non – inverting configuration offers high input impedance and low output impedance, thus improving the load drive capacity.

13. Why are active filters preferred at radio frequencies?

A low-pass active filter that can minimize radio-frequency interference because the attenuation occurs in passive components before any active elements might demodulate the RFI. This is a concern with op-amps because they typically don't act as amplifiers at RF frequencies.

14. What do you mean by frequency scaling?

Once the filter is designed, sometimes it is necessary to change the value of cut off frequency f_H. The method used to change the cut off frequency f_H to a new cut off frequency fH1 is called as frequency scaling.

15.Definebandpass filter.

A bandpass filter is basically a frequency selector. It allows one particular band of frequencies to pass. Thus, the pass band is between the two cut-off frequencies f_h and $f_l$where $f_h > f_l$. Any frequency outside this band gets attenuated.

16.What do you mean by low pass filter?

A low-pass filter is a filter that passes signals with a frequency lower than a certain cut off frequency and attenuates signals with frequencies higher than the cut off frequency. The amount of attenuation for each frequency depends on the filter design.

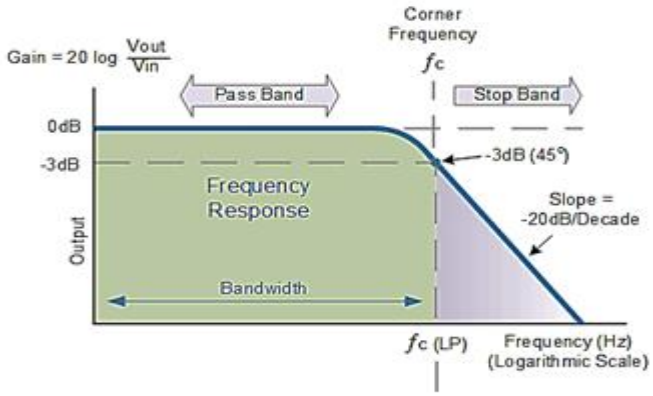
17.What do you mean by high pass filter?

A *high-pass filter* is an electronic *filter* that *passes* signals with a frequency higher than a certain cutoff frequency and attenuates signals with frequencies lower than the cutoff frequency. The amount of attenuation for each frequency depends on the *filter* design.

18. What do you mean by band reject filter?

In signal processing, a *band-stop filter* or *band-rejection filter* is a *filter* that passes most frequencies unaltered, but attenuates those in a specific range to very low levels. It is the opposite of a *band-pass filter*

19. Draw the frequency response curve of a first order low pass filter.



20. What is Butterworth response?(Nov-13)

The Butterworth filter is a type of signal processing filter designed to have as flat a frequency response as possible in the passband. It is also referred to as a maximally flat magnitude filter.

As the Butterworth filter is maximally flat, this means that it is designed so that at zero frequency, the first 2n-1 derivatives for the power function with respect to frequency are zero. Thus it is possible to derive the formula for the Butterworth filter frequency response:

$$\left|\frac{V_{out}}{V_{in}}\right|^2 = \frac{1}{1+(f/f_c)^{2n}}$$

Where:

f = frequency at which calculation is made

f_o = the cut-off frequency, i.e. half power or -3dB frequency

V_{in} = input voltage

V_{out} = output voltage

n = number of elements in the filter

21.What is a multivibrator?

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator.

22. What do you mean by monostablemultivibrator?

Monostablemultivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi-stable state. An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state.

23.What is an astablemultivibrator?

Astablemultivibrator is a free running oscillator having two quasi-stable states. Thus, there are oscillations between these two states and no external signal is required to produce the change in state.

24. What is a bistablemultivibrator?

Bistablemultivibrator is one that maintains a given output voltage level unless an external trigger is applied. Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until a second trigger is applied. Thus, it requires two external triggers before it returns to its initial state.

25.Comparemonostable and astablemultivibrator?

S.No	MonostableMultivibrator	Astablemultivibrator
1.	It has only one stable state	It has no stable state.
2.	Trigger is required for the operation	Trigger is not required for the operation
3.	Two components R & C are required with IC 555 to obtain the circuit.	Three components R , R & C are required with IC555 to obtain the circuit

26.Define an oscillator?

An oscillator is an amplifier, which uses a positive feedback and without any external input signal, generates an output waveform, at a desired frequency.

27.State the conditions for oscillation or Barkhausencriterian.

(i) the total phase shift around a loop, as the signal proceeds from input through amplifier, feedback network network back to input again, completing a loop is precisely 0 0r 360.

(ii) The magnitude of the product of the open loop gain of the amplifier A and the magnitude of the feedback factor β is unity i.e.$|A\beta| = 1$.

28. Mention any two audio frequency oscillators ?

- RC phase shift oscillator
- Wein bridge oscillator

29. Mentionany two audio frequency oscillators.

- ✓ RCphaseshift oscillator
- ✓ Wein bridgeoscillator

30.Whatare the characteristics ofa comparator?

- ✓ Speed ofoperation
- ✓ Accuracy
- ✓ Compatibilityoftheoutput

31. List the waveform produced by the function generator.

a. Sine waveform from the triangular wave(using sine wave synthesis)

b. square wave from triangular wave train.

c. Triangular wave (equal positive and negative slopes as well as maximum amplitude.

32.What is the use of the noise signal?

Noise is required nowadays as a test signal for a variety of measurements, e.g, for the evaluation of multichannel PCM systems, studies on biomedical phenomena, vibrating testing, aerodynamics, seismology**.**

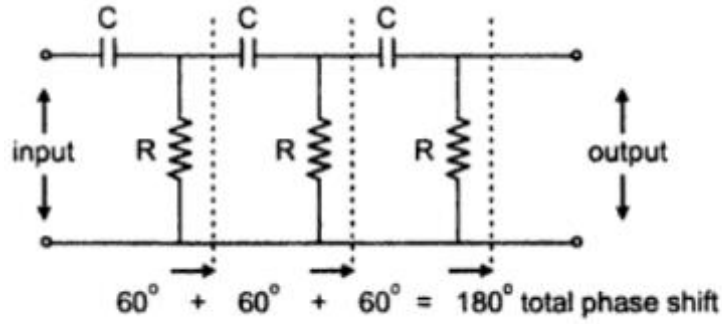
****

1. What is an oscillator? Draw and explain the working principle of RC-phase shift oscillator. (Nov-15)

Oscillator:

- Any circuit which is used to generate AC voltage without AC input signal is called an ***oscillator***
- RC phase shift oscillator basically consist of an amplifier and a feedback network consisting of resistors and capacitors arranged in ladder fashion.
- By using proper values of R & C the angle ϕ is adjusted in practice equal to 60^{o}.

- Hence in RC phase shift oscillator, the feedback network consists of three RC sections each producing a phase shift of 60^o.
- Thus total phase shift is 180^o.



Feedback network in RC phase shift oscillator

R-C Phase Shift Oscillator using Op-amp

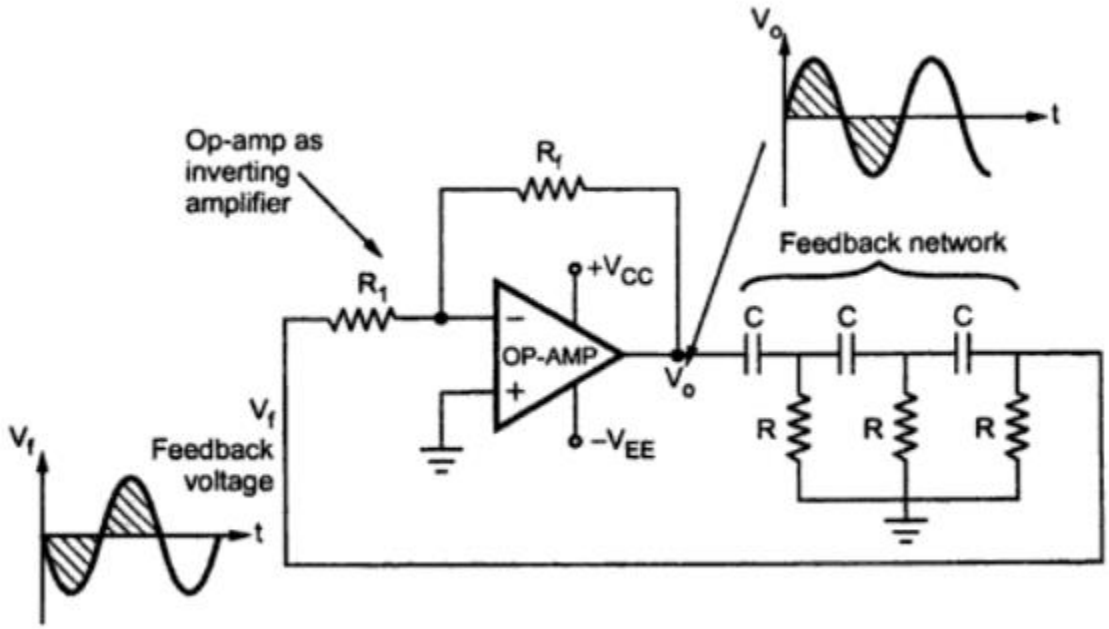


Fig. R-C Phase shift oscillator using op-amp

R-C phase shift oscillator using op-amp uses op-amp in inverting amplifier mode. Thus it introduces the phase shift of 180° between input and output. The feedback network consists of 3 RC sections each producing 60° phase shift. Such a RC phase shift oscillator using op-amp is shown in the Fig. 7.11.

The output of amplifier is given to feedback network. The output of feedback network drives the amplifier. The total phase shift around a loop is 180° of amplifier and 180° due to 3 RC section, thus 360°. This satisfies the required condition for positive feedback and circuit works as an oscillator.

The frequency of sustained oscillations generated depends on the values of R and C and is given by,

$$\boxed{f = \frac{1}{2\pi \sqrt{6}\, R\, C}}$$

The frequency is measured in Hz.

At this frequency the gain of the op-amp must be at least 29 to satisfy $A\beta = 1$.

Now gain of the op-amp inverting amplifier is given by,

$$|A| \geq \frac{R_f}{R_1} \geq 29 \text{ for oscillations}$$

$$\therefore \quad R_f \geq 29\, R_1$$

Thus circuit will work as an oscillator which will produce a sinusoidal waveform if gain is 29 and total phase shift around a loop is 360°. This satisfies the Barkhausen criterion for the oscillator. These oscillators are used over the audio frequency range i.e. about 20 Hz upto 100 kHz.

Advantages

The advantages of R-C phase shift oscillator are,

1. The circuit is simple to design.
2. Can produce output over audio frequency range.
3. Produces sinusoidal output waveform.
4. It is a fixed frequency oscillator.

Disadvantages

By changing the values of R and C, the frequency of the oscillator can be changed. But the values of R and C of all three sections must be changed simultaneously to satisfy the oscillating conditions. But this is practically impossible. Hence the phase shift oscillator is considered as a fixed frequency oscillator, for all practical purposes.

And the frequency stability is poor due to the changes in the values of various components, due to effect of temperature, aging etc.

Phase Shift Oscillator Design

Practically the resistance R_f of the inverting amplifier is designed, by making current through it, much larger than input bias current of the op-amp.

Let the current through R_f is I_1 then

$$I_1 = 100\, I_{B(max)} \quad \ldots (1)$$

Without amplitude stabilization, **the output of the oscillator oscillates between the levels $\pm V_{sat}$.**

$$\therefore \quad V_o = + V_o(sat)$$

$$\therefore \quad R_f = \frac{V_o(sat)}{I_1} \quad \ldots (2)$$

$+ V_o(sat)$ can be assumed 1 V less than $+ V_{CC}$.

Now $A_{CL} \geq 29$

$$\therefore \quad \frac{R_f}{R_1} \geq 29 \quad \ldots (3)$$

Design the value of R_1 from the gain requirement.

To prevent the loading of the amplifier because of RC networks, it is necessary that $R_1 \geq 10\ R$.

$$\therefore \quad R = \frac{R_1}{10} \quad \ldots (4)$$

Now $C = \dfrac{1}{2\pi\sqrt{6}\, f R}$ gives required value of capacitor

2. Design the phase shift oscillator to have output frequency of 500 Hz. Use ±12 V supply.

Solution : As f is less than 1 kHz, Use op-amp 741 with $I_B(max) = 50$ nA.

$$\therefore \quad I_1 = 100\ I_B(max) = 5\ \mu A$$

$$\therefore \quad R_f = \frac{V_o(sat)}{I_1} \quad \text{where } V_o(sat) = 12 - 1 = 11\ V$$

$$= \frac{11}{50\times10^{-6}} = \mathbf{2.2\ M\Omega} \text{ (standard value)}$$

$$A_{CL} = \frac{R_f}{R_1} \geq 29$$

$$\therefore \quad R_1 = \frac{R_f}{29} = \frac{220\times10^3}{29} = \mathbf{75.86\ k\Omega}$$

Use standard value of 75.86 kΩ

$$R = \frac{R_1}{10} = \frac{75.8\times10^3}{10} = \mathbf{7.5\ k\Omega} \text{ (standard value)}$$

$$\therefore \quad C = \frac{1}{2\pi\sqrt{6}\,f\,R} = \frac{1}{2\pi\sqrt{6}\times500\times7500} = \mathbf{0.017\ \mu F}$$

Use standard value of 0.017 μF

The designed circuit is shown in the Fig.

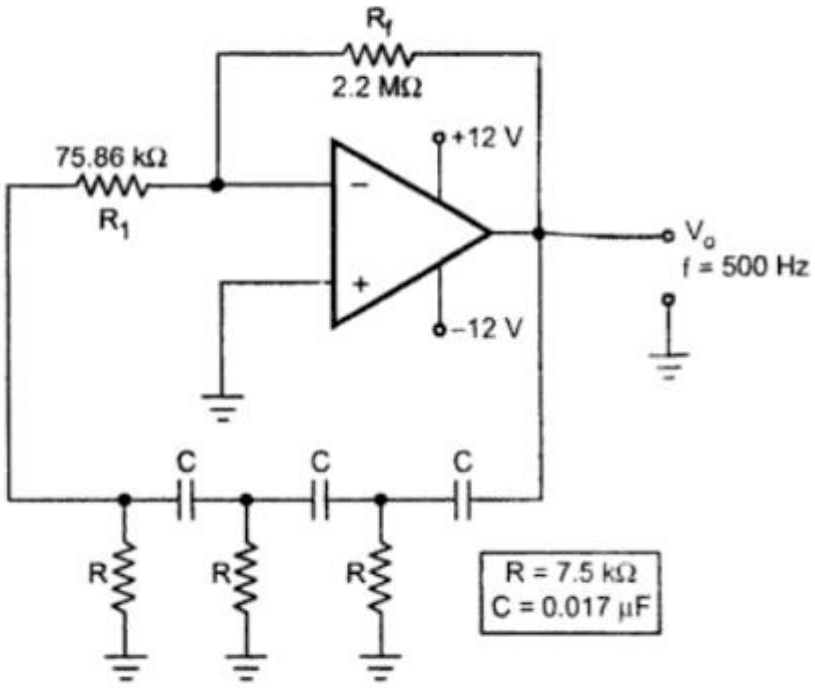


Fig.

3. Draw and explain the working principle of wein bridge oscillator.

INRODUCTION:

Generally in an oscillator, amplifier stage introduces 180° phase shift and feedback network introduces additional 180° phase shift, to obtain a phase shift of 360° (2π radians) around a loop. This is required condition for any oscillator. But Wien bridge oscillator uses a noninverting amplifier and hence does not provide any phase shift during amplifier stage. As total phase shift required is 0° or 2 nπ radians, in Wien bridge type no phase shift is necessary through feedback. Thus the total phase shift around a loop is 0°.

Wien Bridge Oscillator using Op-amp

If the amplifier circuit using transistors is replaced by the amplifier circuit using op-amp, with basic feedback network remains as the Wien bridge circuit, the oscillator is called Wien bridge oscillator using op-amp. The Fig. shows the Wien bridge circuit using op-amp.

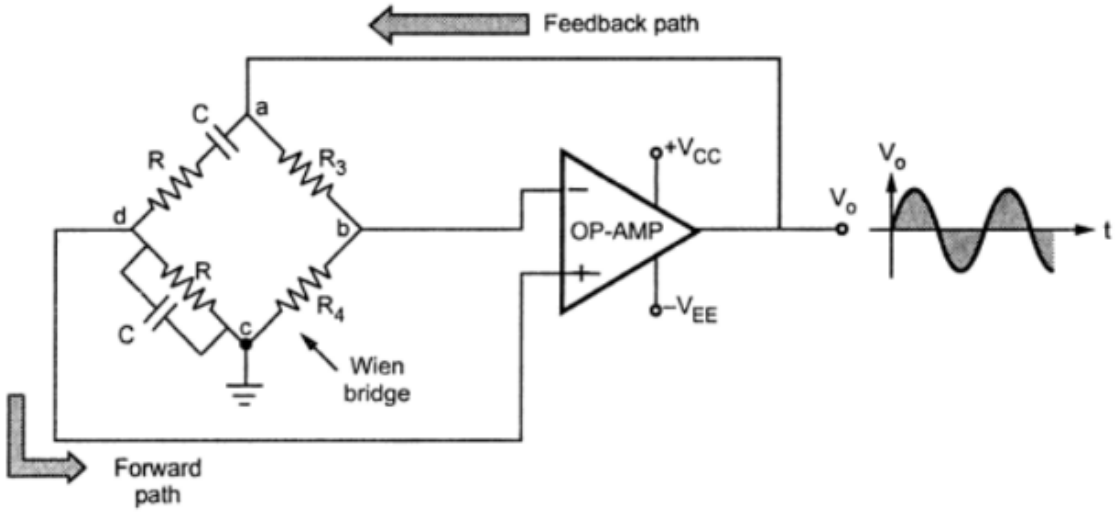


Fig. Wien bridge oscillator using op-amp

The resistance R and capacitor C are the components of frequency sensitive arms of the bridge. The resistance R_3 and R_4 form the part of the feedback path. The op-amp output is connected to bridge input points a and c while bridge output points b and d are connected to the op-amp input. The gain of the op-amp can be adjusted by using the resistances R_3 and R_4. The gain of the op-amp is given by,

$$A = 1 + \frac{R_3}{R_4}$$

According to the oscillating conditions, $A \geq 3$.

$$\therefore \quad 1 + \frac{R_3}{R_4} \geq 3$$

$$\therefore \quad \frac{R_3}{R_4} \geq 2$$

Thus the ratio of R_3 and R_4 greater than or equal to two, will provide sufficient loop gain for the circuit to oscillate at the frequency calculated as,

$$f = \frac{1}{2\pi RC}$$

The simplified circuit diagram of the Wien bridge oscillator is shown in the Fig.

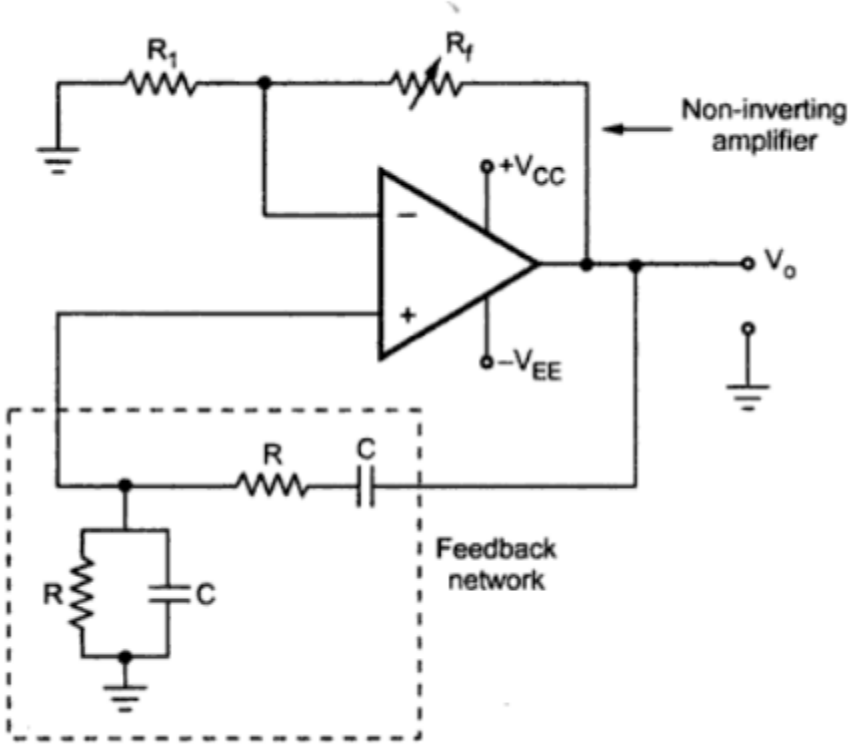


Fig. Simplified diagram of Wien bridge oscillator

Advantages

The various advantages of Wien bridge oscillator are,

1. By varying the two capacitor values simultaneously, by mounting them on the common shaft, different frequency ranges can be obtained.
2. The perfect sine wave output is possible.
3. It is useful audio frequency range i.e. 20 Hz to 100 kHz.

Wien Bridge Oscillator Design

Select the capacitor value much larger than the stray capacitance, about 0.01 to 0.05 µF.

From the equation of frequency, obtain the value of R.

$$R = \frac{1}{2\pi fC}$$

Then for noninverting amplifier,

$$R_f = 2\,R_1$$

Choose R_1 and design the value of R_f . Keep R_f variable for fine adjustments.

4. Design the wein bridge oscillator to have output frequency of 10 KHz.

Solution : Choose C = 0.01 μF

$$\therefore \quad R = \frac{1}{2\pi f C} = \frac{1}{2\pi \times 10 \times 10^{3} \times 0.01 \times 10^{-6}} = \mathbf{1.5915\ k\Omega}$$

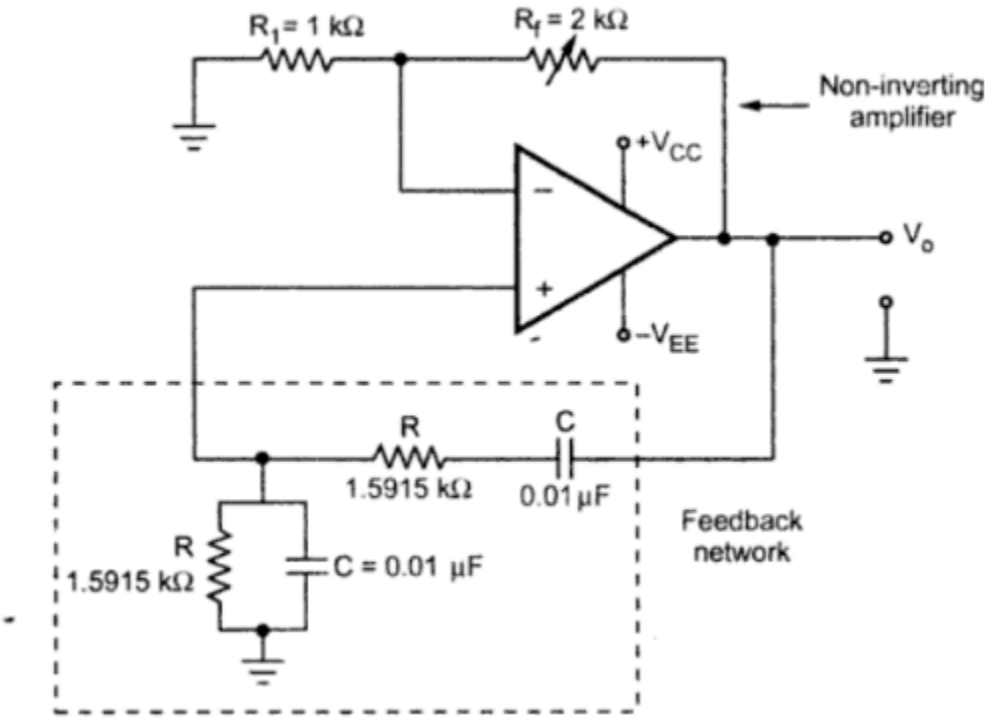
Choose standard value of 1.5 kΩ

Now $R_f = 2\ R_1$

Choose $R_1 = \mathbf{1\ k\Omega}$

$\therefore \quad R_f = \mathbf{2\ k\Omega}$

Use standard value of 2.2 kΩ to have $A_{CL} > 3$. The designed circuit is shown



5. Draw and explain the working principle AstableMultivibrator using OPAMP.

Astable Multivibrator using Op-amp (Square Wave Generator)

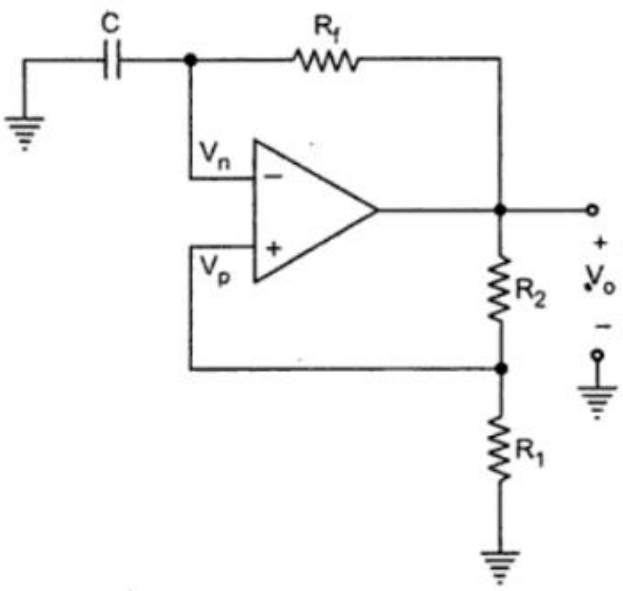


Fig. 4.57 Astable multivibrator using op-amp

In this section we are going to study astable multivibrator operation using op-amp. Fig. 4.57 shows astable multivibrator circuit using op-amp. It looks like a comparator with hysteresis (schmitt trigger), except that the input voltage is replaced by a capacitor. The circuit has a time dependent elements such as resistance and capacitor to set the frequency of oscillation.

As shown in the Fig. 4.57 the comparator and positive feedback resistors R_1 and R_2 form an inverting schmitt trigger.

When V_o is at $+V_{sat}$, the feedback voltage is called the upper threshold voltage V_{UT} and is given as

$$V_{UT} = \frac{R_1 \cdot (+V_{sat})}{R_1 + R_2} \quad \ldots (1)$$

When V_o is at $-V_{sat}$, the feedback voltage is called the lower-threshold voltage V_{LT} and is given as

$$V_{LT} = \frac{R_1 \cdot (-V_{sat})}{R_1 + R_2} \quad \ldots (2)$$

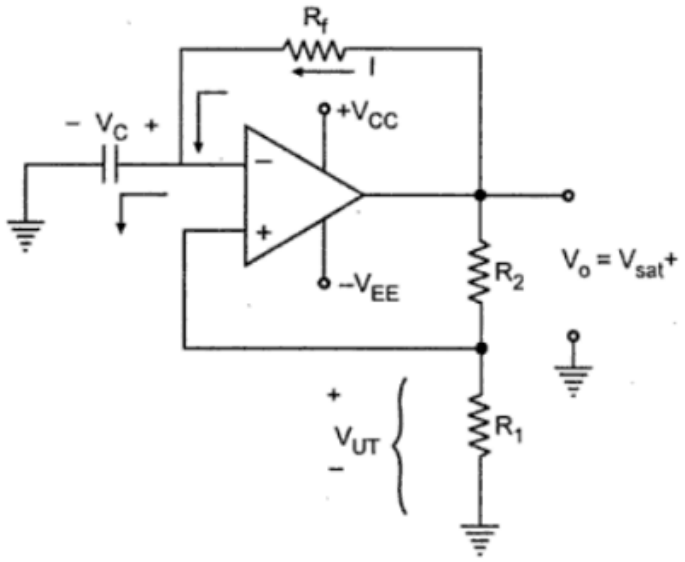


Fig. 4.58 (a) When $V_o = +V_{sat}$, capacitor charges towards V_{UT}

When power is turn ON, V_o automatically swings either to $+V_{sat}$ or to $-V_{sat}$ since these are the only stable states allowed by the schmitt trigger. Assume it swings to $+V_{sat}$. With $V_o = +V_{sat}$ we have $V_p = V_{UT}$ and capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting (–) input. This is illustrated in Fig. 4.58 (a). As long as the capacitor voltage V_C is less than V_{UT}, the output voltage remains at $+V_{sat}$.

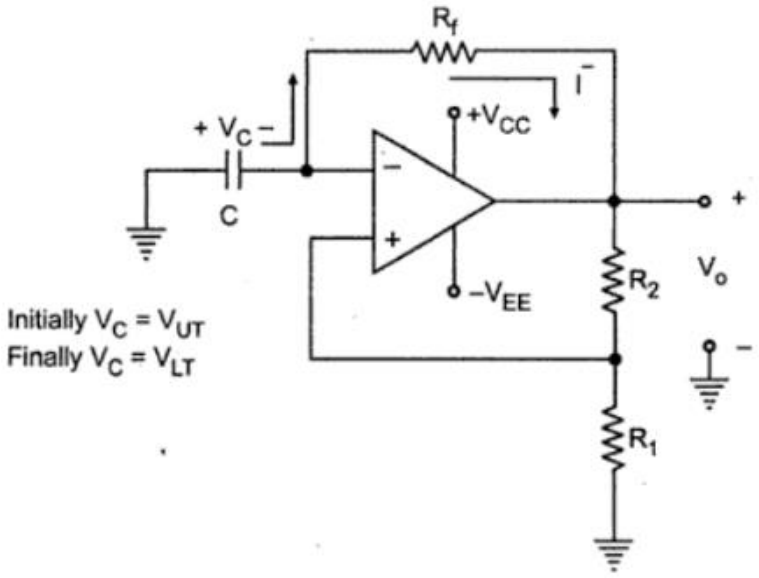


Fig. 4.58 (b) When $V_o = -V_{sat}$, capacitor charges towards V_{LT}

As soon as V_C charges to a value slightly greater than V_{UT}, the (–) input goes positive with respect to the (+) input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$ and we have $V_p = V_{LT}$, which is negative with respect to ground. As V_o switches to $-V_{sat}$, capacitor starts discharging via R_f, as shown in the Fig. 4.58 (b).

The current I^- discharges capacitor to 0 V and recharges capacitor to V_{LT}. When V_C becomes slightly more negative than the feedback voltage V_{LT}, output voltage V_o switches back to $+V_{sat}$. As a result, the condition in Fig. 4.58 (a) is reestablished except that capacitor now has a initial charge equal to V_{LT}. The capacitor will discharge from V_{LT} to 0V and then recharge to V_{UT}, and the process is repeating. Once the initial cycle is completed, the waveforms become periodic, as shown in the Fig. 4.58 (c).

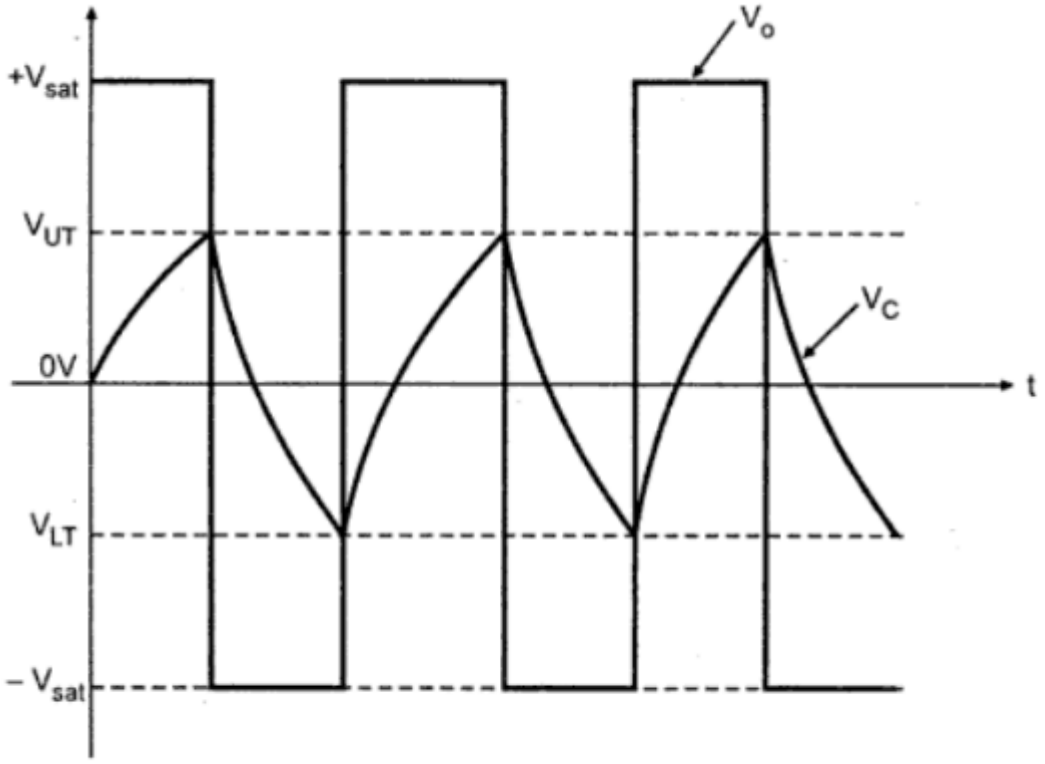


Fig. 4.58 (c) Waveforms

4.20.1 Frequency of Oscillation

The frequency of oscillation is determined by the time it takes the capacitor to charge from V_{UT} to V_{LT} and vice versa. The voltage across the capacitor as a function of time is given as

$$V_C(t) = V_{max} + (V_{initial} - V_{max})e^{(-t/T)} \quad \ldots (3)$$

where $V_C(t)$ is the instantaneous voltage across the capacitor.

$V_{initial}$ is the initial voltage

V_{max} is the voltage toward which the capacitor is charging.

Let us consider the charging of capacitor from V_{LT} to V_{UT}, where V_{LT} is the initial voltage, V_{UT} is the instantaneous voltage and $+V_{sat}$ is the maximum voltage. At $t = T_1$, voltage across capacitor reaches V_{UT} and therefore equation (3) becomes

$$V_{UT} = +V_{sat} + (V_{LT} - +V_{sat})e^{(-T_1/R_f C)} \quad \ldots (4)$$

$$\therefore -(V_{LT} - +V_{sat})e^{(-T_1/R_f C)} = +V_{sat} - V_{UT}$$

$$\therefore -(V_{LT} - +V_{sat})e^{(-T_1/R_f C)} = +V_{sat} - V_{UT}$$

$$\therefore \quad e^{(-T_1/R_f C)} = \frac{(+V_{sat} - V_{UT})}{(+V_{sat} - V_{LT})}$$

$$\therefore \quad \frac{-T_1}{R_f C} = ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$\therefore \quad T_1 = -R_f C\, ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$= R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \quad \ldots (5)$$

The time taken by capacitor to charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT}. Therefore, total time required for one oscillation is given as

$$T = 2T_1 \quad \ldots (6)$$

$$\therefore \quad \boxed{T = 2R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)} \quad \ldots (7)$$

The frequency of oscillation can be determined as $f_o=1/T$, where T represents the time required for one oscillation.

Substituting the value of T we get,

$$\boxed{f_o = \frac{1}{2R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)}} \quad \ldots (8)$$

Substituting the values of V_{UT} and V_{LT} we get,

$$T = 2R_f C ln\left[\frac{+V_{sat} - (R_1 \times - V_{sat})/R_1 + R_2}{+V_{sat} - (R_1 \times + V_{sat})/R_1 + R_2}\right]$$

If magnitudes of $+ V_{sat}$ and $- V_{sat}$ are equal,

$$T = 2R_f C \ ln\left[\frac{+V_{sat}\left(1+\frac{R_1}{R_1+R_2}\right)}{+V_{sat}\left(1-\frac{R_1}{R_1+R_2}\right)}\right]$$

$$\therefore \quad \boxed{T = 2R_f C \ ln\left(\frac{2R_1+R_2}{R_2}\right)}$$

6. Draw and explain generation of sawtooth waveform using OPAMP.

Sawtooth Wave Generator

Unlike triangular wave, sawtooth wave has unequal rise time and fall time. That is, it may fall negatively many times faster than it rises positively, or vice versa. The sawtooth wave generator can be implemented by slightly modifying the triangular wave generator, as shown in the Fig. 6.9.

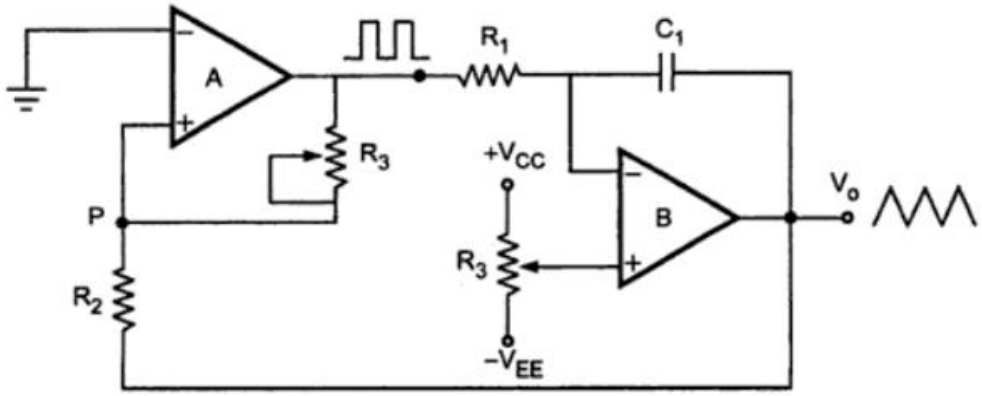


Fig. 6.9 Sawtooth wave generator

Here, noninverting terminal (+ input) of the integrator is driven by the voltage set between $+V_{CC}$ to $-V_{EE}$ by the potentiometer. Depending on the R_4 setting, a certain d.c. level is added in the output of the integrator B. As output voltage of the integrator decides the effective voltage at point P, added d.c. level in the output of the integrator will affect the duty cycle of the comparator output. When voltage at the noninverting input of the integrator is negative, the duty cycle is less than 50 % resulting longer rise time than the fall time as shown in the Fig. 6.10. On the other hand, when voltage at the noninverting input of the integrator is positive, the duty cycle is greater than 50 % and rise time is less than the fall time.

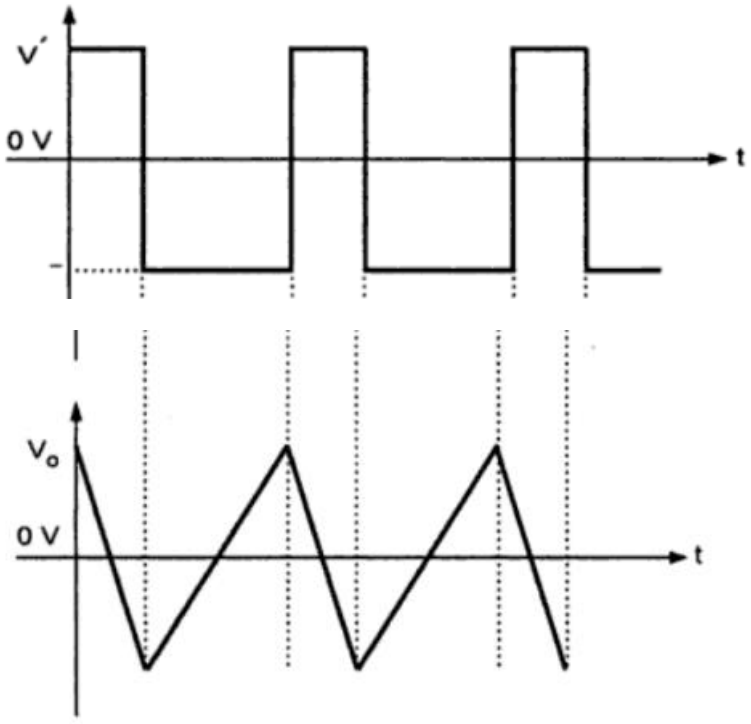


Fig. 6.10 Waveforms of sawtooth wave generator

It is important to note that the frequency of the sawtooth waveform decreases when voltage at the noninverting input of the integrator B is adjusted towards $+V_{CC}$ or $-V_{EE}$. However, the amplitude of the sawtooth wave is independent of the voltage setting at the noninverting input of the integrator B.

7. Explain in detail about state variable filter.

State Variable Filters (SV Filters)

In 1967, **W.J. Kerwin, L.P. Huelsman** and **R.W. Newcomb** developed first state variable filter using two integrators and one summing amplifier. This filter is also called **KHN filter**. This KHN filter provides second order responses of low pass, band pass and high pass filters. Moreover by using fourth op-amp, the three responses can be combined to obtain responses for notch filter and all pass filters. Thus inturn such KHN filter is said to be universal filter as it provides second order response of all the types of filters like low pass, high pass, band pass, notch and all pass.

A typical KHN filter using op-amps in inverting mode is as shown in the Fig. 3.46.

Using principle of superposition for linear inputs, we can write,

$$V_{0HP} = -\frac{R_5}{R_3} V_{in} - \frac{R_5}{R_4} V_{0LP} + \left[1+\frac{R_5}{(R_3 \| R_4)}\right]\left[\frac{R_1}{R_1+R_2}\right] V_{0BP}$$

Simplifying above expression, we get

$$V_{0HP} = -\frac{R_5}{R_3} V_{in} - \frac{R_5}{R_4} V_{0LP} + \left[\frac{1+\frac{R_5}{R_3}+\frac{R_5}{R_4}}{\left(1+\frac{R_2}{R_1}\right)}\right] V_{0BP} \quad \ldots(1)$$

But op-amp 2 is integrator, so we can write,

$$V_{0BP} = \frac{-1}{sR_6C_1} V_{0HP} \quad \ldots(2)$$

Similarly op-amp 3 is also an integrator, hence we can write,

$$V_{0LP} = \frac{-1}{sR_7C_2} V_{0BP} \quad \ldots(3)$$

Substituting value of V_{0BP} from equation (2) in (3), we get

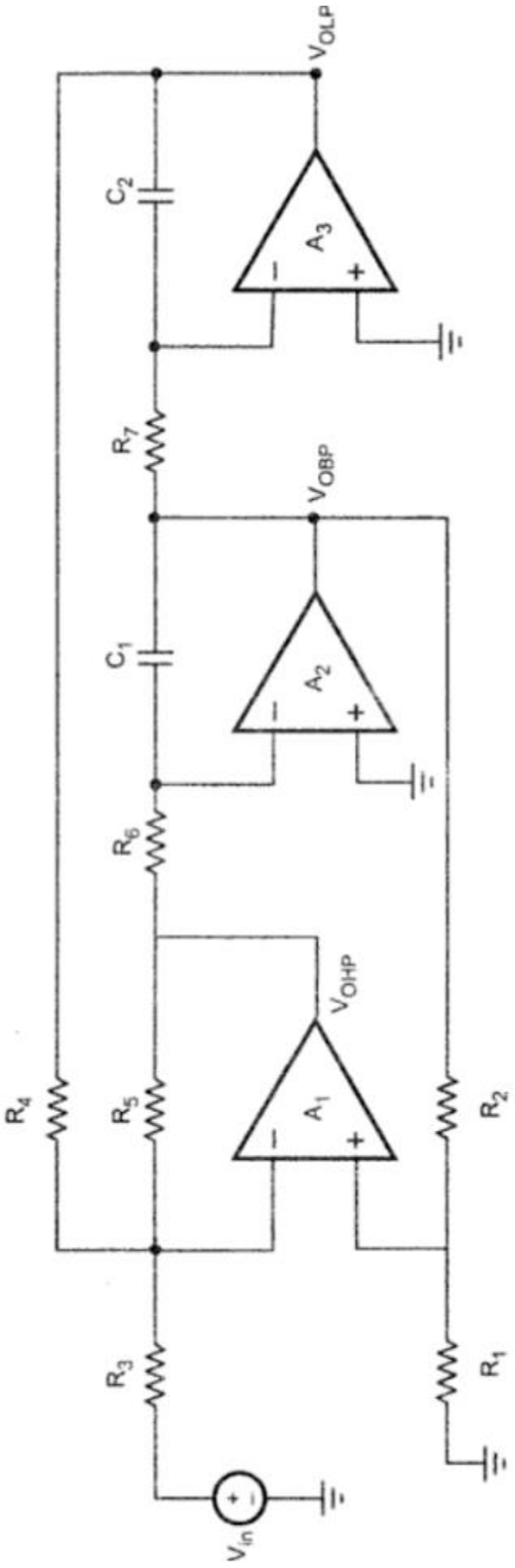
$$V_{0LP} = \frac{-1}{sR_7C_2}\left[\frac{-1}{sR_6C_1} V_{0HP}\right]$$

$$\therefore \quad V_{0LP} = \frac{1}{s^2(R_6C_1R_7C_2)} V_{0HP} \quad \ldots(4)$$

Substituting values of V_{0BP} and V_{0LP} in equation (1), we get

$$V_{0HP} = -\frac{R_5}{R_3} V_{in} - \frac{R_5}{R_4}\left[\frac{1}{s^2R_6C_1R_7C_2} \times V_{0HP}\right] + \left[\frac{1+\frac{R_5}{R_3}+\frac{R_5}{R_4}}{\left(1+\frac{R_2}{R_1}\right)}\right]\left[\frac{-1}{sR_6C_1}\right] V_{0HP}$$

Collecting V_{0HP} terms and rearranging terms, we get,



State variable or KHN filter of inverting type

$$\frac{V_{0HP}}{V_{in}} = T_{0HP}\, T_{HP}$$

Then,

$$T_{0HP} = -\frac{R_5}{R_3}$$

$$\omega_0 = \frac{\sqrt{R_5 / R_4}}{\sqrt{R_6 C_1 R_7 C_2}} \qquad \ldots (6)$$

$$Q = \frac{\left(1+\frac{R_2}{R_1}\right)\sqrt{R_5 R_6 C_1 / R_4 R_7 C_2}}{1+\frac{R_5}{R_4}+\frac{R_5}{R_3}}$$

Dividing equation (2) by V_{in} on both the sides, we get,

$$\frac{V_{0BP}}{V_{in}} = \frac{-1}{sR_6C_1}\,\frac{V_{0HP}}{V_{in}}$$

This equation can be expressed as,

$$\frac{V_{0BP}}{V_{in}} = T_{0BP}\, T_{BP}$$

Then

$$T_{0BP} = \frac{1+R_2 / R_1}{1+\frac{R_3}{R_4}+\frac{R_3}{R_5}} \qquad \ldots (7)$$

Similarly dividing equation (3) by V_{in} on both the sides, we get,

$$\frac{V_{0LP}}{V_{in}} = \frac{1}{s^2(R_6C_1R_7C_2)}\,\frac{V_{0HP}}{V_{in}} = T_{0LP}\, T_{LP}$$

Then

$$T_{0LP} = -\frac{R_4}{R_3} \qquad \ldots (8)$$

But in general for SV filters, the components selected are

$$R_5 = R_4 = R_3 = R_6 = R_7 = R$$

and

$$C_1 = C_2 = C$$

Then design equations can be written as,

$$\omega_0 = \frac{1}{RC} \quad , \quad Q = \frac{1}{3}\left(1+\frac{R_2}{R_1}\right) \qquad \ldots(9)$$

$$T_{0HP} = -1 \quad , \quad T_{0BP} = Q \quad , \quad T_{0LP} = -1$$

The procedure of tunning universal or state variable filter is as given below.

i) For the required magnitude response, adjust R_3.

ii) Tune desired value of ω_0 adjusting either R_6 or R_7.

iii) Tunning of Q is done by adjusting ratio $\frac{R_2}{R_1}$.

8. Explain in detail about switched capacitor filter.

Basic Operation of Switched Capacitor Filter

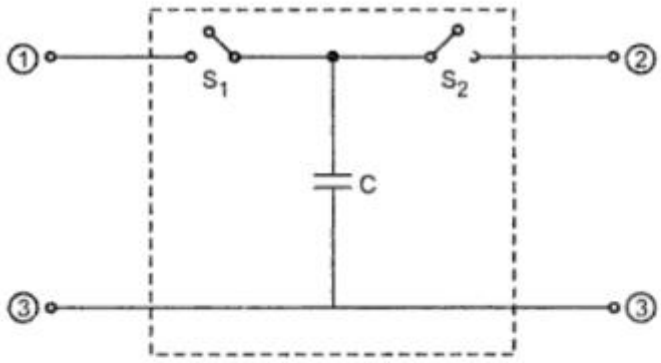


Fig. Block schematic of switched capacitor filter

A switched capacitor filter is a three terminal device which consists of capacitor and MOS switches. The block schematic of switched capacitor filter is shown in the Fig. 3.99. The S_1 and S_2 are the two MOS switches and C is the capacitor. The three terminals are marked as 1, 2 and 3. The terminal 3 is common at input and output and generally grounded.

The two switches operated alternately and a capacitor C together is used to simulate high value resistors. Let us see the simulation of a resistor using capacitor and the two switches.

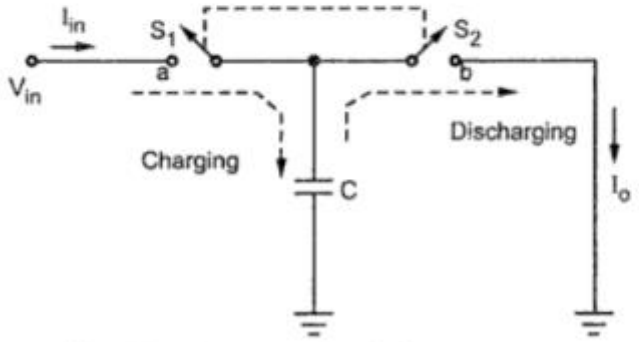


Fig. Resistance simulation

Consider a circuit using a basic switched capacitor filter, as shown in the Fig. 3.100. The two switches S_1 and S_2 are the MOS transistors which are alternately opened and closed. Thus when S_1 is closed, S_2 is open and vice versa.

The switches are opened and closed alternately by using an external clock with a frequency f_{CLK}.

Consider the switch S_1 is in position 'a' i.e. it is closed. So capacitor C gets charged to voltage V_{in}. Hence the total charge on the capacitor is,

$$Q = C V_{in} \quad \ldots (1)$$

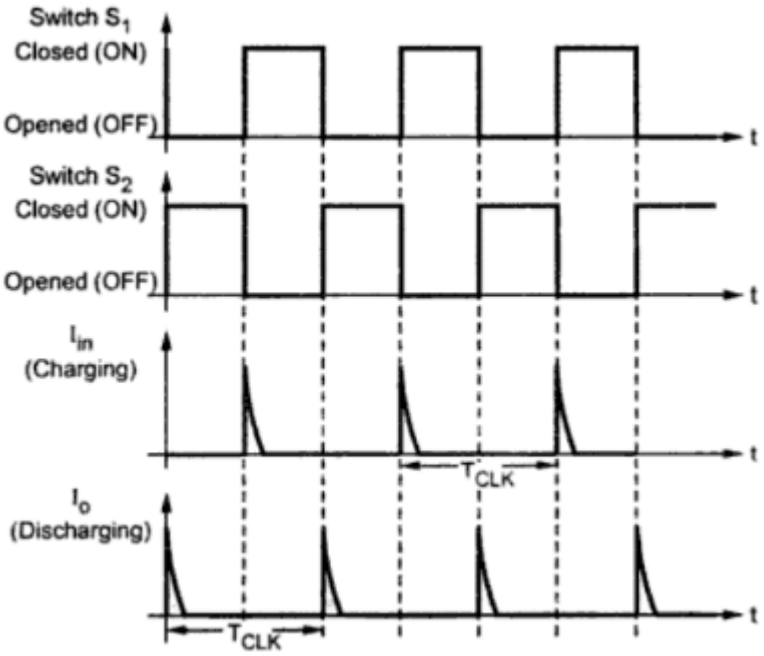
When S_1 is open and S_2 is in position 'b' i.e. closed then the capacitor C discharges and charge Q flows to the ground.

If the switches are ideal i.e. they open and close instantaneously and resistance of the switches is zero when they are closed then charging and discharging of the capacitor takes place instantly.

So let, I_{in} = Charging current

and I_o = Discharging current

Then when S_1 is closed, I_{in} flows instantly whose amplitude depends on charge Q flowing per unit time. Hence I_{in} occurs in pulse form, at the instants when S_1 is closed. While when S_2 is closed, I_o occurs in pulse form. So the capacitor current consists of short bursts every time when switch is closed. The waveforms of I_{in} and I_o, related to the closing and opening of switches are shown in the Fig.



Input and output current waveforms for switched capacitor filter

The time between closing of switch S_1 or S_2 is called clock time, denoted as T_{CLK}. This can be controlled by an external clock.

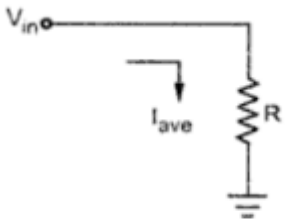
Thus if switches are opened and closed at a faster rate, then frequency of occurrence of current pulses will be high but their amplitudes will remain unchanged. But due to frequent occurrence of current pulses, the average current flowing will be more for higher switching rate. This average current is rate of change of flux with respect to the clock time T_{CLK}.

$$\therefore \quad I_{ave} = \frac{Q}{T_{CLK}} \qquad \ldots (2)$$

From equation (2), $I_{ave} = \frac{C V_{in}}{T_{CLK}} = C V_{in} f_{CLK}$

$$\therefore \quad \boxed{\frac{V_{in}}{I_{ave}} = \frac{1}{C f_{CLK}}} \qquad \ldots (3)$$

where $f_{CLK} = \frac{1}{T_{CLK}}$ = Clock frequency



Consider a resistance to which voltage V_{in} is applied, which drives average current I_{ave}, through the resistor. This is shown in the Fig. 3.102.

Fig. 3.102

According to Ohm's law,

$$\boxed{\frac{V_{in}}{I_{ave}} = R} \qquad \ldots (4)$$

Comparing (3) and (4), it can be concluded that the switched capacitor filter can be effectively used to simulate the resistors. The value of the resistor it is simulating, can be written as,

$$R = \frac{1}{C f_{CLK}} \quad \ldots (5)$$

Key Point: *Thus R is a function of capacitor C and the external clock frequency.*

The capacitor C is constant hence the value of R can be adjusted as per the requirement, by controlling the external clock frequency f_{CLK}.

Advantages of Switched Capacitor Filter

1. Very high value of resistors can be easily simulated using small value capacitors, of the order of 10 pF.
2. The switched capacitor filters require no external reactive components like inductors and capacitors.
3. Complete active filters can be easily obtained on a monolithic IC chip.
4. The cut-off frequencies of the filters are proportional to the external clock frequency of switched capacitor filter. Hence can be easily controlled.
5. The cut-off frequencies of switched capacitor filters can be programmed so as to obtain within very high range of frequencies, of the order of 200000 : 1 range.
6. Accuracy is very high.
7. The overall cost of the system is low.
8. Due to good temperature characteristics, the systems have good temperature stability.

9. Explain in detail about design of First order low pass filter.

First Order Low Pass Butterworth Filter

The first order low pass butterworth filter is realised by R-C circuit used along with an op-amp, used in the noninverting configuration. The circuit diagram is shown in Fig. 6.64.

This also called **one pole low pass Butterworth filter.**

The resistances R_f and R_1 decide the gain of the filter in the pass band.

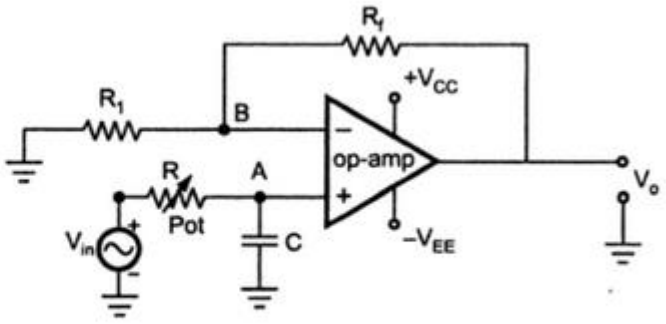


Fig. 6.64 First order low pass Butterworth filter

Analysis of the Filter Circuit

The impedance of the capacitor C is $-jX_C$ where X_C is the capacitive reactance given by $X_C = \frac{1}{2\pi fC}$.

By the potential divider rule, the voltage at the non-inverting input terminal A which is the voltage across capacitor C is given by,

$$V_A = \frac{-jX_C}{R - jX_C} \cdot V_{in} \quad \ldots (1)$$

$$\therefore \quad V_A = \frac{-j\left(\frac{1}{2\pi fC}\right)}{R - j\left(\frac{1}{2\pi fC}\right)} \cdot V_{in} = \frac{-j}{2\pi fRC - j} \cdot V_{in}$$

$$= \frac{V_{in}}{1 - \frac{2\pi fRC}{j}}$$

but $\quad -j = \frac{1}{j} \quad$ and $\quad -\frac{1}{j} = j$

$$\therefore \quad V_A = \frac{V_{in}}{1 + j2\pi fRC} \quad \ldots (2)$$

As the op-amp is in the non-inverting configuration,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_A \quad \ldots (3)$$

$$V_o = \left(1 + \frac{R_f}{R_1}\right) \frac{V_{in}}{(1 + j2\pi fRC)}$$

i.e. $$\frac{V_o}{V_{in}} = \frac{A_F}{1 + j\left(\frac{f}{f_H}\right)} \quad \ldots (4)$$

where $$A_F = \left(1 + \frac{R_f}{R_1}\right) = \text{Gain of filter in pass band} \quad \ldots (5)$$

and $$f_H = \frac{1}{2\pi RC} = \text{High cut-off frequency of filter} \quad \ldots (6)$$

and f = operating frequency

The $\frac{V_o}{V_{in}}$ is the transfer function of the filter and can be expressed in the polar form as,

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

where

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^2}} \quad \ldots (7)$$

and

$$\phi = -\tan^{-1}\left(\frac{f}{f_H}\right) \quad \ldots (8)$$

The phase angle ϕ is in degrees.

The equation (7) describes the behaviour of the low pass filter.

1. At very low frequencies, $f < f_H$

$$\left|\frac{V_o}{V_{in}}\right| \cong A_F \text{ i.e. constant}$$

2. At $f = f_H$,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{2}} = 0.707\ A_F \quad \text{i.e. 3 dB down to the level of } A_F.$$

3. At $f > f_H$

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

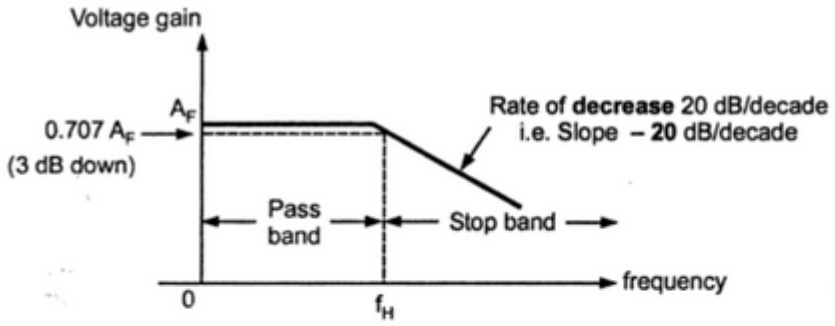


Fig. 6.65 Frequency response

Thus, for the range of frequencies, $0 < f < f_H$, the gain is almost constant equal to f_H which is high cut-off frequency. At $f = f_H$, gain reduces to 0.707 A_F i.e. 3 dB down from A_F. And as the frequency increases than f_H, the gain decreases at a rate of 20dB/decade. The rate 20 dB/decade means decrease of 20 dB in gain per 10 times change in frequency. The same rate can be expressed as 6 dB/octave i.e. decrease of 6 dB per two times change in the frequency. The frequency f_H is called **cut off frequency, break frequency, – 3dB frequency** or **corner frequency**. The frequency response is shown in the Fig. 6.65.

Design Steps

The design steps for the first order low pass Butterworth filter are

1) Choose the cut off frequency, f_H.
2) Choose the capacitance C usually betwen 0.001 and 1 μF. Generally, it is selected as 1 μF or less than that. For better performance, mylar or tantalum capacitors are selected.
3) Now, for the RC circuit,

$$f_H = \frac{1}{2\pi RC}$$ refer equation (8)

Hence, as f_H and C are known, calculate the value of R.

4) The resistances R_f and R_1 can be selected depending on the required gain in the pass band.

$$A_F = 1 + \frac{R_f}{R_1}$$

10.Explain in detail about design of First order high pass filter.

First Order High Pass Butterworth Filter

As mentioned earlier, a high pass filter is a circuit that attenuates all the signals below a specified cut-off frequency denoted as f_L. Thus, a high pass filter performs the opposite function to that of low pass filter. Hence, the high pass filter circuit can be obtained by interchanging frequency determining resistances and capacitors in low pass filter circuit.

The first order high pass filter can be obtained by interchanging the elements R and C in a first order low pass filter circuit. The Fig. 6.67 shows the first order high pass Butterworth filter.

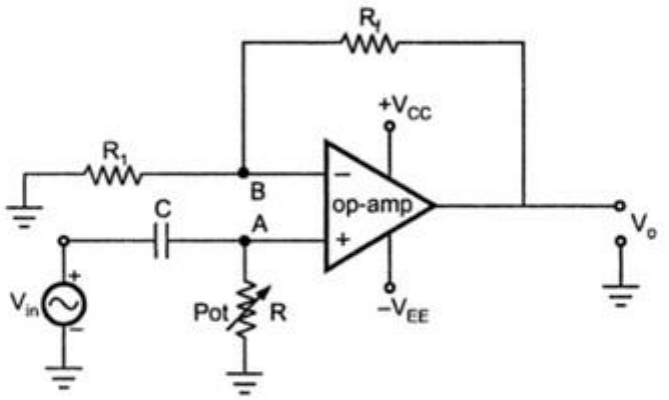


Fig. 6.67 First order high pass Butterworth filter

It can be observed that as compared to first order low pass filter (Fig. 6.64), the positions of R and C are changed in the high pass circuit shown in Fig. 6.67.

The frequency at which the gain is 0.707 times the gain of filter in pass band is called **low cut-off frequency** and denoted as f_L. So, all the frequencies greater than f_L are allowed to pass but the maximum frequency which is allowed to pass is determined by the closed loop bandwidth of the op-amp used.

Analysis of the Filter Circuit

The impedance of the capacitor is $-j X_C = -j\left(\frac{1}{2\pi f C}\right)$ where f is the input i.e. operating frequency.

By the voltage divider rule, the potential of the non-inverting terminal of the op-amp is,

$$V_A = V_{in}\left[\frac{R}{R - j X_C}\right] \qquad \ldots (1)$$

$$\therefore \quad V_A = V_{in}\left[\frac{R}{-j X_C\left(\frac{R}{-j X_C} + 1\right)}\right] \qquad \text{taking } -j X_C \text{ outside}$$

As $-\frac{1}{j} = j$, we can write,

$$\frac{1}{-j X_C} = \frac{j}{X_C} = \frac{j}{\left(\frac{1}{2\pi f C}\right)} = j\,2\pi f C \qquad \ldots (2)$$

Substituting in the above expression of V_A,

$$\therefore \quad V_A = V_{in}\left[\frac{\left(-\frac{R}{jX_C}\right)}{\left(-\frac{R}{jX_C}\right)+1}\right]$$

$$\therefore \quad V_A = V_{in}\left[\frac{j2\pi fRC}{1+j2\pi fRC}\right] \qquad \ldots (3)$$

This can be represented as,

$$\therefore \quad V_A = V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

where $f_L = \frac{1}{2\pi RC}$ = Low cut-off frequency ... (4)

Now, for the op-amp in non-inverting configuration,

$V_o = A_F V_A$

where V_A = Voltage at the non-inverting input

and $A_F = \left(1+\frac{R_f}{R_1}\right)$ = Gain of op-amp in pass band

Now, for the op-amp in non-inverting configuration,

$V_o = A_F V_A$

where V_A = Voltage at the non-inverting input

and $A_F = \left(1+\frac{R_f}{R_1}\right)$ = Gain of op-amp in pass band

$$\therefore \quad V_o = A_F V_{in}\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]$$

$$\therefore \quad \boxed{\frac{V_o}{V_{in}} = A_F\left[\frac{j\left(\frac{f}{f_L}\right)}{1+j\left(\frac{f}{f_L}\right)}\right]} \qquad \ldots. (5)$$

This is the required expression for the transfer function of the filter.

For the frequency response, we require the magnitude of the transfer function which is given by,

$$\boxed{\frac{V_o}{V_{in}} = \frac{A_F\left(\frac{f}{f_L}\right)}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}}} \qquad \ldots. (6)$$

The equation (6) describes the behaviour of the high pass filter.

1) At low frequencies, i.e. $f < f_L$

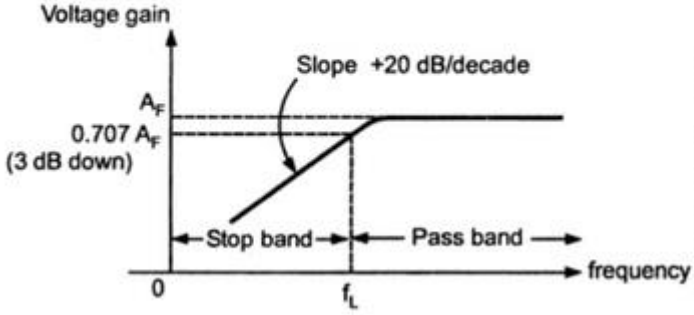
$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

2) At $f = f_L$,

$$\left|\frac{V_o}{V_{in}}\right| = 0.707\ A_F$$ i.e. 3 dB down from the level of A_F

3) At $f > f_L$, i.e. high frequencies, 1 can be neglected as compared to $\left(\frac{f}{f_L}\right)$ from denominator.

$$\therefore \quad \left|\frac{V_o}{V_{in}}\right| \cong A_F$$ i.e. constant



Thus, the circuit acts as high pass filter with a passband gain as A_F. For the frequencies, $f < f_L$, the gain increases till $f = f_L$ at a rate of +20dB/decade. Hence, the slope of the frequency response in stop band is + 20 dB/decade for first order high pass filter.

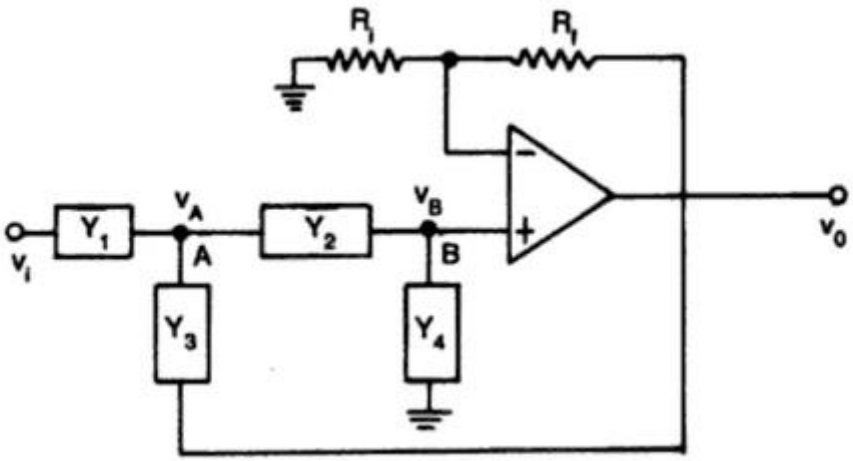
11.Explain in detail about design of Second order low pass filter.

Second Order Active Filter

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two *RC* pairs and has a roll-off rate of – 40 dB/decade. A general second order filter (Sallen-Key filter) is shown in Fig. 7.3. The results derived here can be used for analysing low pass and high pass filters.

The op-amp is connected as non-inverting amplifier and hence,

$$v_o = \left(1 + \frac{R_f}{R_i}\right) v_B = A_o v_B \tag{7.13}$$



where $$A_o = 1 + \frac{R_f}{R_i} \tag{7.14}$$

and v_B is the voltage at node *B*.

Kirchhoff's current law (KCL) at node A gives

$$v_i Y_1 = v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - v_B Y_2$$

$$= v_A (Y_1 + Y_2 + Y_3) - v_o Y_3 - \frac{v_o Y_2}{A_o} \tag{7.15}$$

where v_A is the voltage at node *A*.

KCL at node *B* gives,

$$v_A Y_2 = v_B(Y_2 + Y_4) = \frac{v_o(Y_2 + Y_4)}{A_o}$$

$$v_A = \frac{v_o(Y_2 + Y_4)}{A_o Y_2} \tag{7.16}$$

Substituting Eq. (7.16) in Eq. (7.15) and after simplification, we get the voltage gain as

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4 (Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \tag{7.17}$$

To make a low pass filter, choose, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = sC$ as shown in Fig. 7.4. For simplicity, equal components have been used.

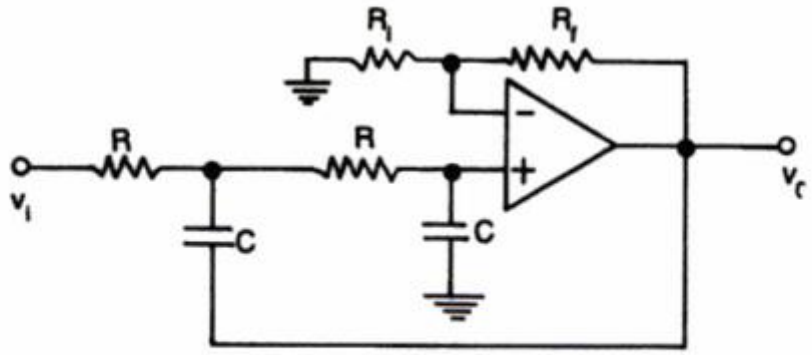


Fig. 7.4 Second order low-pass filter

From Eq. (7.17), we get the transfer function $H(s)$ of a low pass filter as,

$$H(s) = \frac{A_o}{s^2 C^2 R^2 + sCR(3 - A_o) + 1} \tag{7.18}$$

This is to note that from Eq. (7.18), $H(0) = A_o$ for $s = 0$ and $H(\infty) = 0$ for $s = \infty$ and obviously the configuration is for low pass active filter. It may be noted that for minimum dc offset $R_i R_f/(R_f + R_i) = R + R = 2R$ should be satisfied.

Second order physical systems have been studied extensively since long back and their step response, damping coefficient and its cause and effect relationship are known. We shall exploit those ideas in case of second order RC active filter. The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as,

$$H(s) = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \tag{7.19}$$

where A_o = the gain
ω_h = upper cut-off frequency in radians/second
α = damping coefficient

Comparing Eq. (7.18) and Eq. (7.19) we get,

$$\omega_h = \frac{1}{RC} \tag{7.20}$$

$$\alpha = (3 - A_o) \tag{7.21}$$

That is, the value of the damping coefficient α for low pass active *RC* filter can be determined by the value of A_o chosen.

Putting $s = j\omega$ in Eq. (7.19) we get

$$H(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2 + j\alpha(\omega/\omega_h) + 1} \tag{7.22}$$

the normalized expression for low pass filter is

$$H(j\omega) = \frac{A_o}{s^2 + \alpha s + 1} \tag{7.23}$$

where normalized frequency $s = j\left(\frac{\omega}{\omega_h}\right)$

The expression of magnitude in dB of the transfer function is,

$$20 \log |H(j\omega)| = 20 \log \left| \frac{A_o}{1 + j\alpha(\omega/\omega_h) + (j\omega/\omega_h)^2} \right|$$

$$= 20 \log \frac{A_o}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\alpha \frac{\omega}{\omega_h}\right)^2}} \tag{7.24}$$

The frequency response for different values of α is shown in Fig. 7.5. It may be seen that for a heavily damped filter ($\alpha > 1.7$), the response is stable. However, the roll-off begins very early to the pass band. As α is reduced, the response exhibits overshoot and ripple begins to appear at the early stage of pass band. If α is reduced too much, the filter may become oscillatory. The flattest pass band occurs for damping coefficient of 1.414. This is called a Butterworth filter. Audio filters are usually Butterworth. The Chebyshev filters are more lightly damped, that is, the damping coefficient α is 1.06. However, this increases overshoot and ringing occurs deteriorating the pulse response. The advantage, however, is a faster initial roll-off compared to Butterworth. A Bessel filter is heavily damped and has a damping

coefficient of 1.73. This gives better pulse response, however, causes attenuation in the upper end of the pass band.

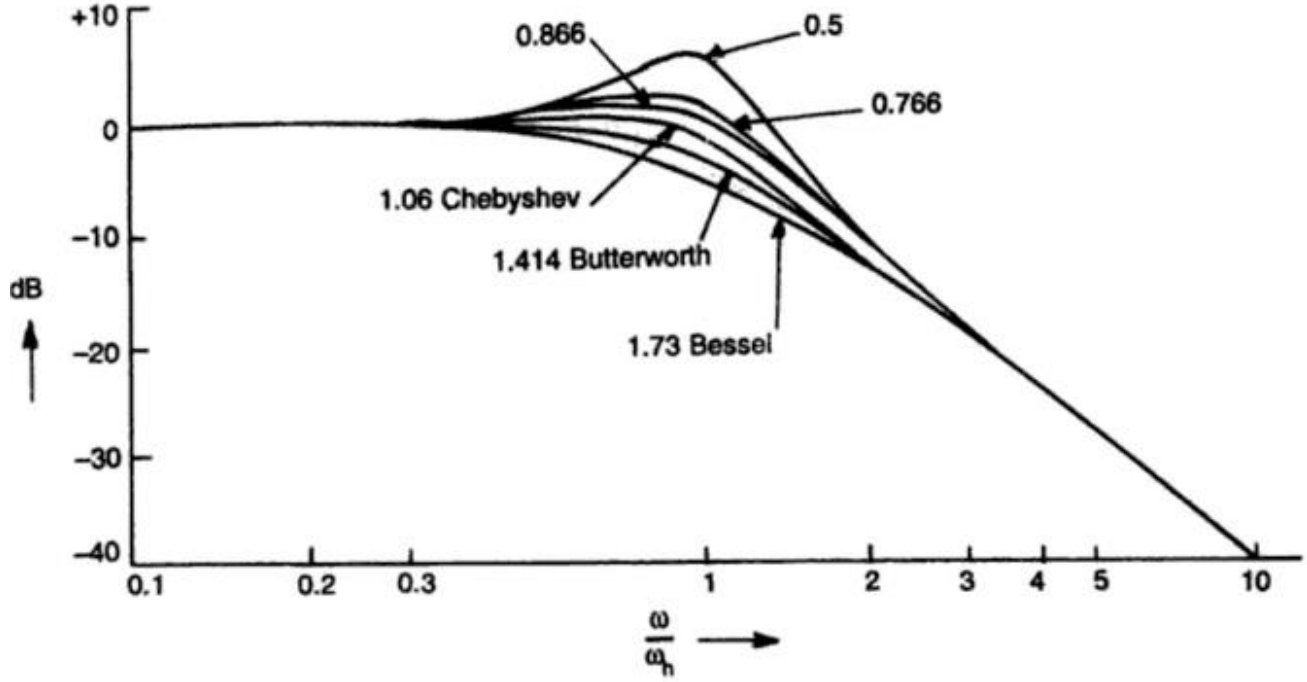


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_0 = 1$)

We shall discuss only Butterworth filter in this text as it has maximally flat response with damping coefficient $\alpha = 1.414$. From Eq. (7.24), with $\alpha = 1.414$, we get

$$20 \log \left| H(j\omega) \right| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^4}} \qquad (7.25)$$

Hence for n-th order generalized low-pass Butterworth filter, the normalized transfer function for maximally flat filter can be written as

$$\left| \frac{H(j\omega)}{A_o} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^{2n}}} \qquad (7.26)$$

UNIT –V PHASE LOCKED LOOP AND TIMER

PLL – principle – block diagram – phase comparator – VCO - lock – in range and capture range – PLL applications. IC 555 timer – functional diagram – Astable and Monostable Multivibrators – Schmitt trigger - Missing pulse detector- dual timer -Applications.

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2 Marks

1. **Define the term capture range in PLL. (Nov-15), (Dec-14)**

   The range of frequencies over which the PLL can acquire lock with the input signal is called as capture range. It is expressed as a percentage of the VCO free running frequency.

2. **Define lock in range of a PLL. (Nov-13)**

   when PLL is in lock, it can trap frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called as lock range. It is expressed as a percentage of the VCO free running frequency.

3. **What is a Schmitt trigger? (Nov-15)**

   A bistable circuit in which the output increases to a steady maximum when the input rises above a certain threshold, and decreases almost to zero when the input voltage falls below another threshold.

4. **List the application of PLL (April-14), (Nov-15A)**

   - Radar synchronisation
   - satellite communication systems
   - air borne navigational systems
   - FM communication systems
   - Computers.

5. **List the basic building block of a PLL. (April-15)**

   - Phase detector/comparator
   - Low pass filter
   - Error amplifier
   - Voltage controlled oscillator

6. **Define sample period and hold period. (Nov-13)**

   In analog device, samples (captures, grabs) the voltage of a continuously varying analog signal and holds (locks, freezes) its value at a constant level for a specified minimum period of time.

7. **What are the basic elements of IC 555 timer? (Nov-15A)**

- A relaxation oscillator
- RS flip flop
- Two comparator
- Discharge transistor.

8. **In a monostable multivibrator using 555 timer R=100K? and time delay is 100ms find the value of C? (Dec-14)**

9. **What is the frequency synthesizer? (April-14), (April-15)**

A frequency synthesizer is an electronic system for generating any of a range of frequencies from a single fixed timebase or oscillator. They are found in many modern devices, including radio receivers, mobile telephones, radiotelephones, walkie-talkies, CB radios, satellite receivers, GPS systems, etc.

10. **List out the types of digital voltmeter. (April-14)**

- Ramp type
- Integrating type
- Potentiometer type

11. **List the importance characteristics of PLL.**

- Acquisition and Tracking
- Pull-in Range
- Lock-in Range
- Hold-in Range

12. **What are the three stages through which PLL operates?**

- Free running
- Capture
- Locked/ tracking

13. **Define duty cycle?**

The ratio of high output and low output period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON Time to total time.

14. **What is mean by PLL?**

A PLL is a basically a closed loop system designed to lock output frequency and phase to the frequency and phase of an input signal

15. **Define VCO.**

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage.

16. Define pull-in time.

The total time taken by the PLL to establish lock is called pull-in time. It depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

17. For perfect lock, what should be the phase relation between the incoming signal and VCO output signal?

The VCO output should be 90 degrees out of phase with respect to the input signal.

18. On what parameters does the free running frequency of VCO depend on?

- External timing resistor,RT
- External timing capacitor,CT
- The dc control voltage Vc.

19. List the features of VCO.

- Wide supply voltage range from 10V to 24V.
- Very linear modulation characteristics.
- High temperature stability.
- Excellent power supply rejection.
- 10 to 1 frequency range with fixed C.
- The frequency can be controlled by means of a control voltage resistor or capacitor.

20. Give the applications of VCO.

- FM modulation.
- Signal generation (triangular or square wave)
- Function generation.
- In frequency multipliers.
- Converting low frequency signals such as EEG and ECG into audio frequency range signals.

21. What is the purpose of having a low pass filter in PLL?

*It removes the high frequency components and noise.

*Controls the dynamic characteristics of the PLL such as capture range, lock-in range, band width and transient response.

*The charge on the filter capacitor gives a short- time memory to the PLL.

22. Write the application of missing pulse detector.

A missing pulse detector does exactly what it says, it signals if a pulse is missing. Suppose you have a system which is going to give you a pulse to do something every once in a while. If the pulse is not there, then something is wrong. The missing pulse detector would raise a signal that there was a missing pulse and then some other action could occur.

23. What is the function of reset in IC 555 timer?

If reset is not used, connect it to Vcc. If reset falls, a high output will be forced low.

24. Define 555 IC?

The 555 timer is an integrated circuit specifically designed to perform signal generation and timing functions.

25. What are the applications of 555 Timer?

- astable multivibrator
- monostable multivibrator
- Missing pulse detector
- Linear ramp generator
- Frequency divider
- Pulse width modulation
- FSK generator
- Pulse position modulator
- Schmitt trigger

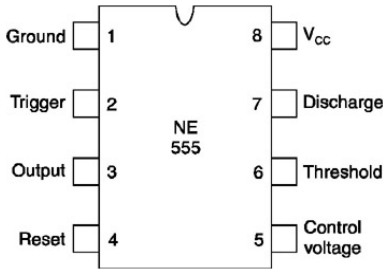
26. List the applications of 555 timer in Astable mode of operation:

- FSK generator
- Pulse-position modulator

27. List the applications of 555 timer in monostable mode of operation:(April-14)

- Missing pulse detector
- Linear ramp generator
- Frequency divider
- Pulse width modulation.

28.Give the pin diagram of IC 555 timer.



29.What is the function of threshold in 555 timers?

Detects when the voltage on the timing capacitor rises above 0.66 Vcc and resets the output when this happens.

30.Explain the pin detail of 555 timer?

Pin	Name	Description
1	Ground	OV supply
2	Trigger	When the pin voltage falls below 0.33 V, the timer is triggered and the output goes high.
3	Output	output

4	Reset	If reset is not used, connect it to Vcc. If reset falls, a high output will be forced low.
5	Control voltage	Provides control voltage
6	Threshold	Detects when the voltage on the timing capacitor rises above 0.66 Vcc and resets the output when this happens.
7	Discharge	Provides a discharge path from the timing capacitor to ground when the output is low
8	VCC	Positive power supply voltage

****

1. Explain in detail about PLL with neat block diagram.

Definition:

The phase locked loop, commonly called PLL, is a closed loop feedback system, whose output frequency and phase are in lock with the frequency and phase of the input signal. The PLL is an important building block of a linear system, which can detect the phases of two signals and reduce the difference in the presence of a phase difference.

Basic PLL Operation

Fig. shows the block diagram of PLL. It consists of

- Phase detector
- Low pass filter
- Error amplifier
- Voltage Controlled Oscillator (VCO)

The phase detector compares the input frequency f_i with the feedback frequency f_o and generates an output signal which is a function of the difference between the phases of the two input signals. The output signal of the phase detector is a dc voltage. The output of phase detector is applied to low-pass filter to remove high frequency noise from the dc voltage. The output of low pass filter without high frequency noise is often referred to as error voltage or control voltage for VCO. When control voltage is zero, VCO is in free-running mode and its output frequency is called as center frequency f_o. The non-zero control voltage results in a shift in the VCO frequency from its free-running frequency, f_o to a frequency f, given by $f = f_o + K_v V_C$, where K_V is the voltage to frequency transfer coefficient of the VCO. The error or control voltage applied as an input to the VCO, forces the VCO to change its output frequency in the direction that reduces the difference between the input frequency and the output frequency of VCO.

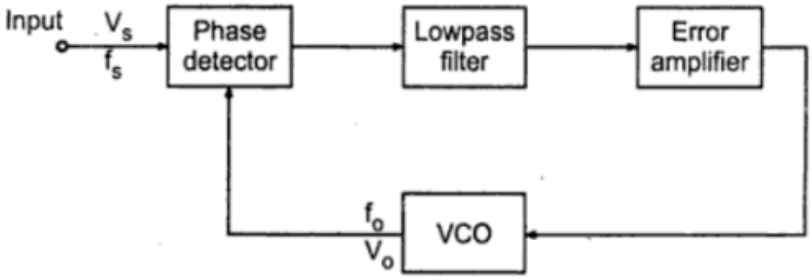


Fig. Block diagram of PLL

This action, commonly known as capturing, continues till the output frequency of VCO is same as the input signal frequency. Once the two frequencies are same, the circuit is said to be locked. In locked condition, phase detector generates a constant dc level which is required to shift the output frequency of VCO from centre frequency to the input frequency. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three states : free running, capture and phase lock.

Important Definitions Related to PLL

Lock range :

When PLL is in lock, it can track frequency changes in the incoming signal. The range of frequencies over which the PLL can maintain lock with the incoming signal is called the **Llock range** or **tracking range** of the PLL. It is usually expressed as a percentage of f_o, the VCO frequency.

Capture range :

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. It is also expressed as a percentage of f_o.

Pull-in time :

The capture of an input signal does not take place as soon as the signal is applied, but it takes finite time. The total time taken by the PLL to establish lock is called **pull-in time**. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and the bandwidth of the low pass filter.

Process of Capture It is an important aspect of PLL, by which the loop achieves the condition of being *in-lock* with a signal from a free-running and unlocked condition. In the unlocked condition of the PLL, the VCO operates at a frequency f_c, called *center frequency* or *free running frequency.* This corresponds to an applied voltage of 0V dc at its control input. The capture process is inherently non-linear and starts occurring as described below.

Let us assume that the feedback loop of the PLL is initially open between the loop-filter and VCO control input. An input signal of frequency f_i, which is assumed to be closer to the VCO center frequency, f_c is applied to the input of the phase detector. The phase detector is usually an analog multiplier that multiplies the two sinusoids together, and it produces the sum and difference of the two signals at its output. Since the high frequency sum component is filtered out by the low-pass filter, the output of the LPF is a sinusoid, whose frequency is equal to the difference between the VCO center frequency f_c and incoming signal frequency f_i.

Considering that the loop is suddenly closed, the difference frequency sinusoid is applied to the VCO input as the control voltage, v_c. Thus this will make the VCO frequency f_o, a sinusoidal function of time. Therefore, it alternately moves closer and farther away from f_i. The output frequency of the phase detector, being the difference between f_o and f_i, moves to a higher frequency when f_o moves away from f_i, and moves to a lower frequency when f_o moves closer to f_i. This fact is reflected in the phase detector output having an asymmetrical wave shape during the capture process as shown in Fig. 10.2. This asymmetry in the waveform produces a dc component in the phase detector output. This dc component shifts the VCO frequency f_o towards f_i

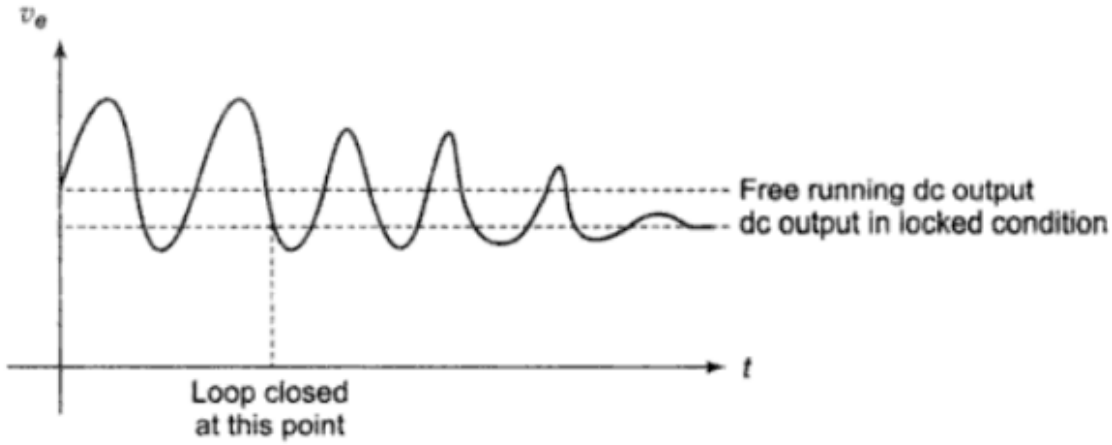


Fig. 10.2 *Output of phase detector during capture process*

and the frequency difference gradually diminishes. When the loop is locked, the frequency difference becomes zero, and a dc voltage remains at the loop-filter output.

The low-pass loop-filter filters out the difference frequency components resulting from interfering signals, which are far away from the center frequency. It also acts as a memory for the loop, when the lock is momentarily lost due to a large interfering transient signal. Therefore, the capture-range and pull-in time are dependent on the amount of gain in the loop and the bandwidth of the filter. The signal will be out of capture range when the beat frequency is too high due to the VCO frequency which is far away from the center frequency. Once lock is achieved, the VCO can track the signal well beyond the capture-range. Reducing the bandwidth of the filter thus improves the *rejectivity* of out-of-band signals, but it reduces the capture range; the pull-in time increases and loop phase margin become less.

2. Explain in detail about phase detector.

Phase Detector / Comparator Block of PLL

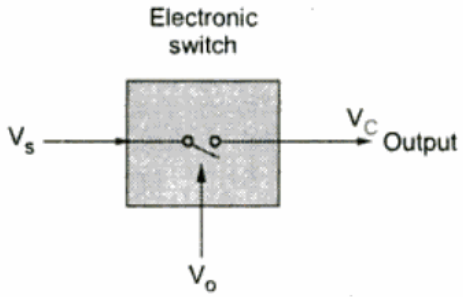
The phase detector is an initial and most important part of PLL. There are two types of phase detectors : Analog and Digital.

Analog Phase Detectors

1. Switch Type Phase Detector.
2. Balanced Modulator Type Phase Detector.

Switch Type Phase Detector

The Fig. 8.2 shows the basic circuit and waveforms of analog phase detector. It consists of electronic switch, S. The switch is opened and closed by signal coming from VCO as



From VCO (a) Basic circuit

shown in the Fig. 8.2 (b). The switch is closed when VCO output is positive; otherwise it is open. Let us see the output of phase detector at different phase angles of input signals.

When $\phi = 0$, i.e. when the input signal V_s is in phase with VCO output V_o, the output waveform V_e will be positive half sinusoids (shaded portion) shown in the Fig. 8.2 (c).

When $\phi = 90°$, the output waveform V_e contains half portion of negative cycle and half portion of positive cycle shown in the Fig. 8.2 (d).

When $\phi = 180°$, the output waveform V_e contains negative half sinusoids shown in Fig. 8.2 (e). The average output voltages (error voltage) at different phase angles of input signals are shown in respective figures by dotted line. It may be seen that the error voltage is zero when the phase shift between the two inputs (V_s and V_o) is 90°. This is a perfect lock condition. For phase shifts 0° and 180° the error voltage is positive and negative, respectively.

The detector studied above is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged.

A phase detector actually multiplies the input signal ($V_s = V_s \sin(2\pi f_s t)$) by the VCO signal ($V_o = V_o \sin(2\pi f_o t + \phi)$). The output of multiplication is an error signal and it is given as

$$V_e = KV_sV_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi) \quad \ldots (1)$$

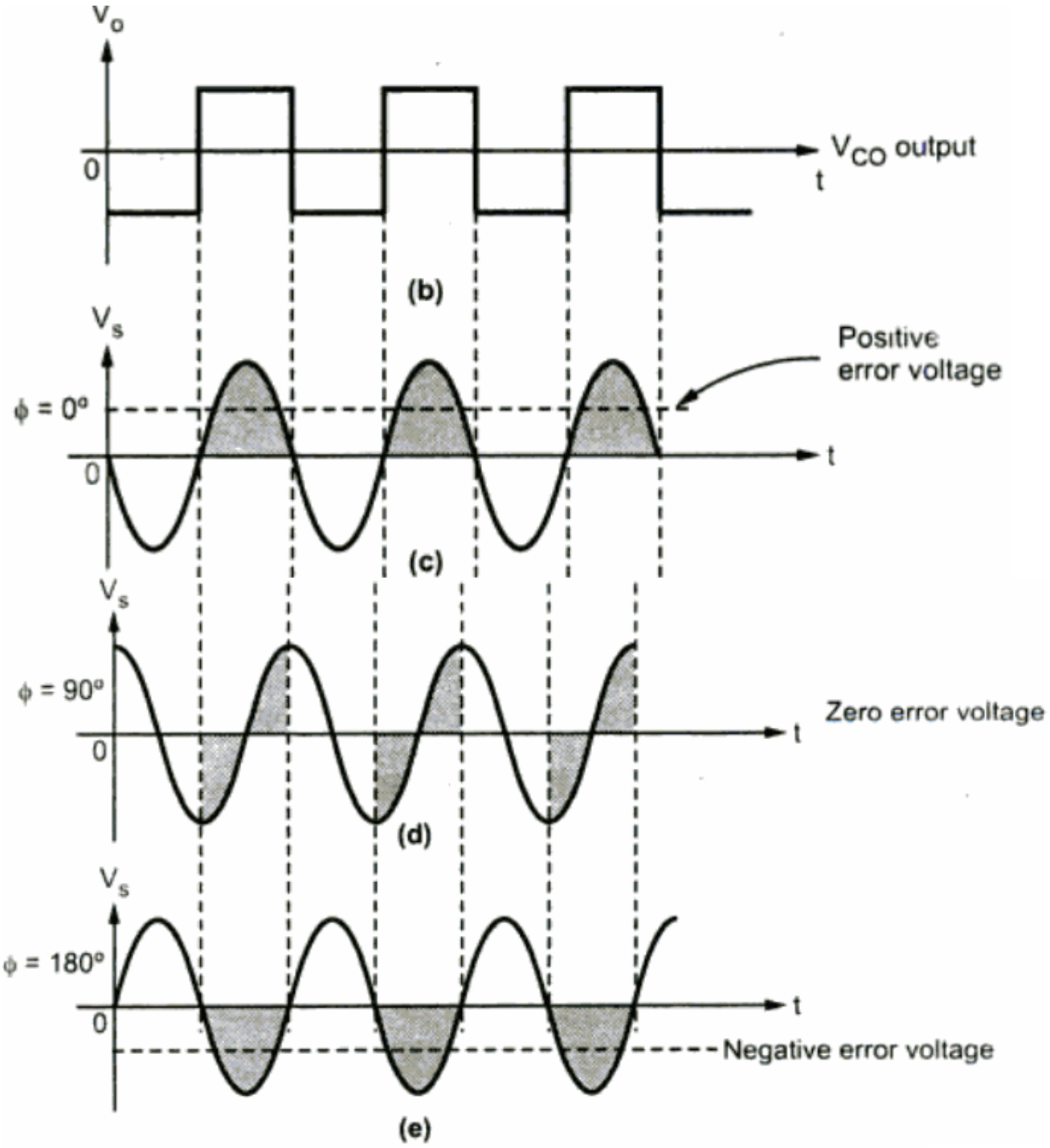


Fig. 8.2 Phase detector basic circuit and waveforms

Where K : Phase detector gain or attenuation constant, the equation (1) can be simplified as

$$V_e = \frac{KV_sV_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \quad \ldots (2)$$

At lock condition $f_s = f_o$,

$$\therefore \quad \boxed{V_e = \frac{KV_sV_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)\right]} \quad \ldots (3)$$

The equation (3) shows that the phase detector output contains double frequency term and a dc term. The dc term $(KV_sV_o/2) \cos \phi$ varies as a function of phase ϕ, i.e. $\cos \phi$ between the two signals. The double frequency term is filtered by the low pass filter and dc term is applied to the modulating input terminal of a VCO. The dc term i.e., the dc error voltage is zero at $\phi = 90$. Therefore, for perfect lock condition $f_s = f_o$ and $\phi = 90°$.

Problems Associated with Switch Type Phase Detector

- The error voltage V_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude..
- The output is proportional to $\cos \phi$ instead of only ϕ. This makes it non-linear.

Digital Phase Detector

Phase Detector Using XOR Gate

The XOR gate can be used as a digital phase detector when both signal f_s and f_o are square waves. This is illustrated in the Fig. 7.15. We know that the output of XOR gate is high when only one of the input signals is high. The Fig. 7.15 shows the input and output waveforms for digital phase detector. Here, f_s is leading f_o by ϕ degrees.

Fig. 7.15 (a) XOR as a digital phase detector

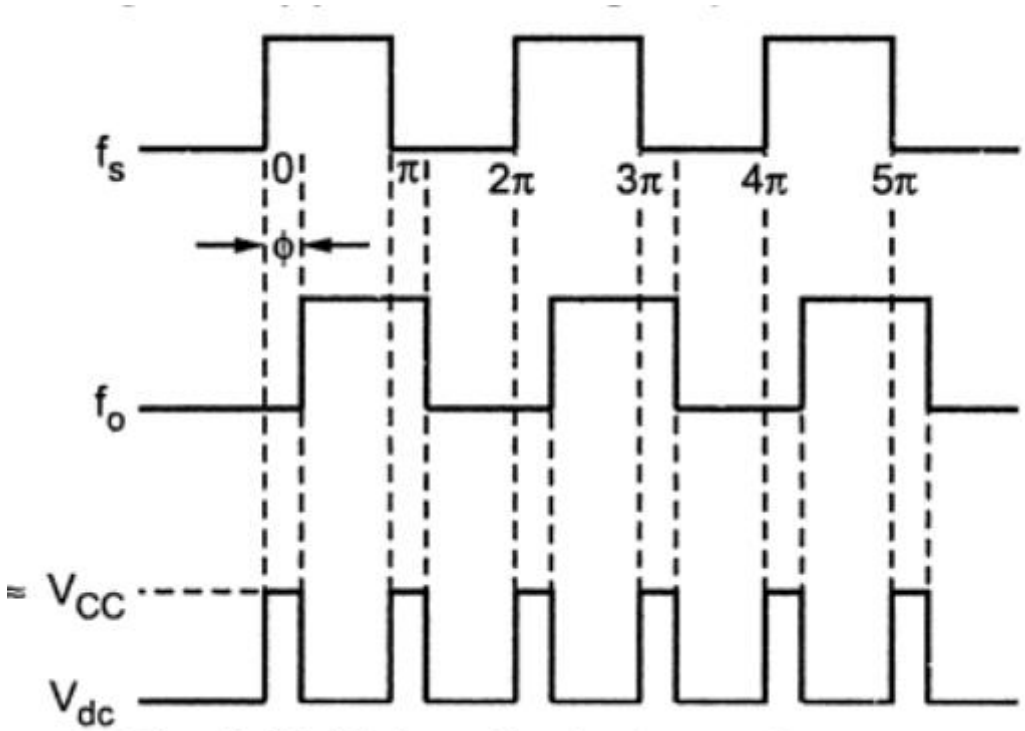


Fig. 7.15 (b) Input/output waveforms

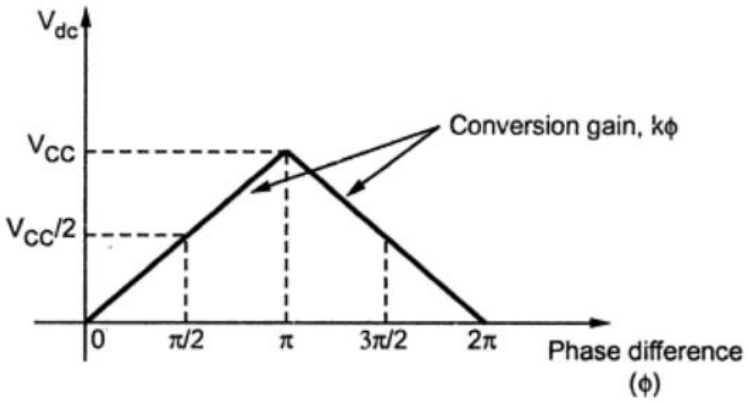


Fig. 7.15 (c) Relationship between V_{dc} and ϕ

Looking at Fig. 7.15 (b) it can realized that when $\phi = 0$, $V_{dc} = 0$ and when $\phi = \pi$, $V_{dc} = V_{CC}$. The relationship between V_{dc} and phase difference ϕ is plotted in the Fig. 7.15 (c). The slope of the curve shown in the Fig. 7.15 (c) gives the conversion ratio K_ϕ of the phase detector. It is given by

$$k_\phi = \frac{V_{cc}}{\pi} \quad \text{V/rad}$$

3. Explain in detail about VCO with neat block diagram.

Voltage Controlled Oscillator (VCO)

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controlled by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillation frequency. Applied voltage is called **control voltage.** The control of frequency with the help of control voltage is also called voltage to frequency conversion. Hence VCO is also called **voltage to frequency converter.** Practically VCO is used to produce square and triangular waveforms whose frequency is controlled by control voltage.

Voltage Controlled Oscillator (VCO) IC 566

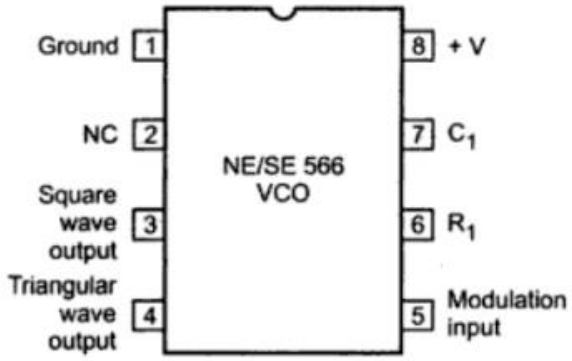


Fig. 4.31 Pin diagram of IC 566 VCO

A voltage controlled oscillator is an oscillator circuit in which the frequency of oscillations can be controller by an externally applied voltage. The VCO provides the linear relationship between the applied voltage and the oscillation frequency. Applied voltage is called **control voltage.** The control of frequency with the help of control voltage is also called voltage to frequency conversion. Hence VCO is also called **voltage to frequency converter.** Practically VCO is used to produce square and triangular waveforms whose frequency is controlled by control voltage.

Practically VCO is available in IC form. The commonly used VCO ICs are NE/SE 566, LM 566 etc. The Fig. 4.31 shows the pin diagram of NE/SE 566 VCO manufactured by Signetics. It is 8 pin IC, which provides two output pins. Its feature is that simultaneously IC provides square and triangular wave outputs which are the functions of input voltage. The input voltage is also called **modulating input voltage.**

Operation : The op-amp A_1 is used as a buffer. The op-amp A_2 is used as a Schmitt trigger and the op-amp A_3 is used as an inverter. The voltage V_C is applied to the modulation input pin, which is a control voltage.

The capacitor C_1 is linearly charged or discharged by a constant current source. The charging current can be controlled by controlling the voltage V_C at pin 5 or by varying the resistance R_1 which is external to the IC. The charging and discharging levels are determined by the Schmitt trigger.

The output voltage of Schmitt trigger is designed to swing between +V and 0.5 V. For $R_a = R_b$, the voltage at non-inverting terminal swings between 0.5(+V) to 0.25(+V). Thus the triangular wave is generated due to alternate charging and discharging of the capacitor C_1, in linear manner. When C_1 voltage increases beyond 0.5(+V), the Schmitt trigger output goes low, and the capacitor starts discharging. When the voltage becomes less than 0.25 (+V), the output of the Schmitt trigger goes high. Due to similar current sources used

The Fig. 4.32 shows the block diagram of NE/SE 566 VCO.

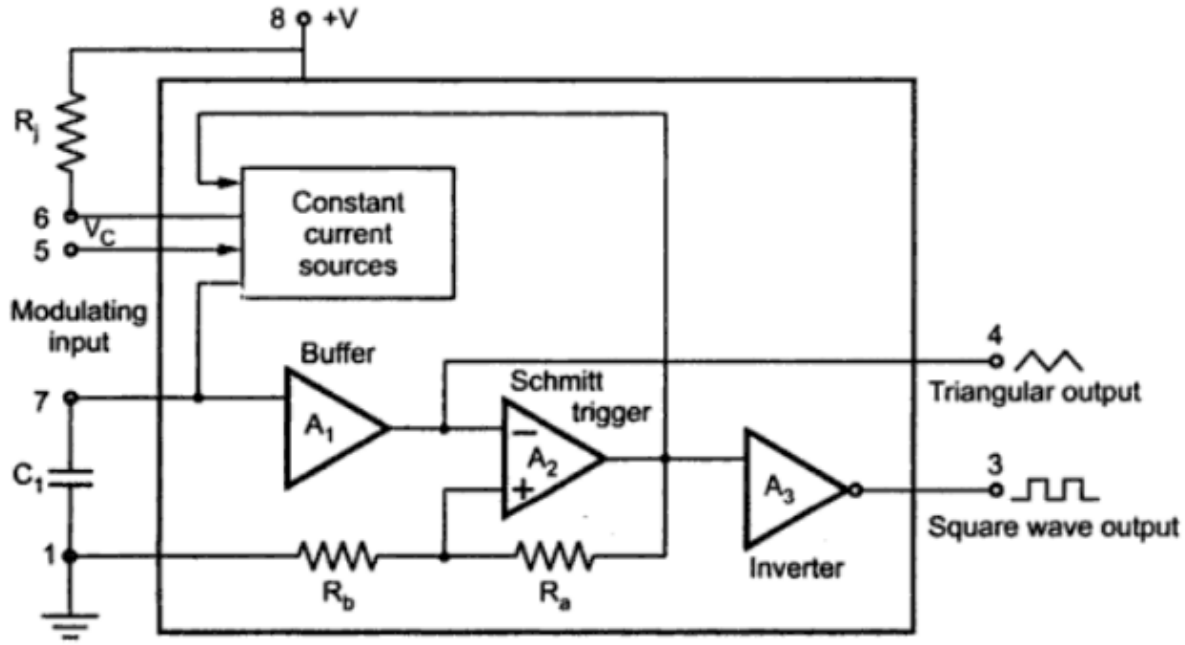


Fig. 4.32 Block diagram of NE/SE 566 VCO

for charging and discharging, the time taken by C_1 to charge and discharge is same. This produces exact triangular wave. The output of the Schmitt trigger output is step response which is available at the pin 3 as a square wave output. The various waveforms are shown in the Fig. 4.33.

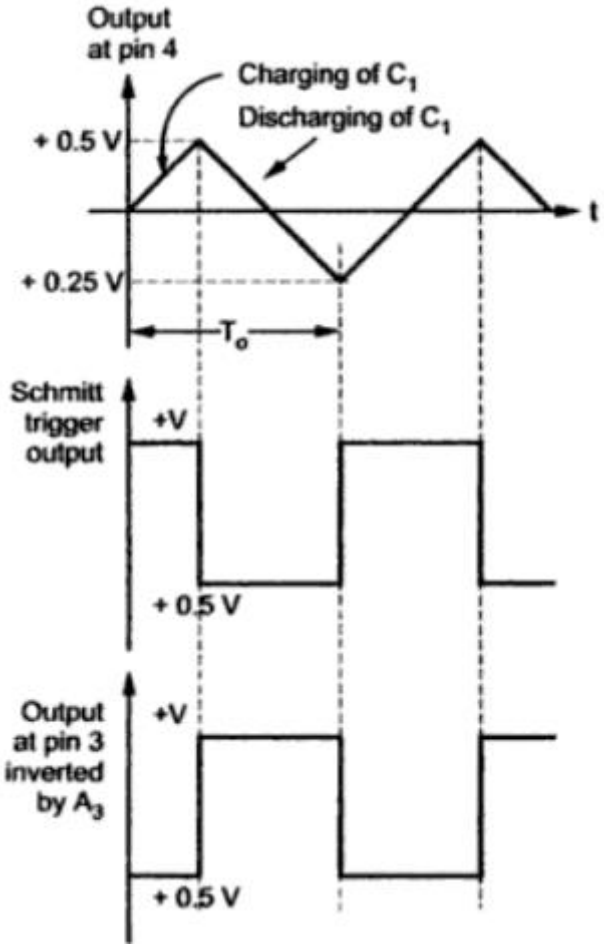


Fig. 4.33 Waveforms for VCO

The frequency of the output waveform is,

$$f_o = \frac{2(+V - V_C)}{C_1 R_1 (+V)} \quad \text{... (1)}$$

R_1 should be in the range of 2 kΩ to 20 kΩ. The equation shows that the frequency of the output oscillations is a frequency of the control voltage V_C. The frequency is also a function of the external resistance R_1 and capacitor C_1.

Typical Connection Diagram of 566 VCO

Practically the modulating input voltage at the pin 5 is controlled using a potential divider formed by the resistances R_2 and R_3. Such a circuit is shown in the Fig. 4.34.

The $R_2 - R_3$ potential divider is used to set the control voltage V_C. The initial voltage V_C at the pins must be such that,

$$0.75(+V) \leq V_C \leq +V$$

where +V is the supply voltage.

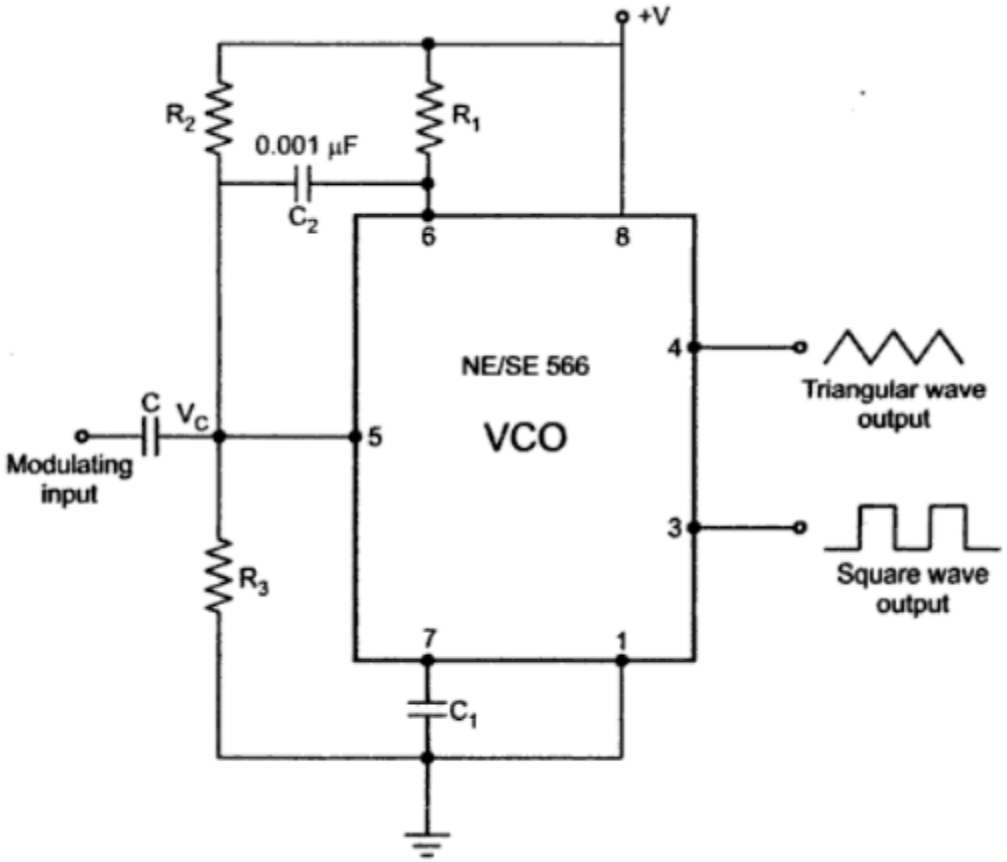


Fig. 4.34 Typical connection diagram of 566 VCO

The modulating input is connected through capacitor coupling to the pin 5 and it must be less than 3 V(p-p). For a fixed V_C and C_1 the frequency can be varied in the range 10 : 1 by varying R_1 between 2 kΩ to 20 kΩ. For fixed R_1 and C_1 the frequency can be varied in the range 10 : 1 by varying control voltage V_C. In both the cases maximum possible output frequency is 1 MHz. The capacitor C_2 connected between pins 5 and 6 is used to elliminate any oscillations present in constant current source.

Features of 566 VCO

1. **Wide supply voltage range 10 V to 24 V.**
2. **Very linear modulation characteristics.**
3. High temperature stability.
4. Excellent power supply rejection.
5. 10 to 1 frequency range with fixed C_1.
6. The frequency can be controlled by means of current, voltage, resistor, or capacitor.

Applications of VCO

The various applications of VCO are

1. FM modulation.
2. Signal generation (Triangular or square wave)
3. Function generation.
4. Frequency shift keying i.e. FSK demodulator.
5. In frequency multipliers.
6. Converting low frequency signals such as EEG and EKG into audio frequency range signals.
7. Tone generation.

4. Explain in detail about various applications of PLL.

Some of the typical applications of PLL are:

- Frequency Multiplication
- Frequency Translation
- AM detection
- FM detection
- Frequency shift keying demodulation
- Frequency synthesizer

Frequency Multiplier

Fig. 8.15 shows the block diagram for a frequency multiplier using PLL 565. Here, a divide by N network is inserted between the VCO output (pin 4) and the phase comparator input (pin 5). Since the output of the divider is locked to the input frequency f_i, the VCO is actually running at a multiple of the input frequency. Therefore, in the locked state, the VCO output frequency f_o is given by,

$$f_o = Nf_i \quad \ldots (1)$$

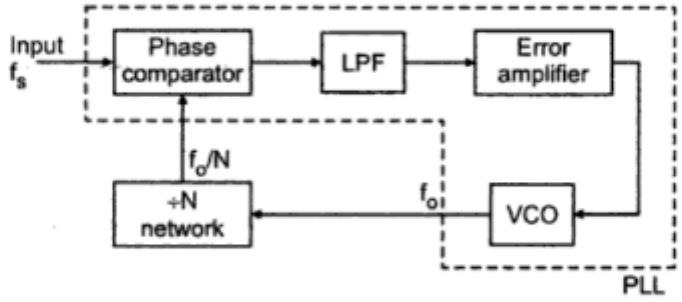


Fig. 8.15 Block diagram of frequency multiplier

By selecting proper divider by N network, we can obtain desired multiplication. For example, to obtain output frequency $f_o = 6\ f_i$, a divide by N should be equal to 6.

Fig. 8.16 shows LM 565 IC used as a frequency multiplier circuit. The IC 7490 is a 4 bit binary counter. It is configured as a divide by 10 circuit.

Frequency Synthesizer

The PLL can be used as the basis for frequency synthesizer that can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator. Fig. 8.17 shows the block diagram of frequency synthesizer. It is similar to frequency multiplier circuit except that divided by M network is added at the input of phase lock loop. The frequency of the crystal-controlled oscillator is divided by an integer factor M by divider network to produce a frequency f_{osc}/M, where f_{osc} is the frequency of the crystal controlled oscillator. The VCO frequency f_{VCO} is similarly divided by factor N by divider network to give frequency equal to f_{vco}/N. When the PLL is locked in on the divided-down oscillator frequency, we will have $f_{osc}/M = f_{vco}/N$, so that $f_{vco} = (N/M)\ f_{osc}$.

By adjusting divider counts to desired values large number of frequencies can be produced, all derived from the crystal controlled oscillator.

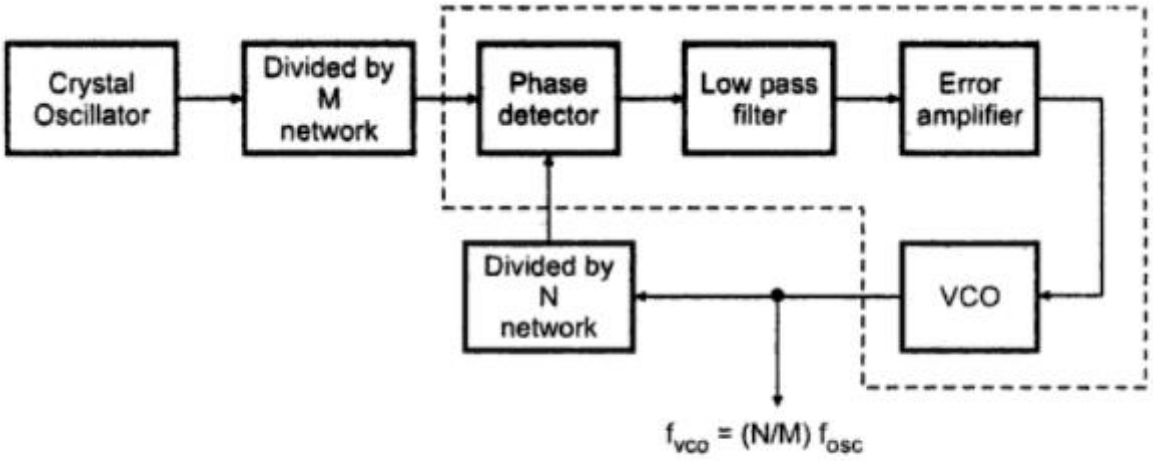


Fig. 8.17 Block diagram of frequency synthesizer

FM Demodulator

The PLL can be very easily used as an FM detector or demodulator. Fig. 8.18 shows the block diagram of FM detector.

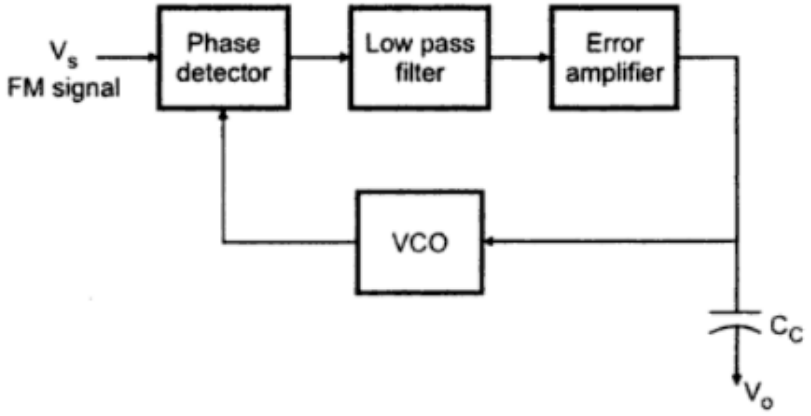


Fig. 8.18 PLL as a FM detector

When the PLL is locked in on the FM signal, the VCO frequency follows the instantaneous frequency of the FM signal, and the error voltage or VCO control voltage is proportional to the deviation of the input frequency from the centre frequency. Therefore, the a-c component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage that is applied to the FM carrier at the transmitter. The faithful reproduction of modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage of VCO. It is also important to note that the FM frequency deviation and the modulating frequency should remain in the locking range of PLL to get the faithful replica of the modulating signal. If the product of the modulation frequency f_m and the frequency deviation exceeds the $(\Delta f_C)^2$, the VCO will not be able to follow the instantaneous frequency variations of the FM signal.

AM Detection

A PLL can be used to demodulate AM signals as shown in Fig. 7.12.

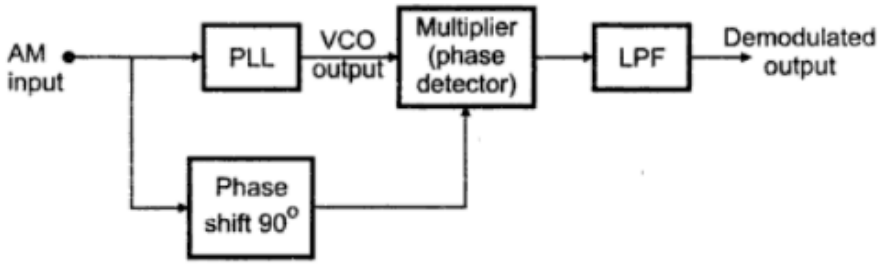


Fig. 7.12 PLL used as AM demodulator

The PLL is locked to the carrier frequency of the incoming AM signal. Once locked the output frequency of VCO is same as the carrier frequency, but it is in unmodulated form. The modulated signal with 90° phase shift and the unmodulated carrier from output of PLL are fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, both the signals applied to the multiplier are in same phase. Therefore, the output of the multiplier contains both the sum and the difference signals. The low pass filter connected at the output of the multiplier rejects high frequency components giving demodulated output. As PLL follows the input frequencies with high accuracy, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

Frequency Translation

The frequency translation means shifting the frequency of an oscillator by a small factor. Fig. 7.13 shows the block schematic for frequency translator using PLL..

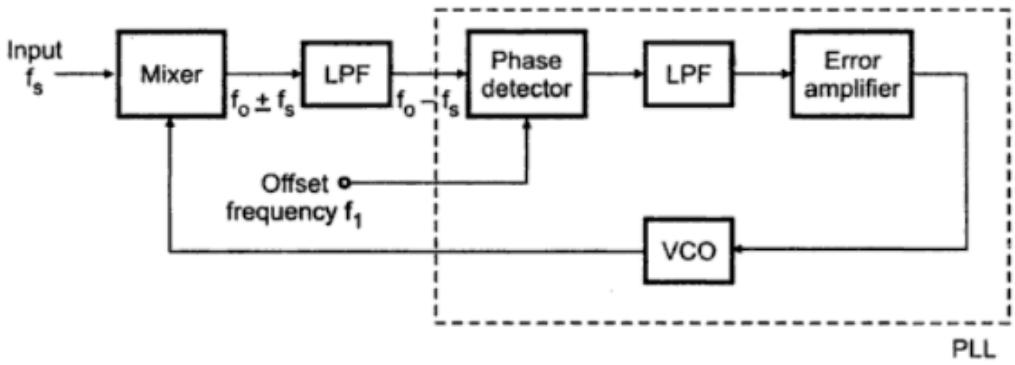


Fig. 7.13 Block schematic for frequency translator using PLL

It consists of mixer, low pass filter and the PLL. The input frequency f_s which has to be shifted is applied to the mixer. Another input to the mixer is the output voltage of VCO, f_o. Therefore, the output of mixer contains the sum and difference signal ($f_o \pm f_s$). The low pass filter connected at the output of mixer rejects the ($f_o + f_s$) signal and gives only ($f_o - f_s$) signal at the output. The ($f_o - f_s$) signal is applied to the phase detector. Another input for phase detector is the offset frequency f_1. In the locked mode, the VCO output frequency is adjusted to make two input frequencies of phase detector equal. This gives

$f_o - f_s = f_1$ and $f_o = f_s + f_1$

By adjusting offset frequency f_1 we can shift the frequency of the oscillator to the desired value.

Frequency Shift Keying (FSK) Demodulator

In digital data communication, binary data is transmitted by means of a carrier frequency. It uses two different carrier frequencies for logic 1 and logic 0 states of binary data signal. This type of data transmission is called frequency shift keying (FSK). In this data transmission, on the receiving end, two carrier frequencies are converted into 1 and 0 to get the original binary data. This process is called as FSK demodulation.

A PLL can be used as a FSK demodulator, as shown in the Fig. 7.11. It is similar to the PLL demodulator for analog FM signals except for the addition of a comparator to produce a reconstructed digital output signal.

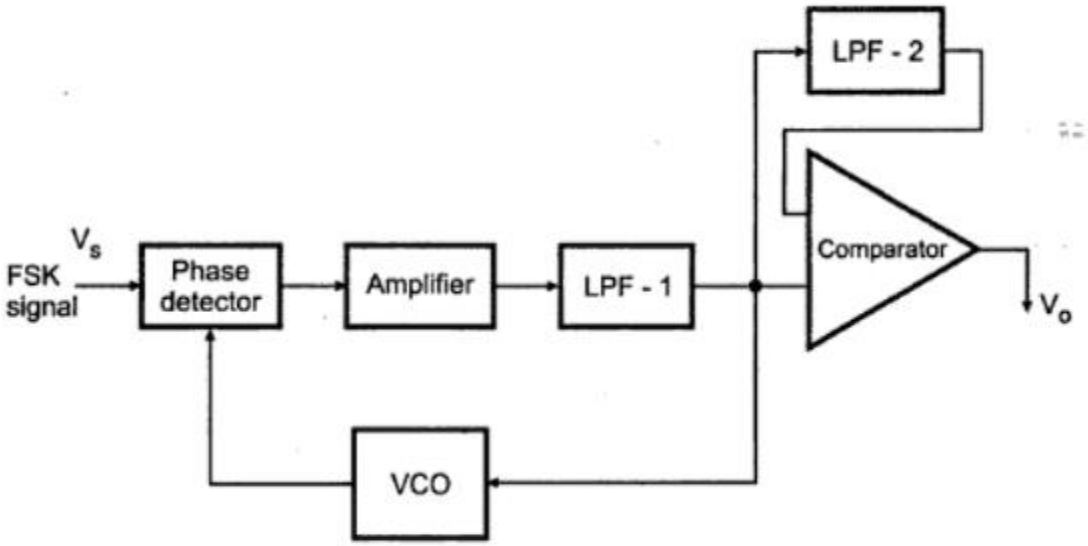


Fig. 7.11 Frequency shift keying demodulator

Let us consider that there are two frequencies, one frequency (f_1) is represented as "0" and other frequency (f_2) is represented as "1". If the PLL is locked into the FSK signal at both f_1 and f_2, the VCO control voltage which is also supplied to the comparator will be given as

$$V_{C1} = (f_1 - f_0) / K_v \text{ and}$$

$$V_{C2} = (f_2 - f_0) / K_v \text{ , respectively.}$$

where K_v is the voltage to frequency transfer coefficient of the VCO.

The difference between the two control voltage levels will be $\Delta V_C = (f_2 - f_1) / K_v$.

The reference voltage for the comparator is derived from the additional low pass filter and it is adjusted midway between V_{C1} and V_{C2}. Therefore, for V_{C1} and V_{C2}, comparator gives output '0' and '1', respectively.

5. Explain the IC 555 Timer with necessary functional block diagram.

- The 555 timer is a highly stable device for generating accurate time delay or oscillation. It was first introduced by Signetics Corporation .

Functional Block Diagram of IC 555

The IC 555 timer combines the following elements :

1) A relaxation oscillator
2) R-S flip-flop
3) Two comparators
4) Discharge transistor

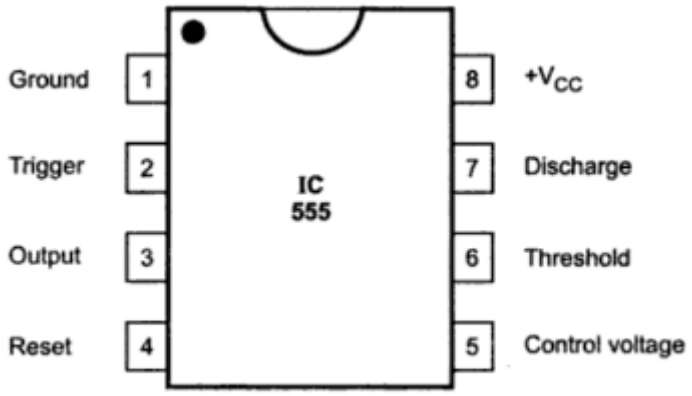


Fig. 6.9 (a) Pin diagram

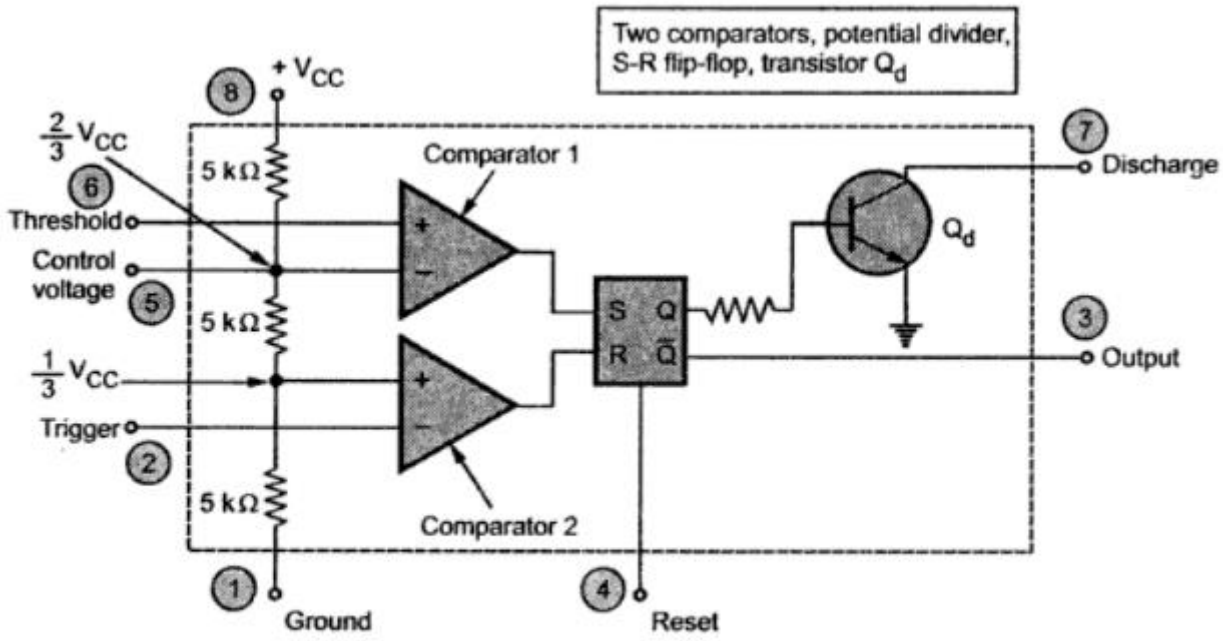


Fig. 5.9 (b) Block diagram of IC 555 timer

Functions of Pins

The pin numbers of IC 555 and their functions are discussed below :

Pin 1 : Ground

All the voltages are measured with respect to this terminal.

Pin 2 : Trigger

The IC 555 uses two comparators. The voltage divider consists of three equal resistances. Due to voltage divider, the voltage of noninverting terminal of comparator 2 is fixed at V_{CC} / 3. The inverting input of comparator 2 which is compared with $V_{CC}/3$, is nothing but trigger input brought out as pin number 2. When the trigger input is slightly less than V_{CC} /3 the comparator 2 output goes high. This output is given to reset input of R-S flip-flop. So high output of comparator 2 resets the flip-flop.

Pin 3 : Output

The complementary signal output ($\overline{Q}$) of the flip-flop goes to pin 3 which is the output. The load can be connected in two ways. One between pin 3 and ground while other between pin 3 and pin 8.

Pin 4 : Reset

This is an interrupt to the timing device. When pin 4 is grounded, it stops the working of device and makes it off. Thus, pin 4 provides on/off feature to the IC 555. This reset input overrides all other functions within the timer when it is momentarily grounded.

Pin 5 : Control Voltage Input

In most of the applications, external control voltage input is not used. This pin is nothing but the inverting input terminal of comparator 1. The voltage divider holds the voltage of this input at 2/3 V_{CC}. This is reference level for comparator 1 with which threshold is compared. If reference level required is other than 2/3 V_{CC} for comparator 1 then external input is to be given to pin 5.

If external input applied to pin 5 is alternating then the reference level for comparator 1 keeps on changing above and below 2/3 V_{CC}. Due to this, the variable pulse width output is possible. This is called **pulse width modulation**, which is possible due to pin 5.

Pin 6 : Threshold

This is the noninverting input terminal of comparator 1. The external voltage is applied to this pin 6. When this voltage is more than 2/3 V_{CC}, the comparator 1 output goes high. This is given to the set input of R-S flip-flop. Thus high output of comparator 1 sets the flip-flop. This makes Q of flip-flop high and $\overline{Q}$ low. Thus the output of IC 555 at pin 3 goes low.

For threshold $> \frac{2}{3} V_{CC}$, flip-flop $\rightarrow$ set, Q $\rightarrow$ high, output at pin 3 $\rightarrow$ low

For trigger $< \frac{1}{3} V_{CC}$, flip-flop $\rightarrow$ reset, Q $\rightarrow$ low, output at pin 3 $\rightarrow$ high

Pin 7 : Discharge

This pin is connected to the collector of the discharge transistor Q_d. When the output is high then Q is low and transistor Q_d is off. It acts as an open circuit to the external capacitor C to be connected across it, so capacitor C can charge as described earlier. When output is low, Q is high which drives the base of Q_d high, driving transistor Q_d in saturation. It acts as short circuit, shorting the external capacitor C to be connected across it.

Pin 8 : Supply $+V_{cc}$

The IC 555 timer can work with any supply voltage between 4.5 V and 16 V.

Applications:

1. Oscillators
2. Pulse generator
3. Mono shot multivibrators
4. Traffic light control
5. Burglar alarm

6. Explain the IC 555 Timer with necessary functional block diagram.

7. Describe the functional block diagram of monostable mode of operation of IC 555 timer. Draw necessary waveform and expression. (Nov-15)

Monostable Multivibrator using IC 555

The IC 555 timer can be operated as a monostable multivibrator by connecting an external resistor and a capacitor as shown in the Fig. 5.10.

The circuit has **only one stable state**. When trigger is applied, it produces a pulse at the output and returns back to its stable state. The duration of the pulse depends on the values of R and C. As it has only one stable state, it is called one shot multivibrator.

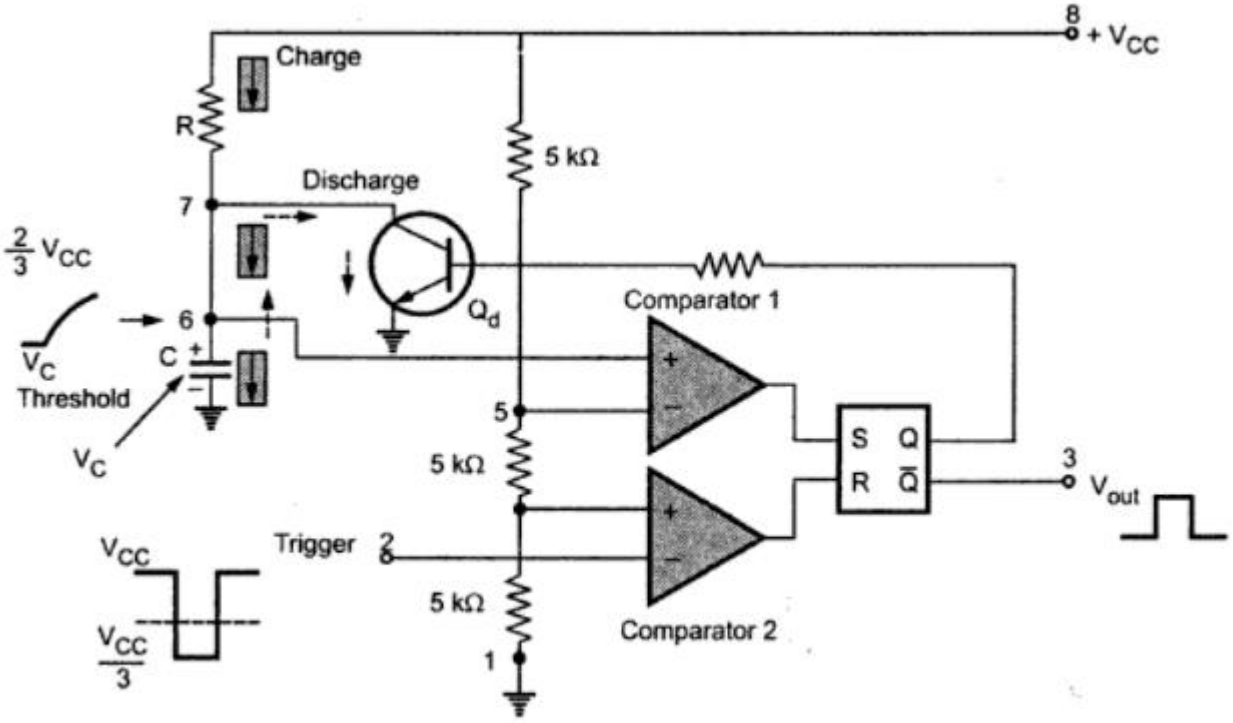


Fig. 5.10 Monostable operation of 555

Operation

The flip-flop is initially set i.e. Q is high. This drives the transistor Q_d in saturation. The capacitor discharges completely and voltage across it is nearly zero. The output at pin 3 is low.

When a trigger input, a low going pulse is applied, then circuit state remains unchanged till trigger voltage is greater than 1/3 V_{CC}. When it becomes less than 1/3 V_{CC}, then comparator 2 output goes high. This resets the flip-flop so Q goes low and $\bar{Q}$ goes high. Low Q makes the transistor Q_d off. Hence capacitor starts charging through resistance R, as shown by dark arrows in the Fig. 5.10.

The voltage across capacitor increases exponentially. This voltage is nothing but the threshold voltage at pin 6. When this voltage becomes more than 2/3 V_{CC} , then comparator 1 output goes high. This sets the flip-flop i.e. Q becomes high and $\bar{Q}$ low. This high Q drives the transistor Q_d in saturation. Thus capacitor C quickly discharges through Q_d as shown by dotted arrows in the Fig. 5.11.

So it can be noted that V_{out} at pin 3 is low at start, when trigger is less than 1/3 V_{CC} it becomes high and when threshold is greater than 2/3 V_{CC} again becomes low, till next trigger pulse occurs. So a rectangular wave is produced at the output. The pulse width of this rectangular pulse is controlled by the charging time of capacitor. This depends on the time constant RC. **Thus RC controls the pulse width.** The waveforms are shown in the Fig. 5.11.

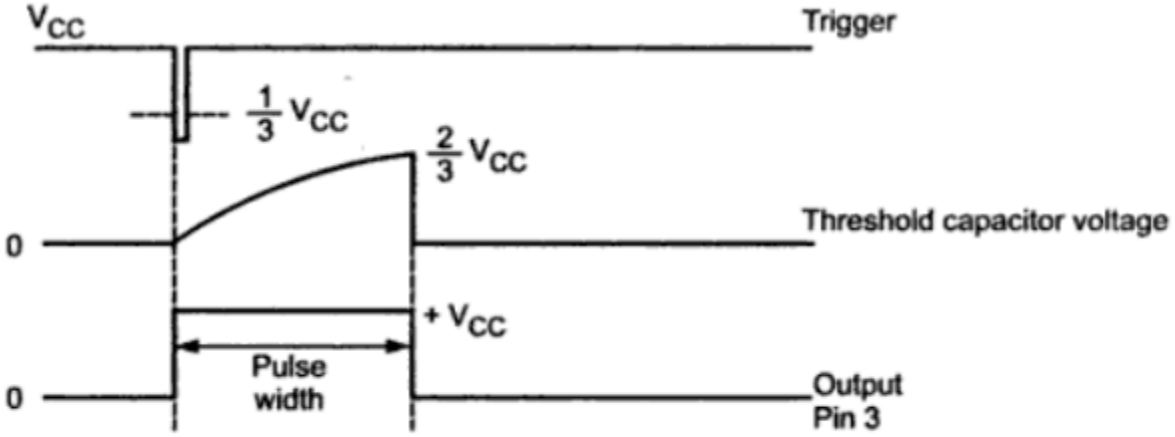
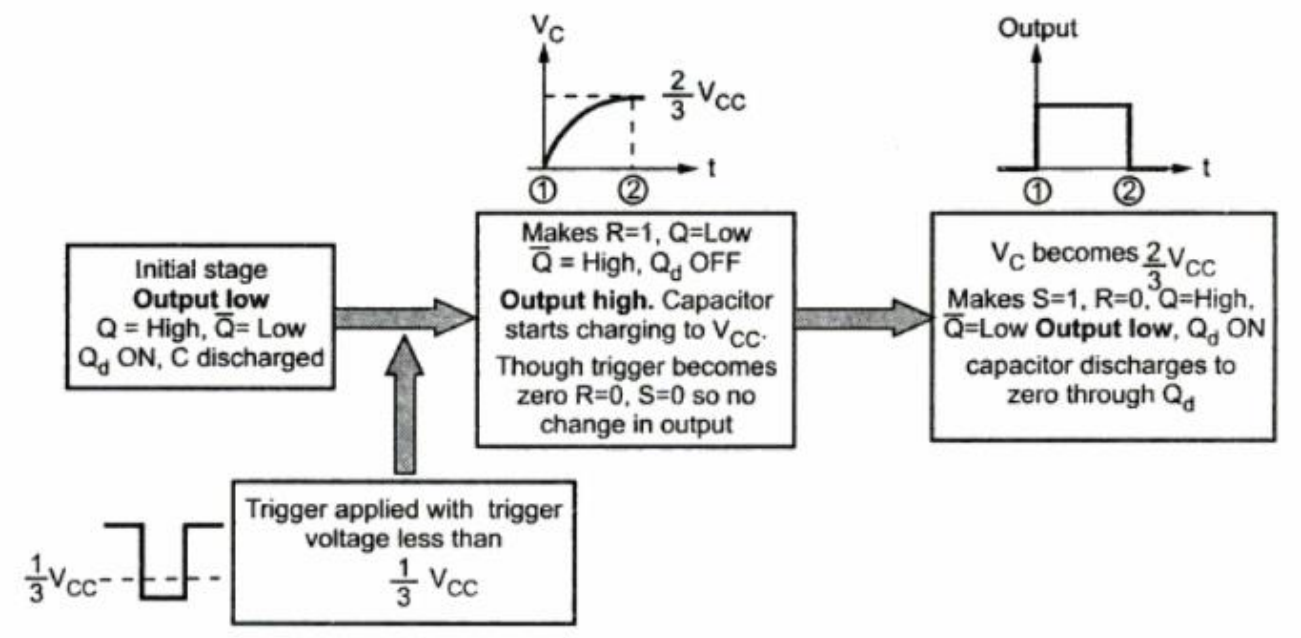


Fig. Waveforms of monostable operation



Applications:

- Frequency divider
- Pulse width modulation
- Missing pulse detector
- Linear ramp generator

Derivation of Pulse Width

The voltage across capacitor increases exponentially and is given by

$$V_C = V\,(1 - e^{-t/CR})$$

If $V_C = 2/3\ V_{CC}$

then $$\frac{2}{3} V_{CC} = V_{CC}\,(1 - e^{-t/CR})$$

$$\frac{2}{3} - 1 = -e^{-t/CR}$$

$$\frac{1}{3} = e^{-t/CR}$$

$$\therefore \quad -\frac{t}{CR} = -1.0986$$

$$\therefore \quad t = +1.0986\ CR$$

$$\therefore \quad t \approx 1.1\ CR$$

where C in farads, R in ohms, t in seconds.

Thus, we can say that voltage across capacitor will reach 2/3 V_{CC} in approximately 1.1 times, time constant i.e. 1.1 RC

Thus the pulse width denoted as W is given by,

$$W = 1.1\ RC.$$

Schematic Diagram

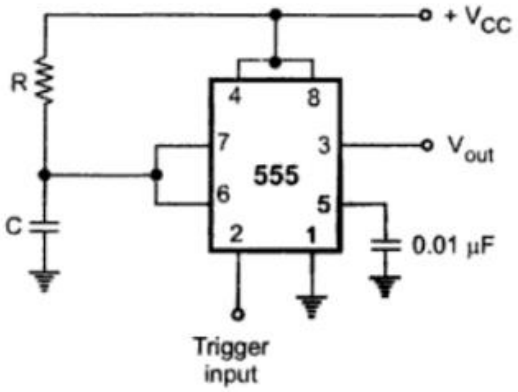


Fig. 6.13 555 timer as monostable multivibrator

Generally a schematic diagram of the IC 555 circuits is shown which does not include comparators, flip-flop etc. It only shows the external components to be connected to the 8 pins of IC 555. Thus, the schematic diagram of IC 555 as a monostable multivibrator is shown in the Fig. 6.13.

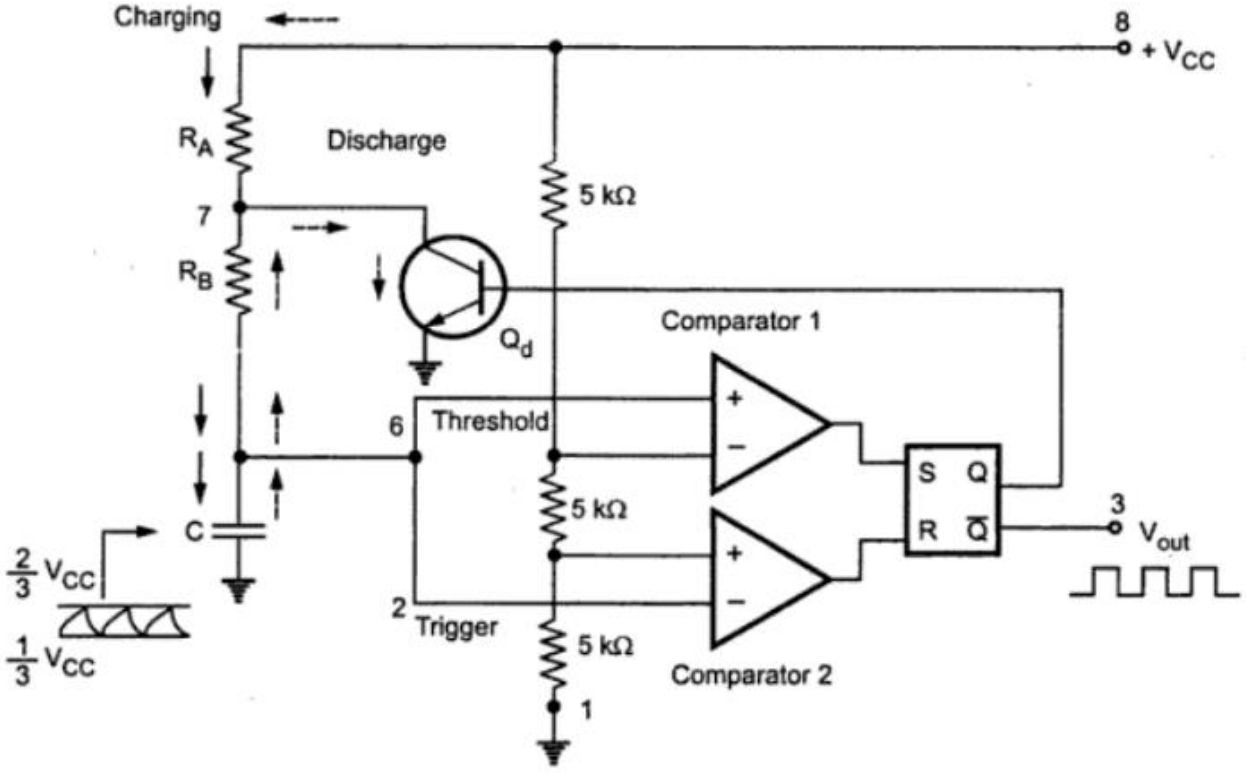
The external components R and C are shown. To avoid accidental reset, pin 4 is connected to pin 8 which is supply $+V_{CC}$. To have the noise filtering of control voltage, the pin 5 is grounded through a small capacitor of 0.01 μF.

8. Describe the functional block diagram of Astable mode of operation of IC 555 timer. Draw necessary waveform and expression.

Astable Multivibrator Using IC 555

The Fig. 6.22 shows the IC 555 connected as an astable multivibrator. The threshold input is connected to the trigger input. Two external resistances R_A, R_B and a capacitor C is used in the circuit.

This circuit has no stable state. The circuit changes its state alternately. Hence the operation is also called free running nonsinusoidal oscillator.



Operation

When the flip-flop is set, Q is high which drives the transistor Q_d in saturation and the capacitor gets discharged. Now the capacitor voltage is nothing but the trigger voltage. So while discharging, when it becomes less than 1/3 V_{CC}, comparator 2 output goes high. This resets the flip-flop hence Q goes low and $\overline{Q}$ goes high.

The low Q makes the transistor off. Thus capacitor starts charging through the resistances R_A, R_B and V_{CC}. The charging path is shown by thick arrows in the Fig. 6.22. As total resistance in the charging path is $(R_A + R_B)$, the charging time constant is $(R_A + R_B)$ C.

Now the capacitor voltage is also a threshold voltage. While charging, capacitor voltage increases i.e. the threshold voltage increases. When it exceeds 2/3 V_{CC}, then the comparator 1 output goes high which sets the flip-flop. The flip-flop output Q becomes high and output at pin 3 i.e. $\overline{Q}$ becomes low. High Q drives transistor Q_d in saturation and

capacitor starts discharging through resistance R_B and transistor Q_d. This path is shown by dotted arrows in the Fig. Thus the discharging time constant is R_B C. When capacitor voltage becomes less than 1/3 V_{CC}, comparator 2 output goes high, resetting the flip-flop. This cycle repeats.

Thus when capacitor is charging, output is high while when it is discharging the output is low. The output is a rectangular wave. The capacitor voltage is exponentially rising and falling. The waveforms are shown in the Fig.

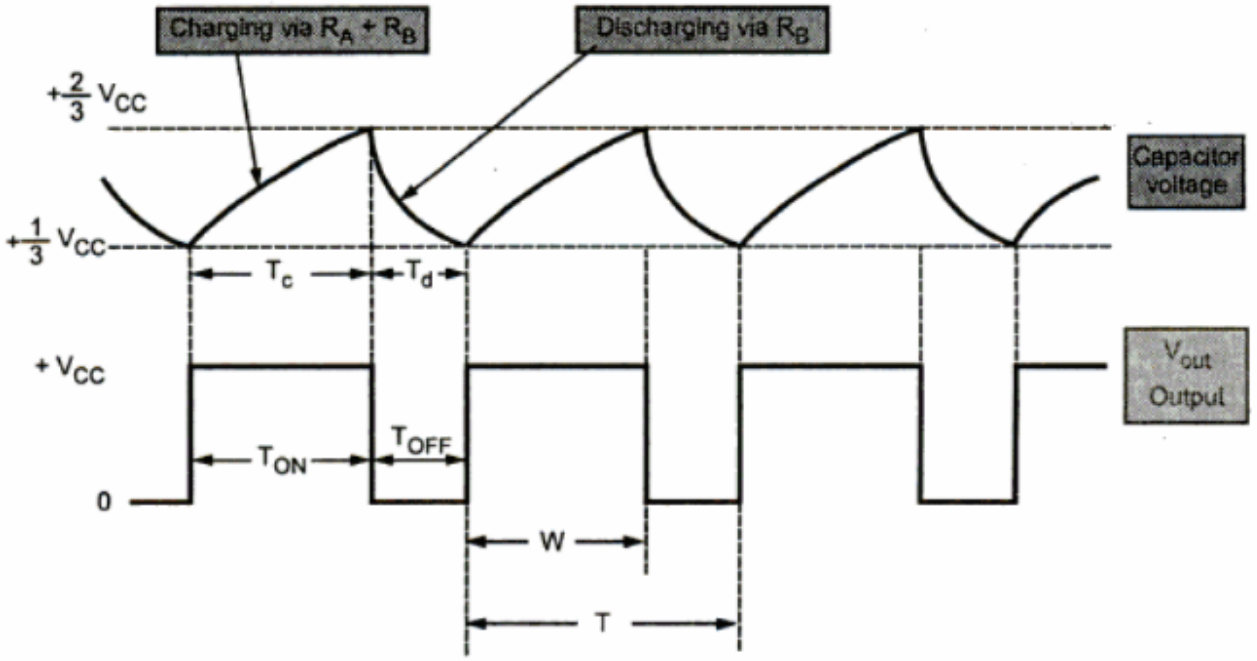


Fig. 4.24 Waveforms of astable operation

Duty Cycle

Generally the charging time constant is greater than the discharging time constant. Hence at the output, the waveform is not symmetric. The high output remains for longer period than low output. The ratio of high output period and low output period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON time i.e. high output to the total time of one cycle. As shown in the Fig. 7.25.

$$W = \text{time for output is high} = T_{ON}$$

$$T = \text{time of one cycle}$$

$$\therefore \quad D = \text{duty cycle} = \frac{W}{T}$$

$$\therefore \quad \boxed{\%\ D = \frac{W}{T} \times 100\ \%}$$

The charging time for the capacitor is given by,

$$T_c = \text{Charging time} = 0.693\ (R_A + R_B)\ C$$

While the discharge time is given by,

$$T_d = \text{Discharging time} = 0.693\ R_B\ C$$

Hence the time for one cycle is,

$$T = T_c + T_d = 0.693\ (R_A + R_B)\ C + 0.693\ R_B\ C$$

$$\therefore \quad \boxed{T = 0.693\,(R_A + 2\,R_B)\,C}$$

while $W = T_c = 0.693\,(R_A + R_B)\,C$

$$\therefore \quad \%D = \frac{W}{T} \times 100 = \frac{0.693\,(R_A + R_B)\,C}{0.693\,(R_A + 2\,R_B)\,C} \times 100$$

$$\therefore \quad \boxed{\%\,D = \frac{(R_A + R_B)}{(R_A + 2\,R_B)} \times 100}$$

While the frequency of oscillations is given by,

$$f = \frac{1}{T} = \frac{1}{0.693(R_A + 2\,R_B)C}$$

$$\therefore \quad \boxed{f = \frac{1.44}{(R_A + 2\,R_B)C}\ \text{Hz}}$$

If R_A is much smaller than R_B, duty cycle approaches to 50% and output waveform approaches to square wave.

Schematic Diagram

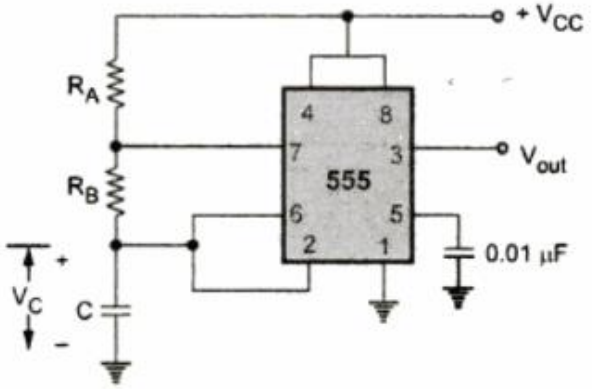


Fig. 7.26 555 timer as astable multivibrator

The Fig. 7.26 shows the schematic diagram of astable timer circuit. It shows only the external components R_A, R_B and C. The pin 4 is tied to pin 8 and pin 5 is grounded through a small capacitor.

The important application of astable multivibrator is voltage controlled oscillator (VCO).

Applications:

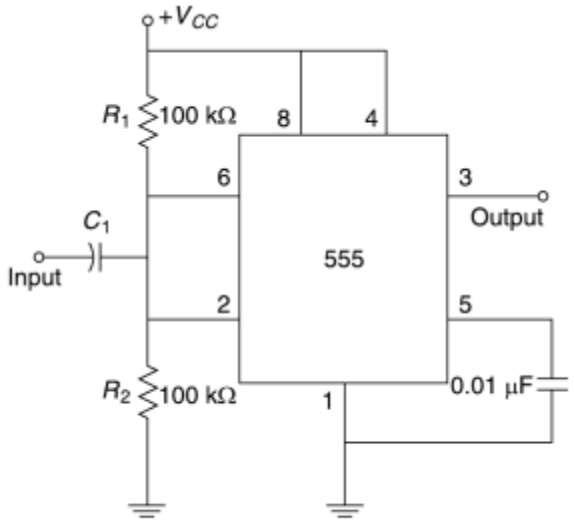
- Square wave generator
- Voltage controlled oscillator
- FSK generator
- Pulse position modulator

9. Describe the operation of Schmitt trigger using of IC 555 timer. Draw necessary waveform and expression.

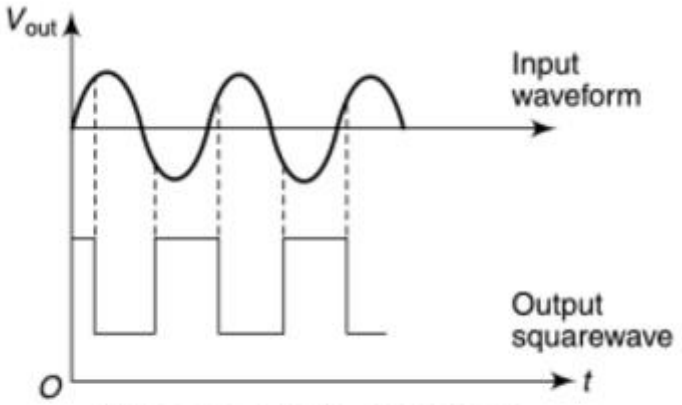
Schmitt trigger circuit is shown in Fig. 5.38(a) where the two internal comparator inputs (pins 2 and 6) are connected together and externally biased at $(1/2)V_{CC}$ through R_1 and R_2. Since the upper comparator at pin 6 will trip at $(2/3)V_{CC}$, and the lower comparator at $(1/3)V_{CC}$, the bias provided by R and R_2 is centered within these two thresholds.

A sine-wave input of sufficient amplitude to exceed the reference levels causes the internal flip-flop to alternatively set and reset, generating a square wave output. As long as R_1 equals R_2, the 555 timer will automatically be biased for any supply voltage in the range of 5 to 16V. From the curve shown in Fig. 5.38(b), it is observed that there is a 180° phase shift.

Unlike a conventional multivibrator type of square wave generator that divides the input frequency by 2, the main advantage of a Schmitt trigger is that it simply converts the sine-wave signal into a square wave signal without division.



(a) Circuit diagram



(b) Input and Output waveforms

Fig. 5.38 *Schmitt Trigger using IC 555 Timer*

10. **Describe the operation of Missing pulse detector using of IC 555 timer.**

Fig. 6.20 (a) shows the circuit diagram for missing pulse detector. When signal input is at ground level (0V), the emitter diode of transistor T_1 forward biases and clamps capacitor voltage V_C to 0.7 V. This forces output voltage to stay in its high state. When signal input goes high, the transistor cuts off and capacitor C begins to charge. If input signal again goes low before the 555 **completes** its timing cycle, the voltage across C is reset to 0.7 V. If, however, input signal does not go low before the 555 completes its timing cycle, the 555 enters its normal state and output voltage goes low. This is illustrated in Fig. 6.20 (b).

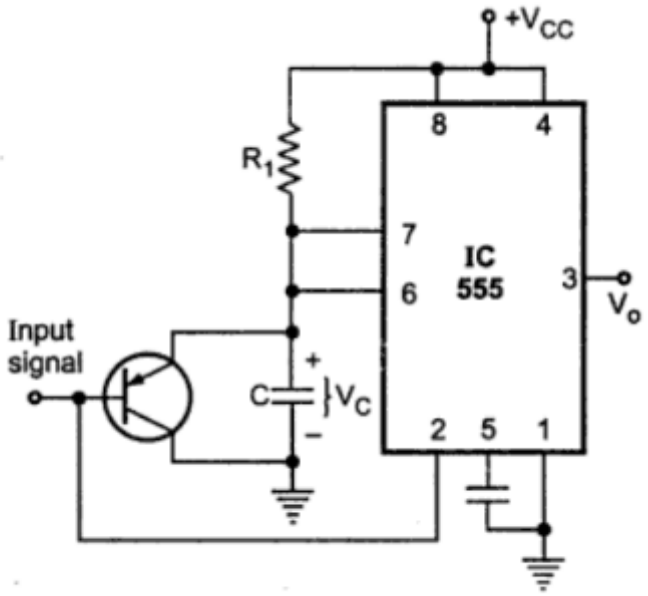


Fig. 6.20 (a) Missing pulse detector

For this circuit timing interval is adjusted such that it is slightly longer than the period of input signal. The continuous low going pulses of the period less than the timing interval do not allow capacitor to charge upto 2/3 V_{CC}. As a result, output voltage remains high. In case of missing pulse (pulse 4), capacitor charges upto 2/3 V_{CC} and forces output voltage in to its low state, as shown in the Fig. 6.20 (b). This type of circuit can be used to detect a missing heart beat.

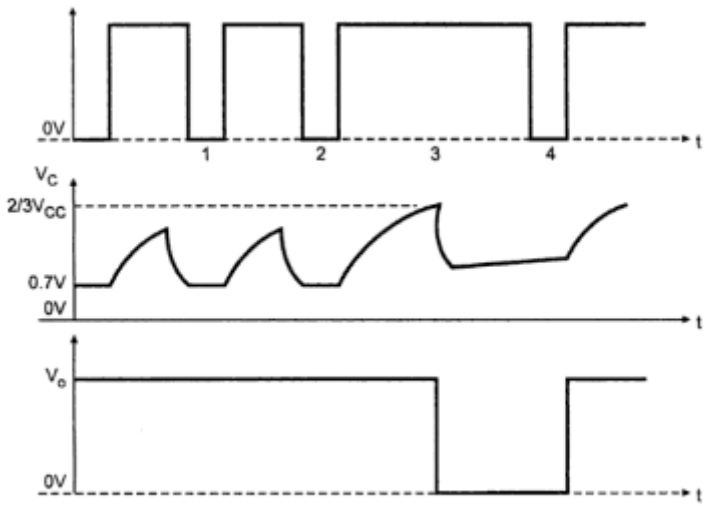


Fig. (b) Waveforms for missing pulse detector