BM T45 – LINEAR INTEGRATED CIRCUITS

UNIT-1

PART - A

1. List the advantage of integrated circuits over discrete component. (May 2014)

- Practically size of an IC is thousands of times smaller than the discrete circuits.
- ICs operate at low voltages.
- The cost of IC is very less
- The power consumption is less

2. What are the two main process of photolithography? (May 2014)

- Making of a photographic mask
- Photo etching

3. a) What is the advantage of dry itching? (Nov 2014)

b) What are the advantage of plasma etching? (May 2017)

- Eliminates handling of dangerous acids and solvents
- Uses small amounts of chemicals
- Isotropic or anisotropic etch profiles
- No unintentional prolongation of etching
- Better process control
- Ease of automation (e.g., cassette loading)

4. Design an amplifier with a gain of +5 using op-amp. (Nov 2014)

$$A_{CL} = 1 + R_f/R_1$$
$$5 = 1 + R_f/10\ \text{k}\Omega$$
$$R_f = 4 \times 10\ \text{k}\Omega = 40\ \text{k}\Omega$$

5. Write down the various processes used to fabricate IC's using silicon planar technology.(Nov 2015)

- Silicon wafer preparation
- Epitaxial growth
- Oxidation
- Photolithography

- Diffusion
- Ion implantation
- Isolation
- Metallization
- Assembly processing and packaging

6. List out the ideal characteristics of an Op-amp. (Nov 2015, Nov 2016, May 2018, May 2019, Sep 2020)

- Infinite open-loop gain $G = v_{out} / v_{in}$
- Zero input offset voltage
- Infinite output voltage range
- Zero output impedance R_{out}
- Zero noise
- Infinite common-mode rejection ratio(CMRR)
- Infinite power supply rejection ratio.

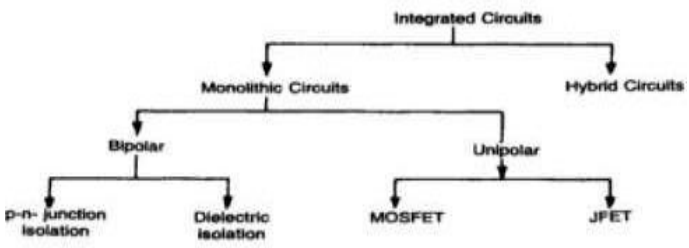
7. List the advantage of ion implantation. (Nov 2016)

- The impurity concentration is highly uniform typically within 1%,over the wafer
- The degree of uniformity is maintained same form wafer to wafer
- The layer can be formed anywhere within substrate
- The lateral spread is very small

8. Explain why inductors are difficult to fabricate in IC's. (May 2017)

- The property of inductor or inductance is that it would create flux lines or magnetic field around the line of conductor.
- The fabricated components in the integrated circuitry are very much susceptible to those flux lines and vulnerable to malfunctioning. This leads to gross failure of the IC.

9. Bring out the classification of IC's. (Nov2017)



10. Design an amplifier with a gain of -10 and input resistance equal to 10 kilo ohm. (Nov2017)

$$R_1 = 10\ \text{k}\Omega$$
$$R_f = -A_{CL}\, R_1$$
$$= -(-10) \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$$

11. Give the difference between monolithic and hybrid IC's. (May 2018)

Monolithic ICs	Hybrid ICs
Monolithic integrated circuits are fabricated entirely on a single chips.	Hybrid integrated circuits are fabricated by inter-connecting a number of individual chips.
Small in size as compared to hybrid ICs	Large in size as compared to monolithic ICs
Monolithic ICs are expensive.	Hybrid ICs are less expensive.
Speed is high as compared to hybrid ICs.	Speed is low as compared to monolithic ICs.

12. What is meant by parasitic capacitance? (Nov 2018)

Parasitic capacitance, or stray capacitance is an unavoidable and usually unwanted capacitance that exists between the parts of an electronic component or circuit simply because of their proximity to each other.

13. Name the different types of IC packages. (May 2019)

- Metal can package
- Dual-in-line package
- Ceramic flat package

14. State the limitations of IC technology. (Sep 2020)

- Some components like transformers and inductors cannot be integrated into an IC.
- High grade P-N-P assembly is not possible.
- It is difficult to achieve low temperature coefficient.
- It is difficult to fabricate an IC with low noise.
- There is a large value of saturation resistance of transistors.

PART – B

1. Explain in detail the AC characteristics of an Op-amp. (May 2014, Nov 2015)

Ac characteristics:

For small signal sinusoidal applications the a.c. characteristics are

1. Frequency response 2. Slew rate

1. Frequency response:

- An ideal op-amp has infinite band width that is open loop gain is 90dB with d.c. signal and this gain should remain the same through audio and radio frequency.
- But practically op-amp gain decreases at high frequency. This is due to a capacitive component in the equivalent circuit of op-amp.
- Due to R0C, the gain decreases by 20 dB per decay and the frequency is said to be brake or corner frequency and is given by

f1= 1/ (2*3.14*R0*C)

|A|= A0*L/ (1+ (f/f1) ^2)

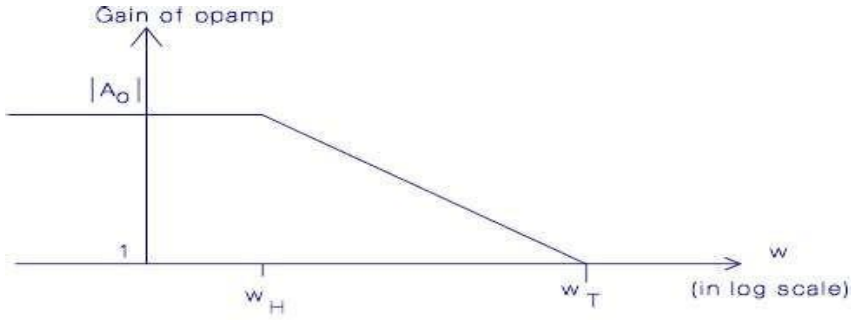


Fig. 1.3: Change in gain of Opamp with Frequency

$$= 1 = \left| \frac{A_o}{1 + \frac{jw_T}{w_H}} \right| \cdot \frac{A_o}{1 + \frac{jw}{w_H}} \cdot (jw_T \rangle w) = A(Aj$$

2. Slew rate:

- The rate of change of output voltage due to the step input voltage and is usually specified as V/micro sec.

For example: 1V/micro sec. slew rate denotes the output rises or falls by 1 volts in 1 micro seconds.

The rate at which the voltage across the capacitor dVc/dt is given by

dVc/dt = I/C

Slew rate SR dVc/dt|max= Imax/ C

For IC741

Imax= 15 micro amps, C= 30 Pico farad

Slew rate = 0.5V/ micro sec.

2.a) Explain the operation of differential amplifier. (May 2014)

b) Explain the modes of operation of operational amplifier. (Nov 2014)

c) Compare the different modes of operational amplifier. (May 2017)

d) Draw the circuit diagram of an Op-amp differential mode and derive an expression for tile output in terms of the input. (May 2018)

e) Draw the circuits for inverting, non-inverting and difference amplifier using Op-amp. Derive an expression for gain for these three configurations. (May 2019, Sep 2020)

f) With neat circuit diagram, explain the working of inverting amplifier and obtain an expression for its gain. (Nov 2018)

g) Sketch the equivalent circuit diagram of an ideal operational amplifier and state its characteristics.

Inverting Amplifier:

- In Fig output voltage v_0 is fed back to the inverting input terminal through the R_f-R_1 network where R_f is the feedback resistor.
- Input signal v_i is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

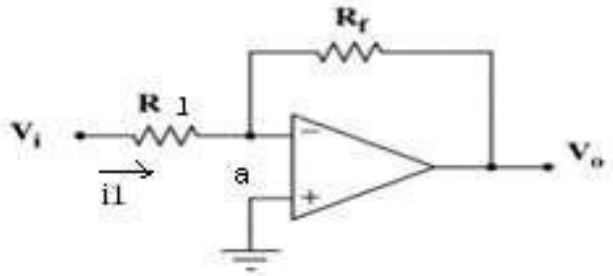


Fig. Inverting Amplifier Circuit

$$\frac{V_a - V_i}{R_i} + \frac{V_a - V_o}{R_f} = 0$$

Sub $V_a = 0$

$$\frac{0 - V_i}{R_i} + \frac{0 - V_o}{R_f} = 0$$

$$\frac{V_i}{R_i} + \frac{V_o}{R_f} = 0$$

$$\frac{V_o}{R_f} = \frac{-V_i}{R_i}$$

$$\boxed{V_o = -\frac{R_f}{R_i} V_i}$$

∴ gain of the inverting amp

$$\boxed{A_V = \frac{V_o}{V_i} = -R_f/R_i}$$

Non inverting amplifier:

- If a signal is applied to the non-inverting input terminal and feed back is given as shown in Fig the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier.
- It may also be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal

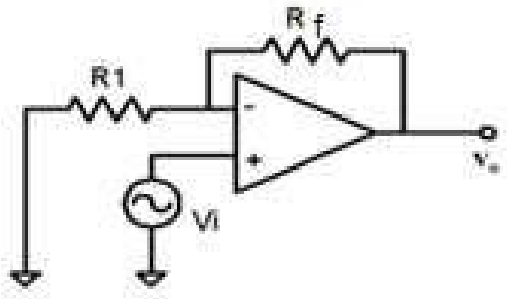


Fig. Non –Inverting Amplifier Circuit

$$V_i = \frac{V_o}{R_i + R_f} R_i$$

$$\frac{V_o}{V_i} = \frac{R_i + R_f}{R_i} = \frac{R_i}{R_i} + \frac{R_f}{R_i}$$

$$\boxed{\frac{V_o}{V_i} = 1 + \frac{R_f}{R_i}}$$

∴ gain of the non inverting amp

$$\boxed{A_V = 1 + \frac{R_f}{R_i}}$$

- As the differential voltage vd at the input terminal of op-amp is zero, the voltage at node 'a' is v_i, same as the input voltage applied to non-inverting input terminal.

Voltage follower

$$R_f = 0$$

$$R_i = \infty$$

$$\boxed{V_o = V_i}$$

Differential amplifier

A differential amplifier is a circuit that can accept two input signals and amplify the difference between these two input signals.

Fig.shows the block diagram of a differential amplifier .

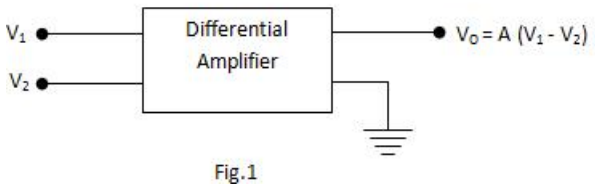


Fig.1

There are two input voltages v_1 and v_2.

The nodal equation at 'a' is

$$\frac{V_a - V_1}{R_1} + \frac{V_a - V_0}{R_2} = 0$$

$$\frac{V_a}{R_1} - \frac{V_1}{R_1} + \frac{V_a}{R_2} - \frac{V_0}{R_2} = 0$$

$$V_a\left(\tfrac{1}{R_1} + \tfrac{1}{R_2}\right) - \frac{V_1}{R_1} - \frac{V_0}{R_2} = 0 \quad \text{---(1)}$$

The nodal equation at 'b' is

$$\frac{V_b - V_1}{R_1} + \frac{V_b - 0}{R_2} = 0$$

Since, $V_a = V_b$

$$V_a\left(\tfrac{1}{R_1} + \tfrac{1}{R_2}\right) - \frac{V_1}{R_1} = 0 \quad \text{---(2)}$$

by solving equ (1) & (2), we get

(1) - (2) $\Rightarrow$ $V_a\left(\tfrac{1}{R_1} + \tfrac{1}{R_2}\right) - \frac{V_2}{R_1} - \frac{V_0}{R_2} = 0$

$V_a\left(\tfrac{1}{R_1} + \tfrac{1}{R_2}\right) - \frac{V_1}{R_1} = 0$

$$-\frac{V_0}{R_1} - \frac{V_0}{R_2} + \frac{V_1}{R_1}$$

$$\frac{V_0}{R_2} = \frac{V_1}{R_1} - \frac{V_2}{R_1}$$

$$\boxed{V_0 = \frac{R_2}{R_1}(V_1 - V_2)}$$

$$V_0 = A_1 V_1 + A_2 V_2$$

Since,

$$V_{CM} = \frac{(V_1 + V_2)}{2} \quad \text{---(1)}$$

$$V_d = V_1 - V_2 \quad \text{---(2)}$$

(1) $\Rightarrow$ $V_1 + V_2 = 2V_{CM}$

(2) $\Rightarrow$ $V_1 - V_2 = V_d$

$$2V_1 = 2V_{CM} + V_d$$

$$\boxed{V_1 = V_{CM} + \frac{V_d}{2}}$$

Sub, V_1 value in equ (2)

$$V_d = V_{CM} + \frac{V_d}{2} - V_2$$

$$\boxed{V_2 = V_{CM} - \frac{V_d}{2}}$$

Sub the value of V_1 & V_2 in V_0

$$V_0 = A_1 V_1 + A_2 V_2$$

$$= A_1\left(V_{CM} + \frac{V_d}{2}\right) + A_2\left(V_{CM} - \frac{V_d}{2}\right)$$

$$= V_{CM}(A_1 + A_2) + \frac{V_d}{2}(A_1 - A_2)$$

$$\boxed{V_0 = V_{CM} A_{CM} + V_d A_{DM}}$$

where $A_{CM} = A_1 + A_2$

$$A_{DM} = \frac{A_1 - A_2}{2}$$

This amplifier amplifies the difference between the two input voltages.

Therefore the output voltage is,

$$v_o = A(v_1 - v_2)$$

Where A is the voltage gain of the amplifier.

Operation of Differential Amplifier

For simplicity, we shall discuss the operation of single-ended input and double-ended outputDA.

Case – 1:

Suppose the signal is applied to input 1 (i.e. base of transistor Q_1) and input 2(i.e.base of transistor Q_2) is grounded as shown in fig

The transistor Q_1 will act in two ways: as a common emitter amplifier and as a common collector amplifier.

As a common emitter amplifier, the input signal to Q_1 will appear at output 1 (i.e. collector ofQ_1) as amplified inverted signal.

As a common collector amplifier, the signal appears on the emitter of Q_1 in phase with the input and only slightly smaller.

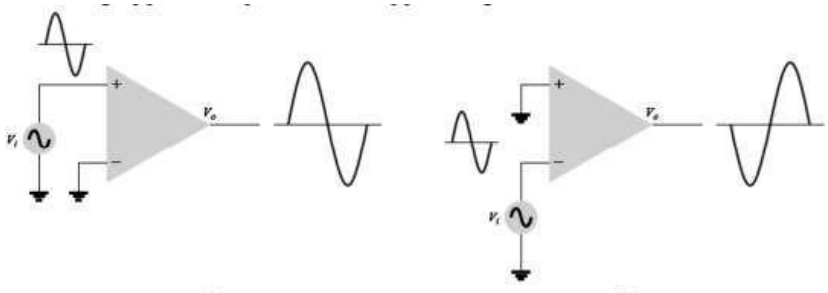
Since the emitters of Q_1 and Q_2 are common, the emitter signal becomes input to Q_2.Therefore,

Q_2 functions as a common base amplifier.

As a result, the signal on the emitter Q_2 will be amplified and appears on output 2 (i.e. collector of Q_2) in phase with the emitter signal and hence in phase with the input signal (signal at input 1).

The differential amplifier exhibits three modes of operation based on the type of input (and/or output) signals. These modes are **single-ended, double-ended or differential, and common**. Since the differential amplifier is the input stage of the op-amp, the op-amp exhibits the same modes

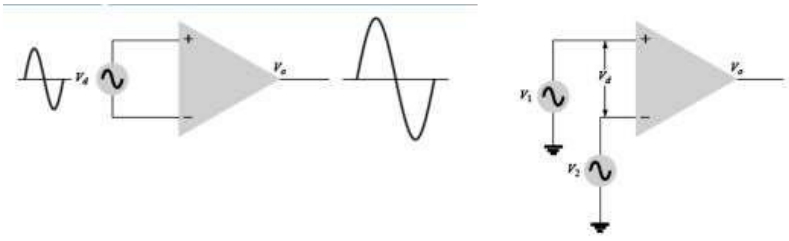
Single-Ended Input: Single-ended input operation results when the input signal is connected to one input with the other input connected to ground. Fig. 1-4 shows the signals connected for this operation. In Fig. 1-4(a), the input is applied to the plus input (with minus input at ground), which results in an output having the same polarity as the applied input signal. Fig. 1-4(b) shows an input signal applied to the minus input, the output then being opposite in phase to the applied signal.



(a) (b)

Fig. 1-4

Double-Ended (Differential) Input: In addition to using only one input, it is possible to apply signals at each input-this being a double-ended operation. Fig. 1-5(a) shows an input, Vd, applied between the two input terminals (recall that neither input is at ground), with the resulting amplified output in phase with that applied between the plus and minus inputs. Fig. 1.5(b) shows the same action resulting when two separate signals are applied to the inputs, the difference signal being Vi1 − Vi2.



(a) (b)

Fig. 1-5

Double-Ended Output: While the operation discussed so far had a single output, the op-amp can also be operated with opposite outputs, as shown in Fig. 1-6(a). An input applied to either input will result in outputs from both output terminals, these outputs always being opposite in polarity. Fig. 1-6(b) shows a single-ended input with a doubleended output. As shown, the signal applied to the plus input results in two amplified outputs of opposite polarity. Fig. 1-6(c) shows the same operation with a single output measured between output terminals (not with

respect to ground). This difference output signal is Vo1 − Vo2. The difference output is also referred to as a floating signal since neither output terminal is the ground (reference) terminal. Notice that the difference output is twice as large as either Vo1 or Vo2 since they are of opposite polarity and subtracting them results in twice their amplitude. Fig. 1-6(d) shows a differential input, differential output operation. The input is applied between the two input terminals and the output taken from between the two output terminals. This is fully differential operation.

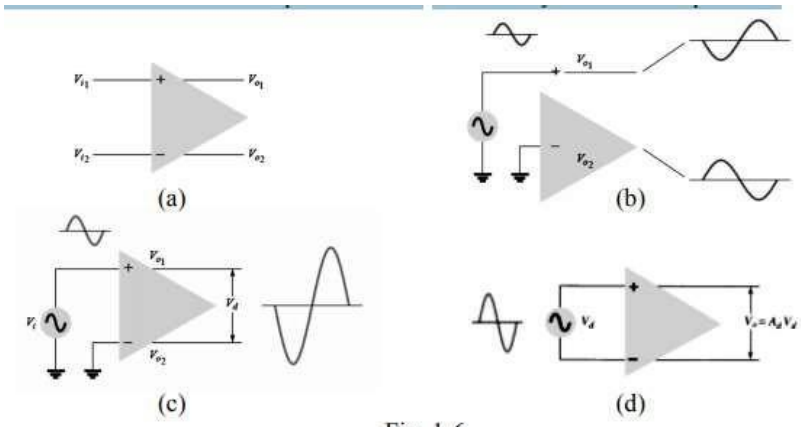


Fig. 1-6

Common-Mode Operation: When the same input signals are applied to both inputs, common-mode operation results, as shown in Fig. 1-7. Ideally, the two inputs are equally amplified, and since they result in opposite polarity signals at the output, these signals cancel, resulting in 0-V output. Practically, a small output signal will result.

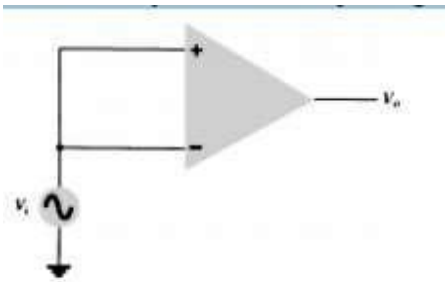


Fig. 1-7

Common-Mode Rejection: A significant feature of a differential connection is that the signals which are opposite at the inputs are highly amplified, while those which are common to the two inputs are only slightly amplified-the overall operation being to amplify the difference signal while rejecting the common signal at the two inputs. Since noise (any unwanted input signal) is generally common to both inputs, the differential connection tends to provide

attenuation of this unwanted input while providing an amplified output of the difference signal applied to the inputs. This operating feature, referred to as common-mode rejection.

2. a) Explain the fabrication of a typical circuit with neat sketch. (Nov 2014, Nov 2017)

b) Explain the basic process used in silicon planar technology with neat diagram. (Nov 2015, May 2018, Nov2018)

c) Describe the epitaxial growth process employed in IC fabrication. (Nov 2016)

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail

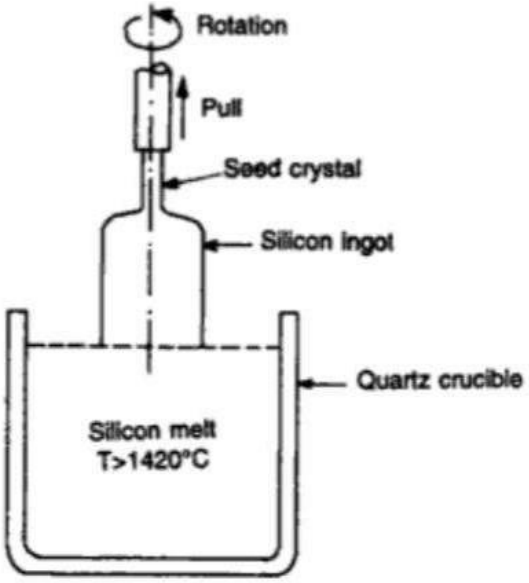
1. Silicon wafer Preparation

The following steps are used in the preparation of Si-wafers

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant

is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.



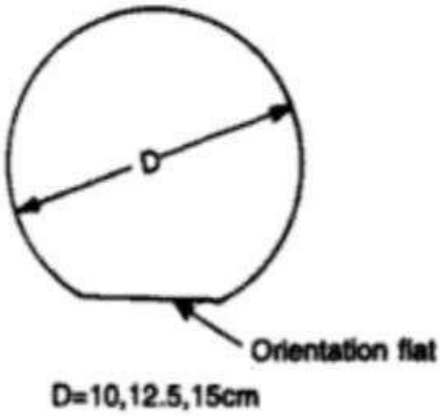


Fig. 1.6 Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

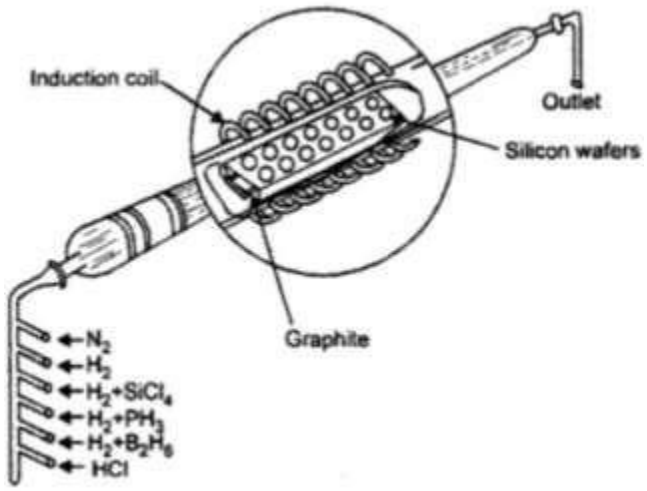
2. Epitaxial growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiC_4 + 2H_2 \underset{}{\overset{1200°C}{\rightleftharpoons}} Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the *n*-type and bi-borane (B_2H_6) for *p*-type doping into the silicon-tetrachloride hydrogen gas stream.



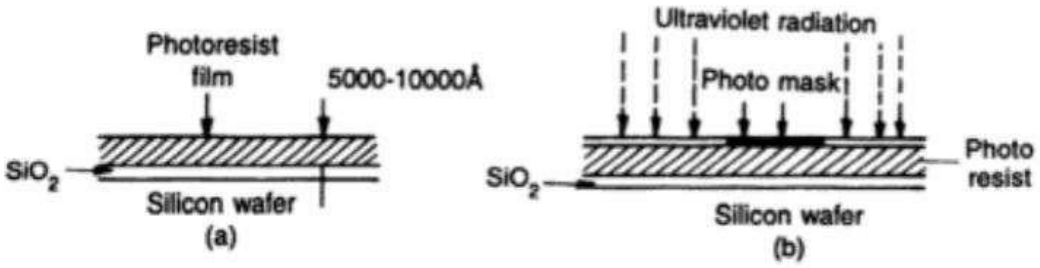
3. Oxidation

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.
2. By selective etching of SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

4. Photolithography

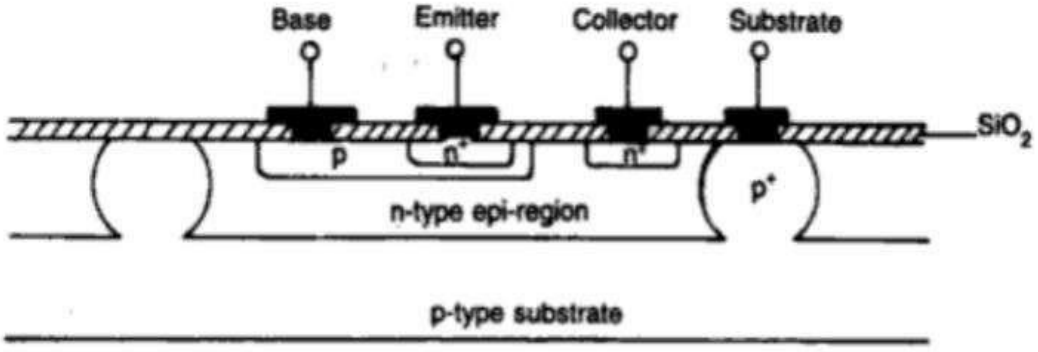
However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become possible to produce device dimension down to submicron range (< 1 μm).

Photolithography involves two processes, namely:
Making of a photographic mask
Photo etching



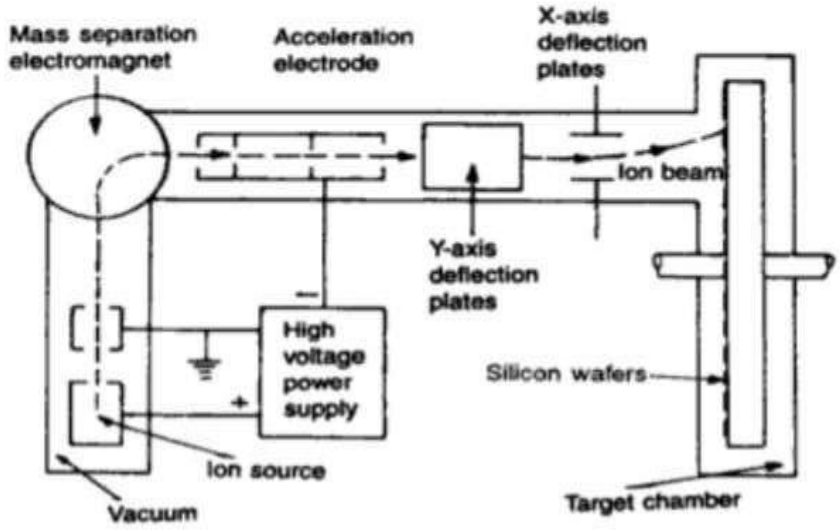
5. Diffusion

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the Silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20″ length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C.



6. Ion implantation

1. It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.



7. Isolation Techniques

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques namely:

pn junction isolation
Dielectric isolation

8. Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages.

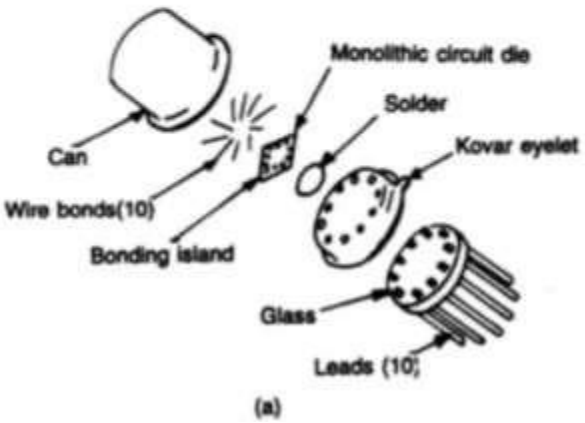
1. It is relatively a good conductor.
2. It is easy to deposit aluminium films using vacuum deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, non-rectifying (i.e. ohmic) contact with *p*-type silicon and the heavily doped *n*-type silicon.

9. Assembly processing and packaging

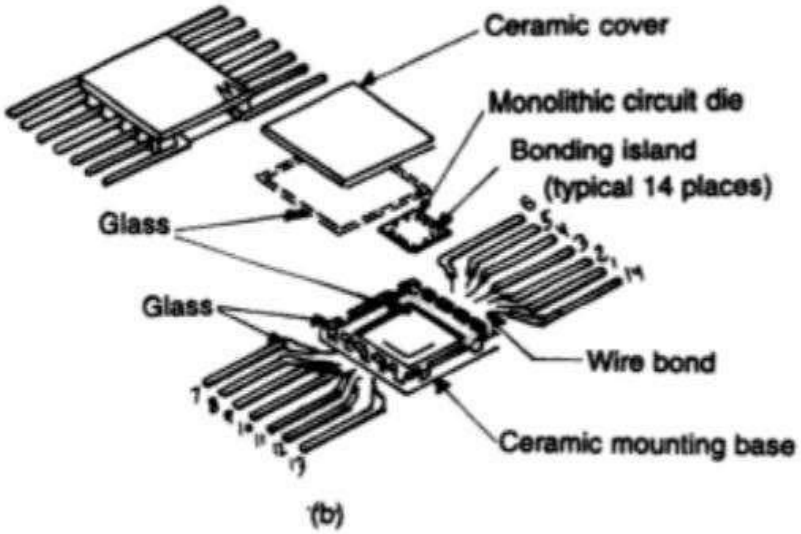
There are three different package configurations available.

1. TO-5 glass metal package
2. Ceramic flat package
3. Dual-in-line (ceramic or plastic type)

TO-5 packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but



(a)



3. a.List the DC characteristics of an Op-amp.

b. Write short notes on the following non-ideal DC characteristics with necessary circuit diagrams and expressions. (Nov 2017)

a) Input offset current

b) Input offset voltage

DC Characteristics:

- An ideal op-amp draws no current from source and its response is independent of temperature.
- Practical op-amp has some dc voltage at the output even with both the inputs are grounded.
- The non-ideal dc characteristics that add error components to the dc output voltage are

a. Input bias current

b. Input offset voltage

c. Input offset current

d. Thermal drift

Input bias current:

- Ideal op-amp draws no current from the input terminal.
- A practical op-amp conducts a small value of dc current to bias the input transistors.
- In fig 1.1,the base current entering into the inverting and non-inverting terminals are $I_{\bar{B}}$ and I_B^+ respectively. I_B^- and I_B^+ are not exactly equal due to internal imbalance between the two inputs.

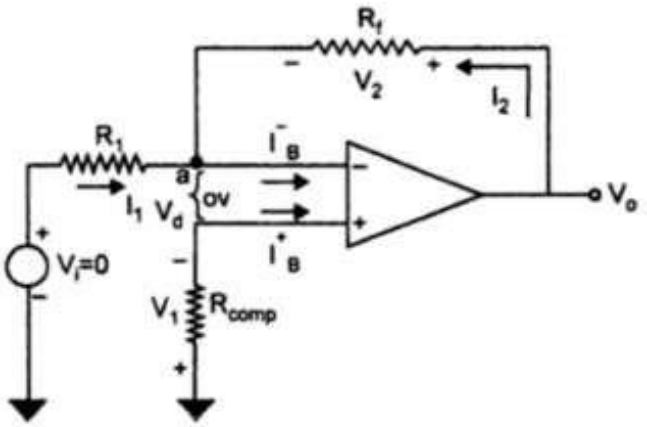


Fig 1.1 Input bias current and Bias current compensation

- Input bias current I_B is defined as the average value of the base currents entering into the terminals of an op-amp during the input bias current.

IB=IB++IB-2 (1.1)

It is compensated by Rcomp= R1|| R2 between non inverting terminal and ground

R1RFR1+RF= RCOMP (1.2)

Input offset current:

- Bias current compensation will work efficiently if both the bias currents I_B^+ and I_B^- are equal.
- The input transistors cannot be made identical hence there will be some difference between I_B^+ and I_B^-. This difference is called offset current I_{OS}.

IOS= IB+- IB+ (1.3)

- The absolute value indicates that there is no way to predict which of the current is large

Input offset voltage

- It is defined as the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier (op-amp), to make the output zero
- This occurs due to unavoidable imbalances inside the op-amp .

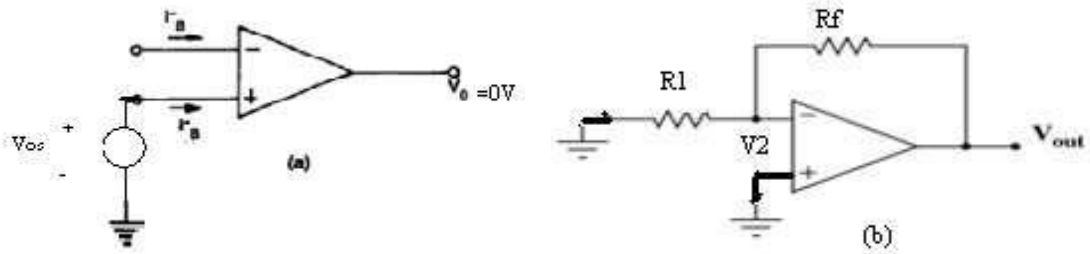


Fig 1.2 a) Op-amp showing input and output offset voltage b) Equivalent circuit for Vi=0

By voltage divider rule V2 is given by,

V2=(R1V0.)(R1.+Rf). (1.4)

Vo=(R1.+Rf) V2(R1.) (1.5)

Vo=1+Rf.R1.V2. (1.6)

Vos=V1-V2 (1.7)

We know that, $V_1=0$

Vos=0 - V2

Vos=V2 (1.8)

Therefore to make input offset voltage to be zero Vos= V_2

Thermal drift:

- Thermal drift is defined as the average rate of change of input offset voltage or offset current or bias current per unit change in temperature
- Bias current, offset current and offset voltage change with temperature. .

- Offset current drift is expressed in nA/^{0}C and offset voltage drift in mV/^{0}C.
- For the 741c, the input resistance is 2Mohms.

Output Voltage Swing

The output voltage swing between -13V to +13V

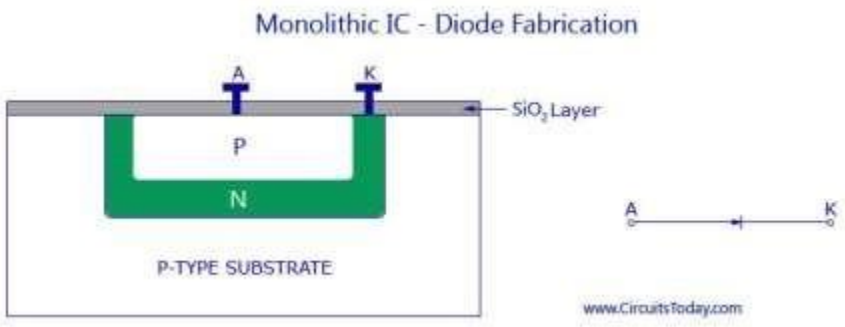
4. a) Explain how a diode, a resistor and a capacitor are fabricated in IC.(Nov 2016)

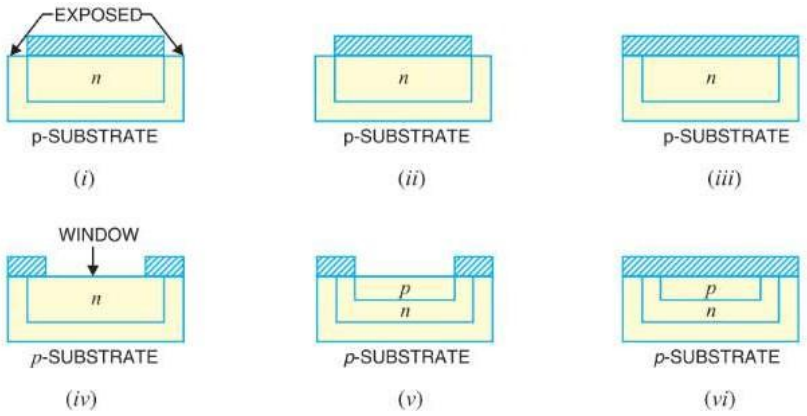
b) Explain how a monolithic capacitor can be fabricated.(Nov 2019)

c) Explain the fabrication of a typical circuit with neat sketch. (Nov 2014, Nov 2017)

Diodes

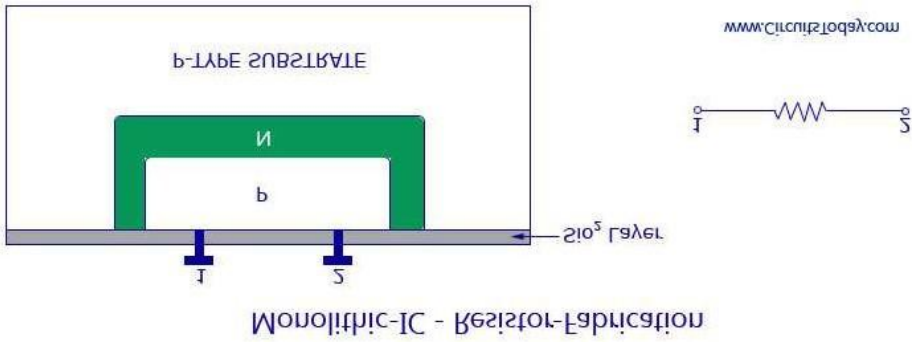
They are also fabricated by the same diffusion process as transistors are. The only difference is that only two of the regions are used to form one P-N junction. In figure, collector-base junction of the transistor is used as a diode. Anode of the diode is formed during the base diffusion of the transistor and the collector region of the transistor becomes the cathode of the diode. For high speed switching emitter base junction is used as a diode.

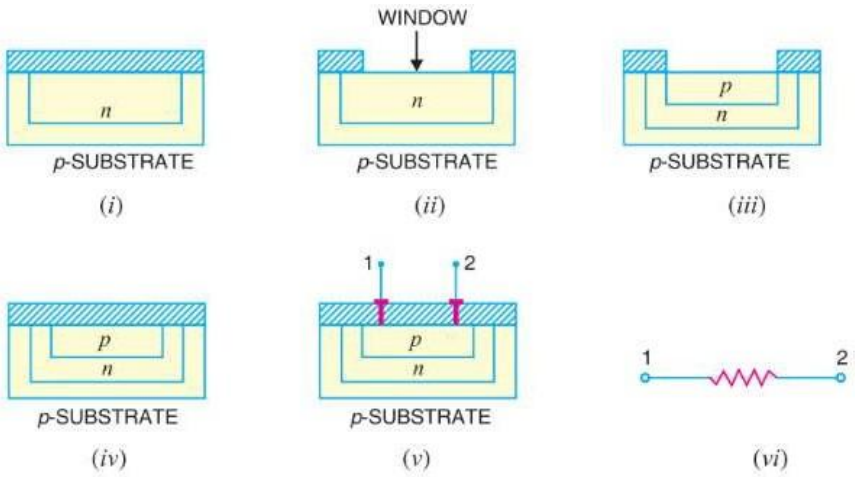




Resistors

The resistors used in IC's are given their respective ohmic value by varying the concentration of doping impurity and depth of diffusion. The range of resistor values that may be produced by the diffusion process varies from ohms to hundreds of kilohms. The typical tolerance, however, may be no better than ± 5%, and may even be as high as ± 20%. On the other hand, if all the resistors are diffused at the same time, then the tolerance ratio may be good. Most resistors are formed during the base diffusion of the integrated transistor, as shown in figure below. This is because it is the highest resistivity region. For low resistance values, emitter region is used as it has much lower resistivity.

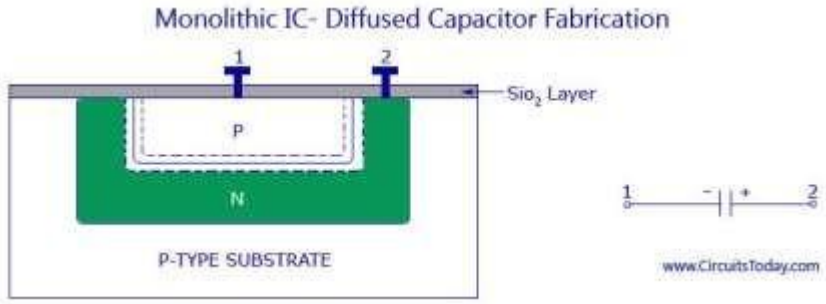




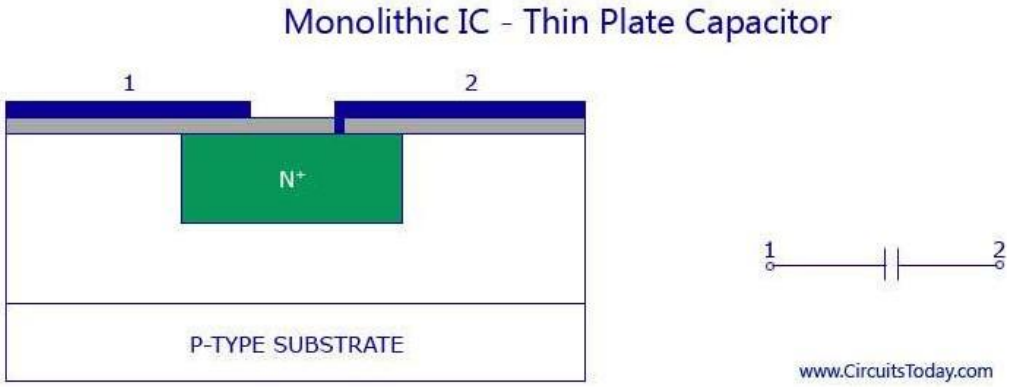
Capacitors

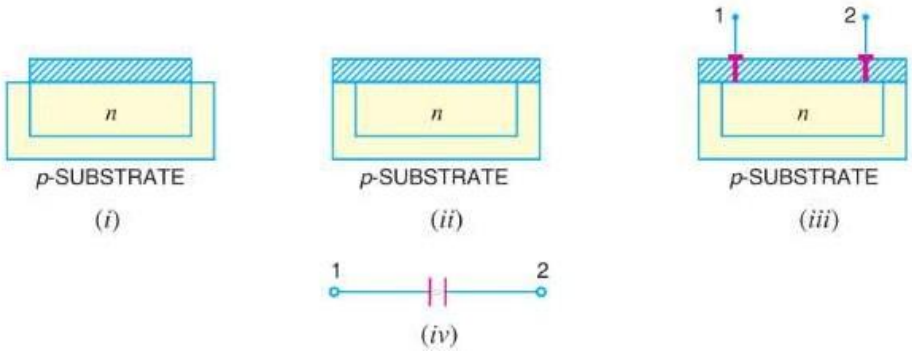
The figure below shows the P and N-regions forming the capacitor plates. The dielectric of the capacitor is the depletion region between them.

All P-N junctions have capacitance so capacitors may be produced by fabricating junctions. The amount of change in the reverse bias varies the value of junction capacitance and also the depletion width. The value may be as less as 100 picoFarads.



Using the silicon dioxide as a dielectric may also be a way to fabricate capacitors. One plate of the capacitors is formed by diffusing a heavily doped N-region. The other plate of the capacitor is formed by depositing a film of aluminium on the silicon dioxide dielectric on the wafer surface. For such a capacitor, a voltage of any polarity can be used, and when comparing a diffused capacitor with such a capacitor the diffused capacitor may have very small values of breakdown voltage.

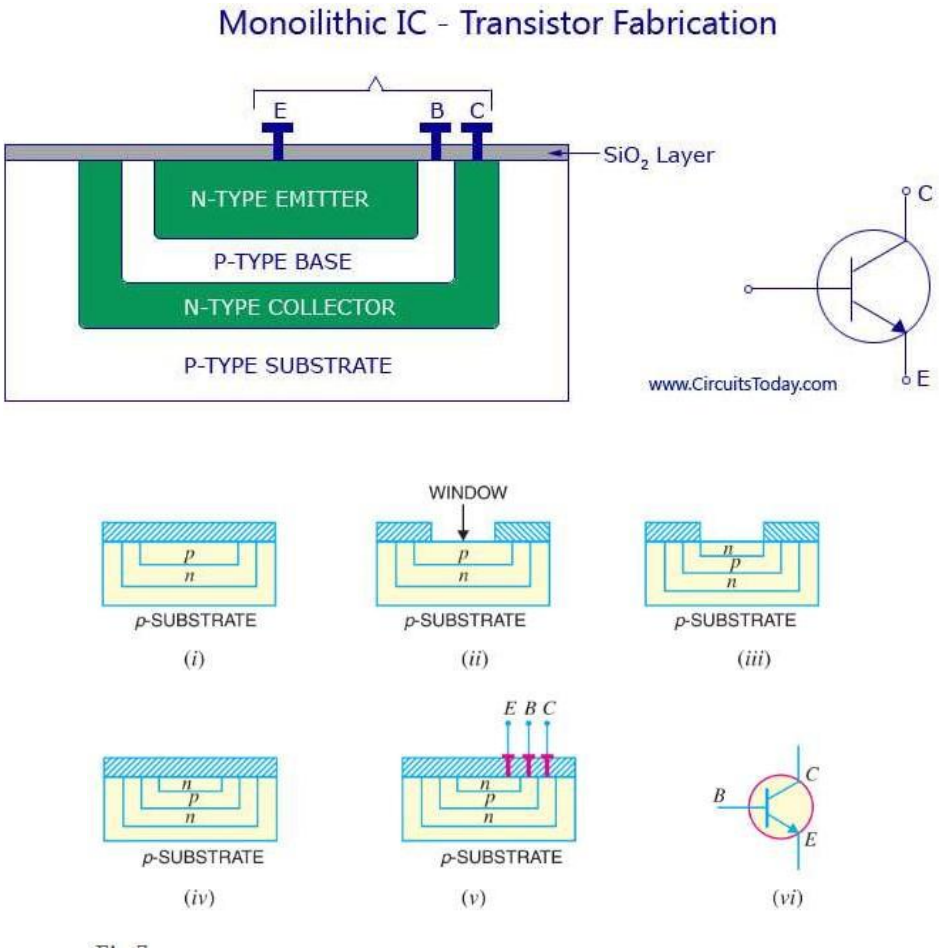




5. Describe briefly about the fabrication methods for transistors and diodes. (May 2017)

Transistors

The fabrication process of a transistor is shown in the figure below. A P-type substrate is first grown and then the collector, emitter, and base regions are diffused on top of it as shown in the figure. The surface terminals for these regions are also provided for connection.



Both transistors and diodes are fabricated by using the epitaxial planar diffusion process that is explained earlier. In case of discrete transistors, the P-type substrate is considered as the collector. `But this is not possible in monolithic IC's, as all the transistors connected on one P-type substrate would have their collectors connected together. This is why separate collector regions are diffused into the substrate.

Even though separate collector regions are formed, they are not completely isolated from the substrate. For proper functioning of the circuit it is necessary that the P-type substrate is always kept negative with respect to the transistor collector. This is achieved by connecting the

substrate to the most negative terminal of the circuit supply. The unwanted or parasitic junctions, even when reverse-biased, can still affect the circuit performance adversely. The junction reverse leakage current can cause a serious problem in circuits operating at very low current levels. The capacitance of the reverse-biased junction may affect the circuit high-frequency performance, and the junction break down voltage imposes limits on the usable level of supply voltage. All these adverse effects can be reduced to the minimum if highly resistive material is employed for the substrate. If the substrate is very lightly doped, it will behave almost as an insulator.

6. a) Explain the various steps utilized in converting a typical circuit into a monolithic IC. (Nov 2017)

b) Explain the fabrication of a typical circuit with neat sketch. (Nov 2014, Nov 2017)

Monolithic IC Manufacturing Process

For the manufacture and production of the monolithic IC, all circuit components and their interconnections are to be formed in a single thin wafer. The different processes carried out for achieving this are explained below.

1. P-layer Substrate Manufacture

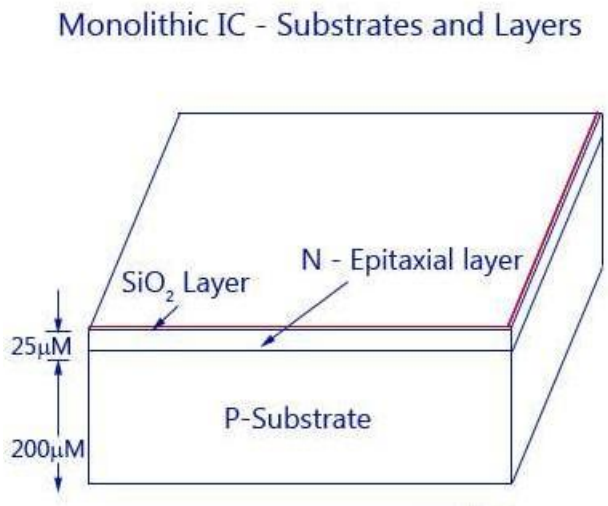
Being the base layer of the IC, the P-type is silicon is first built for the IC. A silicon crystal of P-type is grown in dimensions of 250mm length and 25mm diameter. The silicon is then cut into thin slices with high precision using a diamond saw. Each wafer will precisely have a thickness of 200 micrometer and a diameter of 25 mm. These thin slices are termed wafers. These wafers may be circular or rectangular in shape with respect to the shape of the IC. After cutting hundreds of them each wafer is polished and cleaned to form a P-type substrate layer.

2. N-type Epitaxial Growth

The epitaxial groth process of a low resistive N-type over a high resistive P-type is to be carried out. This is done by placing the n-type layer on top of the P-type and heating then inside a diffusion furnace at very high temperature (nearly 1200C). After heating, a gas mixture f Silicon atoms and pentavalent atoms are also passed over the layer. This forms the epitaxial layer on the substrate. All the components required for the circuit are built on top of this layer. The layer is then cooled down, polished and cleaned.

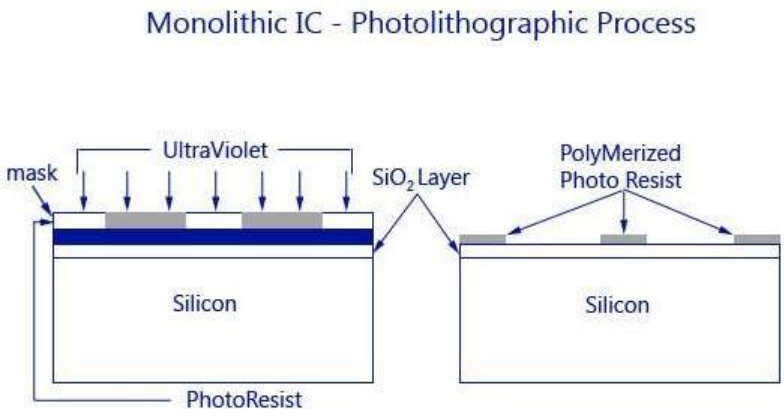
3. The Silicon Dioxide Insulation Layer

As explained above, this layer is required contamination of the N-layer epitaxy. This layer is only 1 micrometer thin and is grown by exposing the epitaxial layer to oxygen atmosphere at 1000C. A detailed image showing the P-type, N-type epitaxial layer and SiO2 layer is given below.



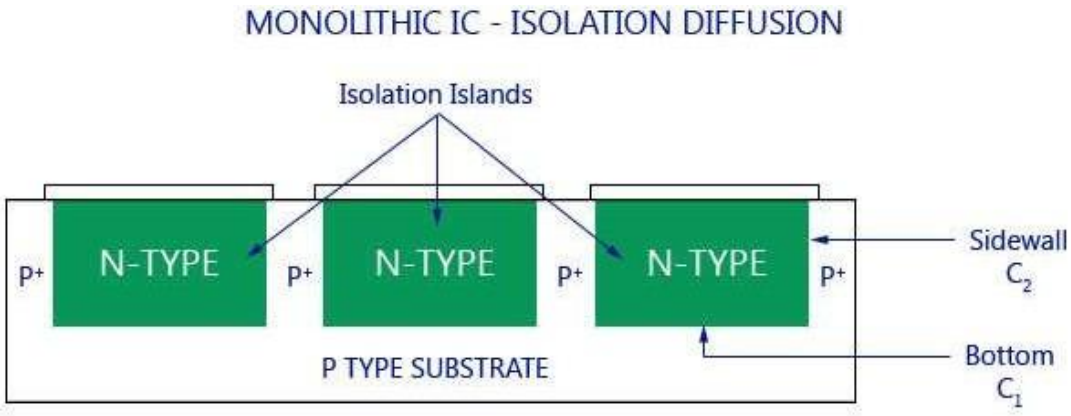
4. Photolithographic Process for SiO2

To diffuse the impurities with the N-type epitaxial region, the silicon dioxide layer has to be etched in selected areas. Thus openings must be brought at these areas through photolithographic process. In this process, the SiO2 layer is coated with a thin layer of a photosensitive material called photoresist. A large black and white pattern is made in the desired patter, where the black pattern represents the area of opening and white represents the area that is left idle. This pattern is reduced in size and fit to the layer, above the photoresist. The whole layer is then exposed to ultraviolet light. Due to the exposure, the photoresist right below the white pattern becomes polymerized. The pattern is then removed and the wafer is developed using a chemical like trichloroethylene. The chemical dissolves the unpolymerized portion of the photoresist film and leaves the surface. The oxide not covered by polymerised photoresist is then removed by immersing the chip in an etching solution of HCl. Those portions of the Si02 which are protected by the photoresist remain unaffected by the acid. After the etching and diffusion process, with the help of chemical solvents like sulphuric acid, the resist mask is then removed by mechanical abrasion. The appropriate impurities are then diffused through oxide free windows.



5. Isolation Diffusion

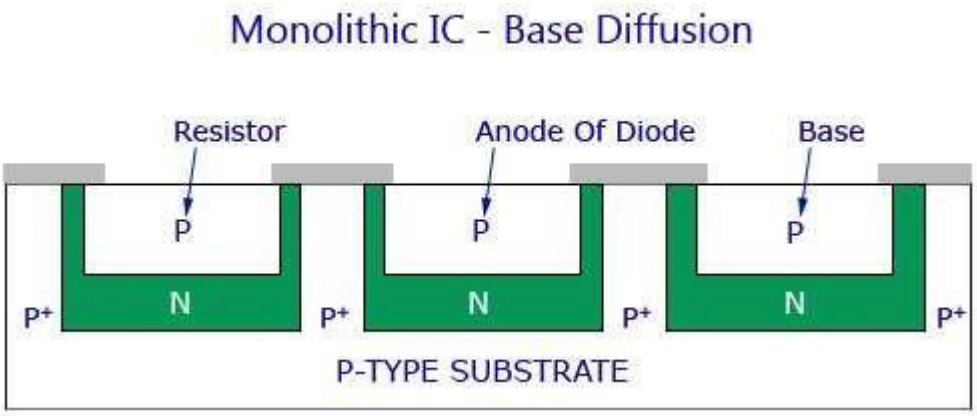
After photolithographic process the remaining SiO2 layer serves as a mask for the diffusion of acceptor impurities. To get a proper time period for allowing a P-type impurity to penetrate into the N-type epitaxial layer, isolation diffusion is to be carried out. By this process, the P-type impurity will travel through the openings in SiO2 layer, and the N-type layer and thus reach the P-type substrate, Isolation junctions are used to isolate between various components of the IC. The temperature and time period of isolation diffusion should be carefully monitored and controlled. As a result of isolation diffusion, the formation of N-type region called Isolation Island occurs. Each isolated island is then chosen to grow each electrical component. From the figure below you can see that the isolation islands look like back-to-back P-N junctions. The main use if this is to allow electrical isolation between the different components inside the IC. Each electrical element is later on formed in a separate isolation island. The bottom of the N-type isolation island ultimately forms the collector of an N-P-N transistor. The P-type substrate is always kept negative with respect to the isolation islands and provided with reverse bias at P-N junctions. The isolation will disappear if the P-N junctions are forward biased.



An effect of capacitance is produced in the region where the two adjoining isolation islands are connected to the P-type substrate. This is basically a parasitic capacitance that will affect the performance of the IC. This kind of capacitance is divided into two. As shown in the figure C1 is one kind of capacitance that forms from the bottom of the N-type region to the substrate and capacitance C2 from the sidewalls of the isolation islands to the P-region. The bottom component C1 is essentially due to step junction formed by epitaxial growth and, therefore, varies as the square root of the voltage V between the isolation region and substrate. The sidewall capacitance C2 is associated with a diffused graded junction and so varies as (-1/2) exponential of V. The total capacitance is of the order of a few picoFarads.

6. Base Diffusion

The working of base diffusion process is shown in the figure below. This process is done to create a new layer of SiO2 over the wafer. P-regions are formed under regulated environments by diffusing P-type impurities like boron. This forms the base region of an N-P-N transistor or as well as resistors, the anode of diode, and junction capacitor. In this case, the diffusion time is so controlled that the P-type impurities do not reach the substrate. The resistivity of the base layer is usually much higher than that of the isolation regions.

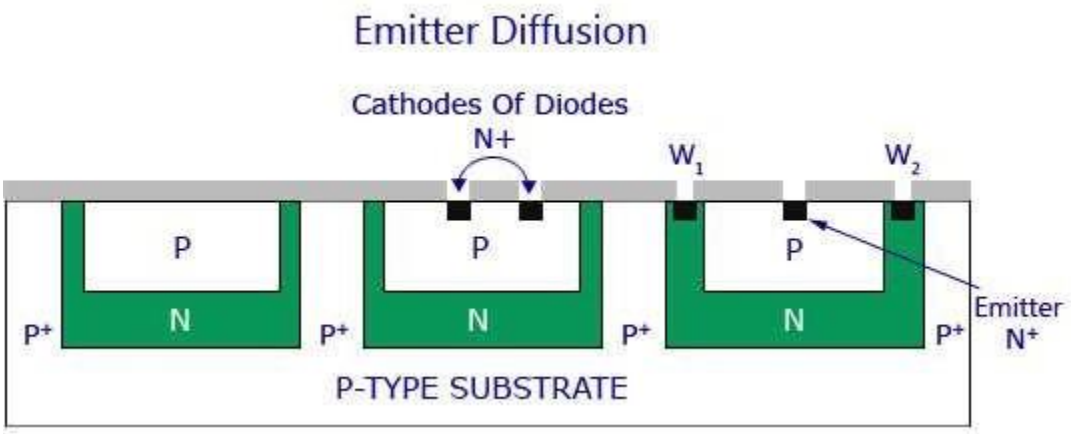


The isolation regions will have a lot lesser resistivity than that of the base layer.

7. Emitter Diffusion

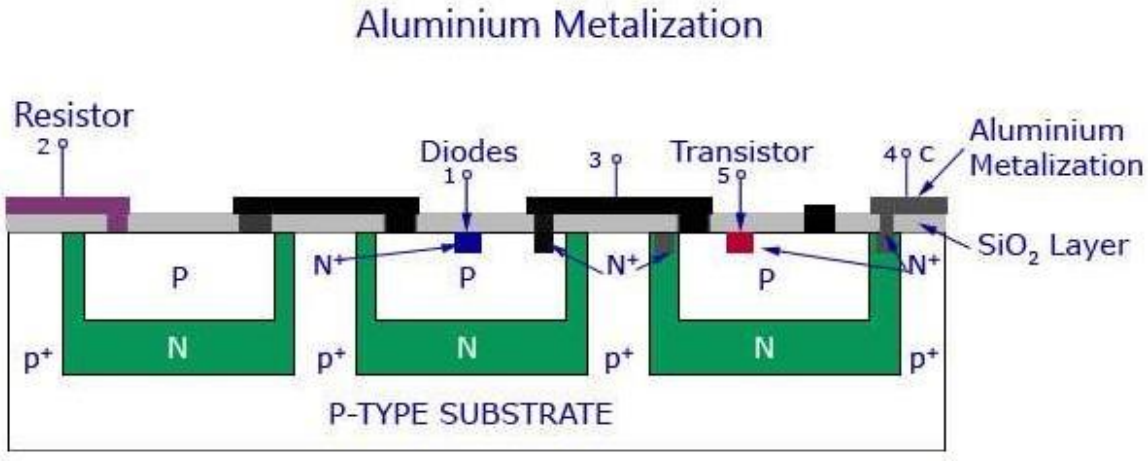
Masking and etching process is again carried out to form a layer of silicon dioxide over the entire surface and opening of the P-type region. The transistor emitters, the cathode regions for diodes, and junction capacitors are grown by diffusion using N-type impurities like phosphorus through the windows created through the process under controlled environmental process. As

shown in the figure below there are two additional windows: W1 and W2. These windows are made in the N-region to carry an aluminium metallization process.



8. Aluminium Metallization

The windows made in the N-region after creating a silicon dioxide layer are then deposited with aluminium on the top surface. The same photoresist technique that was used in photolithographic process is also used here to etch away the unwanted aluminium areas. The structure then provides the connected strips to which the leads are attached. The process can be better understood by going through the figure below.



9. Scribing and Mounting

This is the final stage of the IC manufacturing process. After the metallization process, the silicon wafer is then scribed with a diamond tipped tool and separated into individual chips. Each chip is then mounted on a ceramic wafer and is attached to a suitable header. Next the

package leads are connected to the IC chip by bonding of aluminium or gold wire from the terminal pad on the IC chip to the package lead. Thus the manufacturing process is complete. Thu, hundreds of IC's is manufactured simultaneously on a single silicon wafer.

7. What is thick and thin Technology? Explain various methods used for deposition of thin film technology. (Sep 2020)

Conventional film circuits, both thick and thin, are made by depositing film capacitors and resistors on a passive substrate such as glass or ceramic and subsequently adding pre-fabricated active components to the film structure. Care has to be taken that the film elements and their interconnections are compatible with the rest of the integrated circuit.

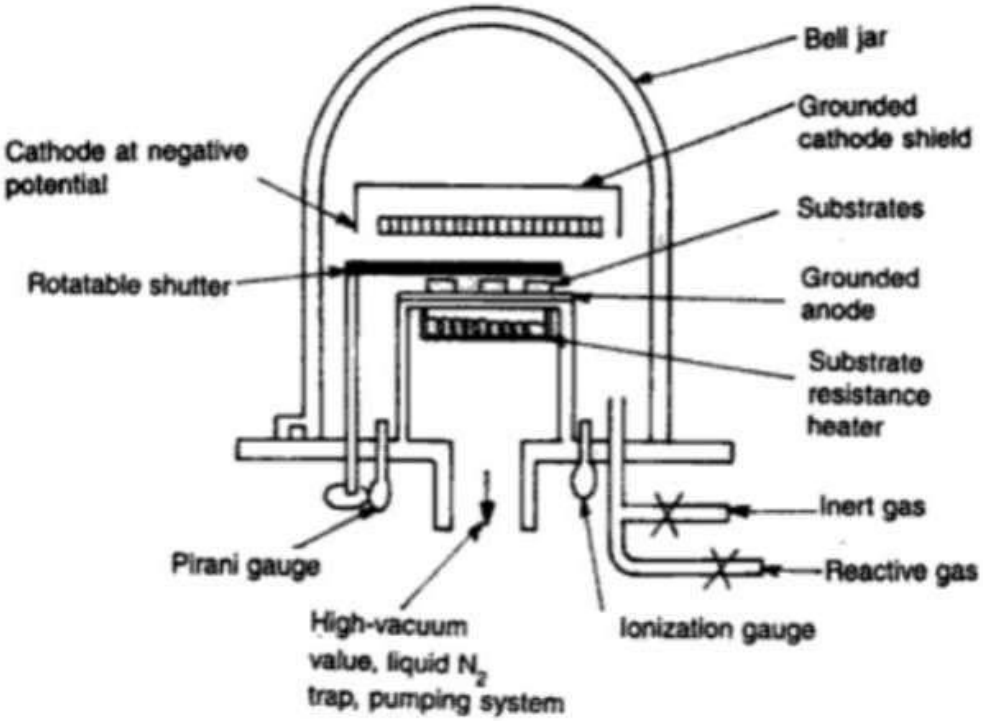
Combining films and semiconductor technology, a circuit designer has greater degree of freedom, a wider range of component values and better electrical performance than either technology can provide separately.

Thin flim and thick flim technology

Various methods in use for deposition of thin film are:

1. Vacuum Evaporation
2. Sputtering
3. Gas plating
4. Electroplating
5. Electroless plating
6. Silk screening

The methods listed above have been used with varying degree of success. In this text however, we limit ourselves to discuss cathode sputtering and plating techniques only.


Bell jar
Grounded cathode shield
Cathode at negative potential
Substrates
Rotatable shutter
Grounded anode
Substrate resistance heater
Inert gas
Reactive gas
Pirani gauge
High-vacuum value, liquid N_2 trap, pumping system
Ionization gauge

BM T45 – LINEAR INTEGRATED CIRCUITS

UNIT- 2

PART-A

1. Define the functions/operations of sample and hold circuit. (May 2014, May 2018)

- The function of the Sample & Hold Circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.
- The sampling period may be from 1 to 10 μS.
- The holding period may be from a few milliseconds to several seconds.

2. What are the applications of integrator and differentiator? (May 2014)

- Differentiators are used as wave shaping circuits, to detect high frequency components in the input signal.
- The integrator circuit is mostly used in analog computers, analog-to-digital converters and wave-shaping circuits.

3. What is summing amplifier? (Nov 2014)

- The summing Amplifier is one variation of inverting amplifier.
- Summing amplifier is basically an op amp circuit that can combine numbers of input signal to a single output that is the weighted sum of the applied inputs.

4. What is slew rate? (Nov 2014)

- The slew rate is defined as the maximum rate of change of output Voltage caused by a step input voltage.
- An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage.

5. How does the precision rectifier differs from the conventional rectifier? (Nov 2015)

- Precision rectifiers use op amp based circuits whereas conventional rectifiers use simple diodes.
- Precision rectifier is a close approximation of an ideal diode because of absence of forward voltage drop.

6. State the important features of an instrumentation amplifier. (Nov 2015, Nov 2016, Nov 2017)

- High common mode rejection ratio (CMRR)

- High open loop gain
- Low DC offset
- Low drift
- Low input impedance
- Low noise.

7. Define Hysteresis and Hysteresis voltage of Schmitt trigger. (Nov 2016)

- Hysteresis can be defined as when the input is higher than a certain chosen threshold, the output is low.
- When the input is below a threshold, the output is high; when the input is between the two, the output retains its current value.
- This dual threshold action is called hysteresis.

8. What is the value of open loop gain and output impedance of an ideal Op-amp. (May 2017)

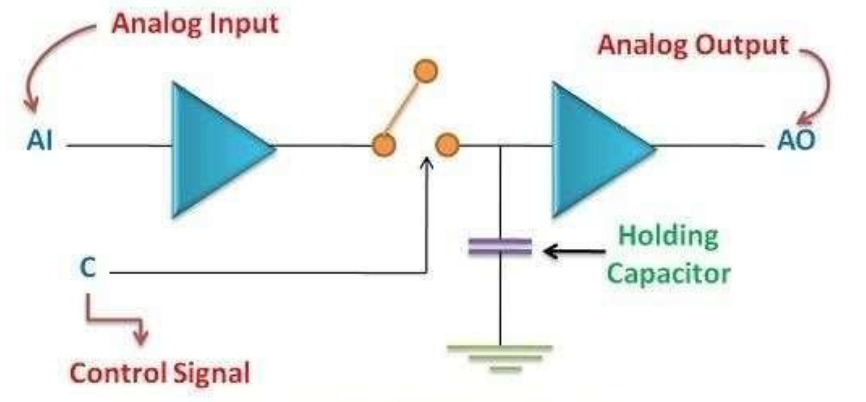
- The output gain will be infinite.
- The output impedance of an ideal op amp is 0.

9. Define CMRR. (May 2017)

- It is defined as the ratio of the differential voltage gain to common mode voltage gain.
- It is expressed in decibels.

CMRR= A_d / A_c

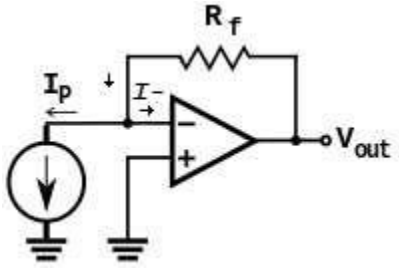
10. Draw the practical sample and hold circuit configuration. (Nov 2017, Nov 2018, May 2019)



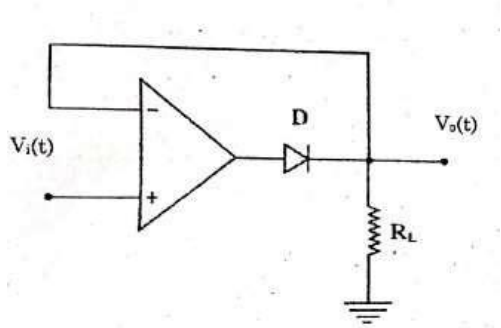
Circuit diagram of Sample and Hold Circuit

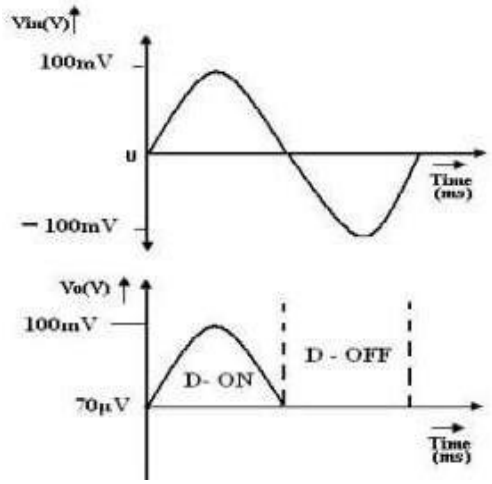
Electronics Coach

11. Draw the circuit of I to V converter using Op- amp. (May 2018)



12. Sketch the output waveform V_0 (t) for the following circuit, if the input voltage is $V_i(t)=2\sin(2000\pi t)$. (Nov 2018)





13. How do a Schmitt trigger acts as a regenerative comparator? (May 2019, Sep 2020)

- A Schmitt trigger circuit is also called a regenerative comparator circuit.
- It is basically an inverting comparator circuit with a positive feedback.
- The purpose of the Schmitt trigger is to convert any regular or irregular shaped input waveform into a square wave output voltage or pulse.

14. Name four applications of comparator. (Sep 2020)

- Zero crossing detector

- Window detector
- Time marker generator
- Phase detector

PART-B

1. What is an instrumentation amplifier? Draw a system whose gain is controlled by an adjustable resistance (May 2014, Nov 2015, May 2018, Nov 2018, Sep 2020)

Instrumentation amplifier

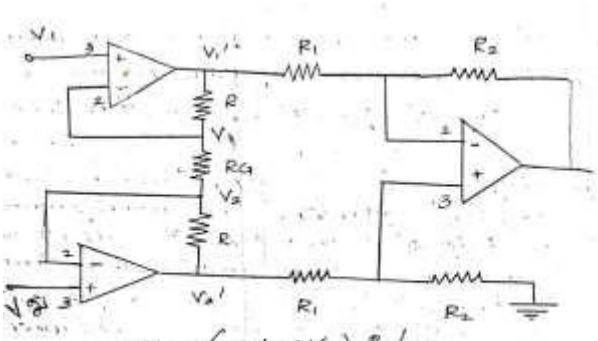
In a number of individual and consumers Application, one is required to measure and control physical quantities. Some typical example are Measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measure with the help of transducers. The output of the transducers has to be amplified so that it can derive the indicator or display system. This function is performed by an instrumentation amplifier. It is also called data amplifiers.

Characteristics

- High gain accuracy
- High CMRR
- Low dc offset
- Low output impedance
- High gain stability with low temperature coefficient.

Applications

- Temperature indicator
- Temperature controller
- Light intensity meter
- Water flow meter
- Thermal conductivity



$$V_o = (V_2' - V_1')\, R_2/R_1$$

Applying nodal analysis,

$$\frac{V_1 - V_1'}{R} + \frac{V_1 - V_2}{R_G} = 0 \quad -(1)$$

$$\frac{V_2 - V_2'}{R} + \frac{V_2 - V_1}{R_G} = 0 \quad -(2)$$

$(1) = (2)$

$$\frac{V_1 - V_1'}{R} + \frac{V_1 - V_2}{R_G} = \frac{V_2 - V_2'}{R} + \frac{V_2 - V_1}{R_G}$$

$$\frac{V_1}{R} - \frac{V_1'}{R} + \frac{V_1}{R_G} - \frac{V_2}{R_G} = \frac{V_2}{R} - \frac{V_2'}{R} + \frac{V_2}{R_G} - \frac{V_1}{R_G} \quad (3)$$

$$V_1 - V_2(1/R) + (V_2' - V_1')(1/R) + 1/R_G\,(V_1 - V_2 - V_2 + V_1) = 0$$

$$\frac{1}{R}(V_1 - V_2) + \frac{1}{R}(V_2' - V_1') + \frac{2}{R_G}(V_1 - V_2)$$

$$\left(\frac{1}{R} + \frac{2}{R_G}\right)(V_1 - V_2) + \frac{1}{R}(V_2' - V_1') = 0$$

$$\left(\frac{1}{R} + \frac{2}{R_G}\right)(V_1 - V_2) = -\frac{1}{R}(V_2' - V_1')$$

$$\left(\frac{1}{R} + \frac{2}{R_G}\right)(V_2 - V_1) = 1/R\,(V_2' - V_1')$$

$$R\left(1/R + \frac{2}{R_G}\right)(V_2 - V_1) = (V_2' - V_1')$$

Sub $V_o = (V_2' - V_1')\, R_2/R_1$

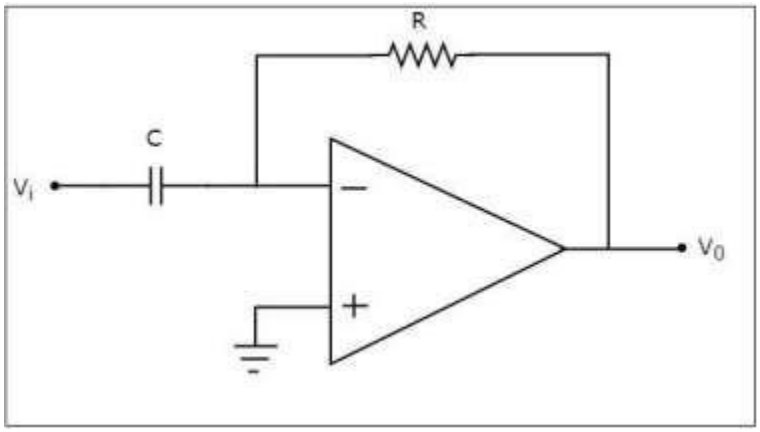
$$(V_2' - V_1') = \frac{V_o R_1}{R_2}$$

$$\frac{V_o R_1}{R_2} = \left(1 + \frac{2R}{R_G}\right)(V_2 - V_1)$$

$$V_o = \left(1 + \frac{2R}{R_G}\right) \frac{R_2}{R_1} (V_2 - V_1)$$

1st stage buffer; 2nd stage buffer; differential amplifier

2. a) Explain the operation of differentiator. (May 2014, Nov 2016, Nov 2018)



The input signal to the differentiator is applied to the capacitor. The capacitor blocks any DC content so there is no current flow to the amplifier summing point, X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is "High" resulting in a low gain (R_f/Xc) and low output voltage from the op-amp. At higher frequencies the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate. This is due mainly to the first-order effect, which determines the frequency response of the op-amp circuit causing a second-order response which, at high frequencies gives an output voltage far higher than what would be expected. To avoid this the high frequency gain of the circuit needs to be reduced by adding an additional small value capacitor across the feedback resistor R_f.

Since the node voltage of the operational amplifier at its inverting input terminal is zero, the current, i flowing through the capacitor will be given as:

$$I_{IN} = I_F \quad \text{and} \quad I_F = -\frac{V_{OUT}}{R_F}$$

The charge on the capacitor equals Capacitance times Voltage across the capacitor

$$Q = C \times V_{IN}$$

Thus the rate of change of this charge is:

$$\frac{dQ}{dt} = C\frac{dV_{IN}}{dt}$$

but dQ/dt is the capacitor current, *i*

$$I_{IN} = C\frac{dV_{IN}}{dt} = I_F$$

$$\therefore -\frac{V_{OUT}}{R_F} = C\frac{dV_{IN}}{dt}$$

from which we have an ideal voltage output for the op-amp differentiator is given as:

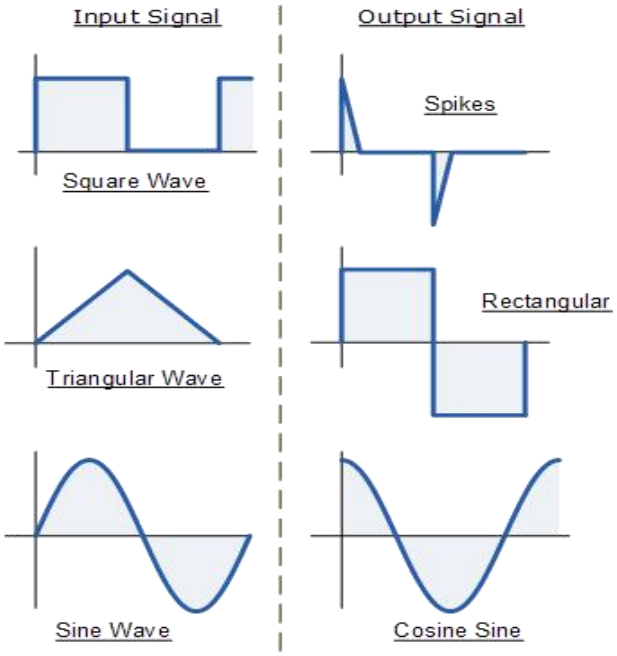
$$V_{OUT} = -R_F C\frac{dV_{IN}}{dt}$$

Therefore, the output voltage V_{out} is a constant $-Rf*C$ times the derivative of the input voltage V_{in} with respect to time. The minus sign (–) indicates a 180° phase shift because the input signal is connected to the inverting input terminal of the operational amplifier.

The Op-amp Differentiator circuit in its basic form has two main disadvantages compared to the previous operational amplifier integrator circuit. One is that it suffers from instability at high frequencies as mentioned above, and the other is that the capacitive input makes it very susceptible to random noise signals and any noise or harmonics present in the source circuit will be amplified more than the input signal itself. This is because the output is proportional to the slope of the input voltage so some means of limiting the bandwidth in order to achieve closed-loop stability is required.

Op-amp Differentiator Waveforms

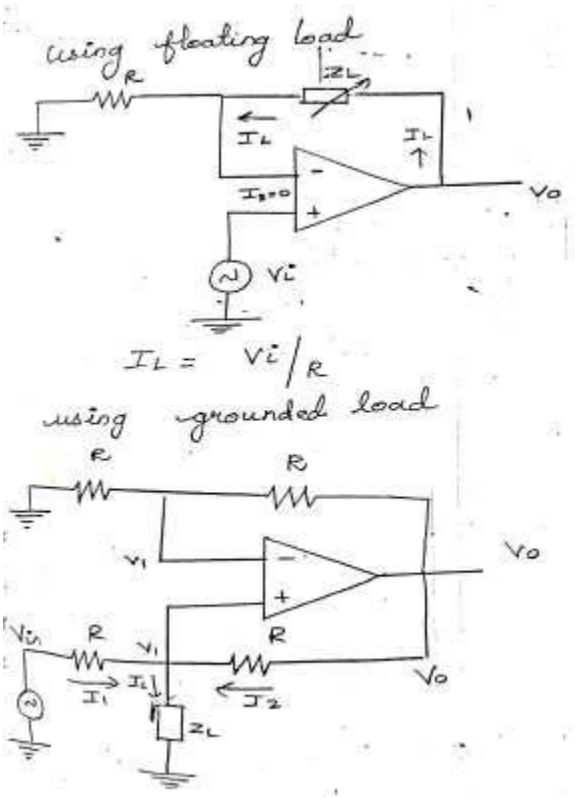
If we apply a constantly changing signal such as a Square-wave, Triangular or Sine-wave type signal to the input of a differentiator amplifier circuit the resultant output signal will be changed and whose final shape is dependent upon the RC time constant of the Resistor/Capacitor combination.



2. Brief about V-I converter. (Nov 2014, Nov 2016, May 2017, May 2019)

V to I converter

The voltage to current converter presented as a special case of the inverting amplifier in which an input voltage is converted into a proportional output current. It is also called transconductance amplifier.



Applying KCL,

$$I_1 + I_2 = I_L$$

$$\frac{V_{in} - V_1}{R} + \frac{V_o - V_i}{R} = I_L$$

$$\frac{V_{in} + V_o - 2V_1}{R} = I_L$$

$$V_{in} + V_o - 2V_1 = I_L R$$

$$-2V_1 = I_L R - V_{in} - V_o$$

$$V_1 = \frac{V_{in} + V_o - I_L R}{2}$$

$$\frac{V_1 - V_o}{R} + \frac{V_1 - 0}{R} = 0$$

$$\frac{2V_1 - V_o}{R} = 0$$

$$2V_1 - V_o = 0$$

$$2V_1 = V_o$$

$$2\left(\frac{V_{in} + V_o - I_L R}{2}\right) = V_o$$

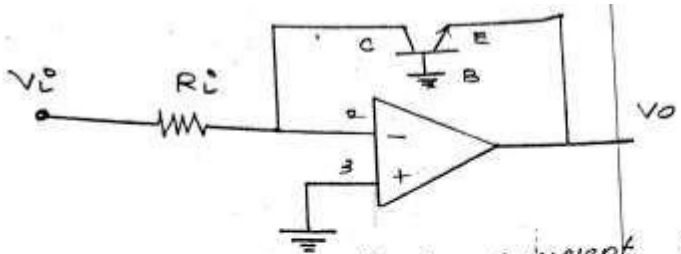
$$V_o = V_{in} + V_o - I_L R$$

$$V_o - V_o = V_{in} - I_L R$$

$$V_{in} = I_L R$$

$$I_L = V_{in}/R$$

4. Brief about Log amplifier. (Nov 2014, Nov 2017, Sep 2020, Nov 2018)



By using diode--current equation

$$I_E = I_S \left(e^{\frac{V_E}{\eta V_T}} - 1 \right)$$

$$\boxed{I_E = I_C}$$

$$I_C = I_S \left(e^{\frac{V_E}{\eta V_T}} - 1 \right)$$

$$\frac{I_C}{I_S} = e^{\frac{V_E}{\eta V_T}} - 1$$

$$\frac{I_C}{I_S} + 1 = e^{\frac{V_E}{\eta V_T}}$$

$$\boxed{V_E = -V_o}$$

$$\frac{-V_o}{\eta V_T} = \ln\left(\frac{I_C}{I_S}\right) \qquad I_C = \frac{V_i}{R_i}$$

$$\frac{-V_o}{\eta V_T} = \ln\left(\frac{V_i/R_i}{I_S}\right)$$

$$\frac{-V_o}{\eta V_T} = \ln\left(\frac{V_i}{R_i I_S}\right)$$

$$\boxed{R_i I_S = V_{ref}}$$

The output voltage is a function of logarithm of the input voltage

$$-V_o = \eta V_T \ln\left(\frac{V_i}{V_{ref}}\right)$$

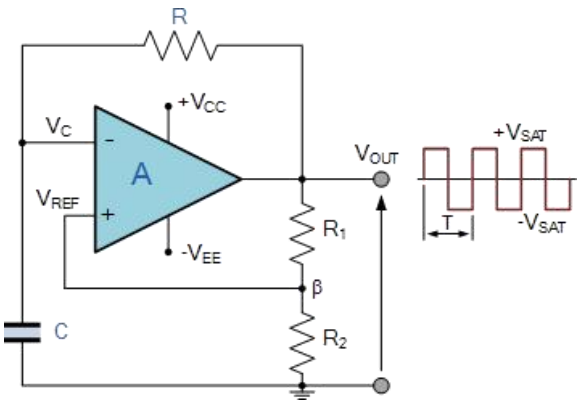
$$V_o = -\eta V_T \cdot 2.303 \log\left(V_i/V_{ref}\right)$$

5. Explain the working of multivibrator using operational amplifiers in detail. (Nov 2014, May 2019)

Op-amp Multivibrator

The idea of converting a periodic waveform into a rectangular output one step further by replacing the sinusoidal input with an RC timing circuit connected across the op-amps output. This time, instead of a sinusoidal waveform being used to trigger the op-amp, we can use the capacitors charging voltage, Vc to change the output state of the op-amp as shown.

Op-amp Multivibrator Circuit



Lets assume that the capacitor is fully discharged and the output of the op-amp is saturated at the positive supply rail. The capacitor, C starts to charge up from the output voltage, Vout through resistor, R at a rate determined by their RC time constant.

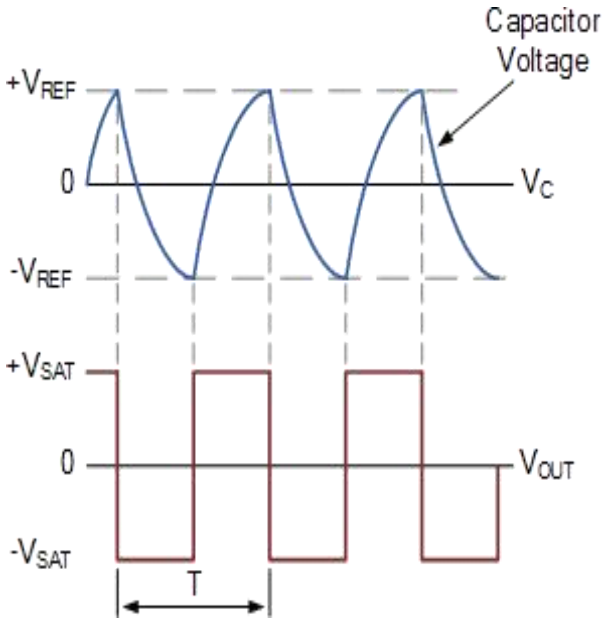
We know from our tutorials about RC circuits that the capacitor wants to charge up fully to the value of Vout (which is +V(sat)) within five time constants. However, as soon as the capacitors charging voltage at the op-amps inverting (-) terminal is equal to or greater than the voltage at the non-inverting terminal (the op-amps output voltage fraction divided between resistors R1 and R2), the output will change state and be driven to the oppos ing negative supply rail.

But the capacitor, which has been happily charging towards the positive supply rail (+V(sat)), now sees a negative voltage, -V(sat) across its plates. This sudden reversal of the output voltage causes the capacitor to discharge toward the new value of Vout at a rate dictated again by their RC time constant.

Op-amp Multivibrator Voltages

Once the op-amps inverting terminal reaches the new negative reference voltage, -Vref at the non-inverting terminal, the op-amp once again changes state and the output is driven to the opposing supply rail voltage, +V(sat). The capacitor now see's a positive voltage across its

plates and the charging cycle begins again. Thus, the capacitor is constantly charging and discharging creating an astable op-amp multivibrator output.



The period of the output waveform is determined by the RC time constant of the two timing components and the feedback ratio established by the R1, R2 voltage divider network which sets the reference voltage level. If the positive and negative values of the amplifiers saturation voltage have the same magnitude, then t1 = t2 and the expression to give the period of oscillation becomes:

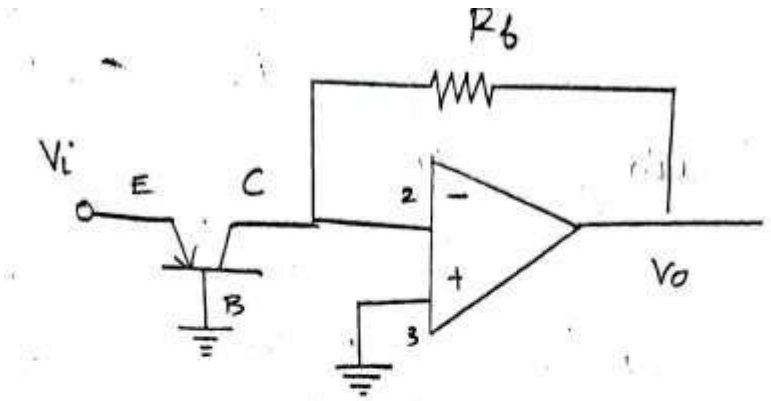
$$\beta = \frac{R_2}{R_1 + R_2}$$

$$T = 2RC \times \ln\left(\frac{1+\beta}{1-\beta}\right) \qquad \therefore f = \frac{1}{T}$$

Where: R is Resistance, C is Capacitance, ln( ) is the Natural Logarithm of the feedback fraction, T is periodic time in seconds, and *f* is oscillation Frequency in Hz.

Then we can see from the above equation that the frequency of oscillation for an **Op-amp Multivibrator** circuit not only depends upon the RC time constant but also upon the feedback fraction. However, if we used resistor values that gave a feedback fraction of **0.462**, (**β = 0.462**), then the frequency of oscillation of the circuit would be equal to just 1/2RC as shown because the linear log term becomes equal to one.

6. Write short notes on Antilog amplifier. (Nov 2015, Nov 2016, May 2017, Sep 2020)



$$I_C = I_S\left(e^{\frac{V_E}{\eta V_T}} - 1\right)$$

$$\frac{I_C}{I_S} + 1 = e^{\frac{V_E}{\eta V_T}} \qquad I_f = -\frac{V_o}{R_f}$$

$$\frac{I_f}{I_S} = e^{\frac{V_i}{\eta V_T}} \qquad V_i = V_E$$

$$I_C = I_f$$

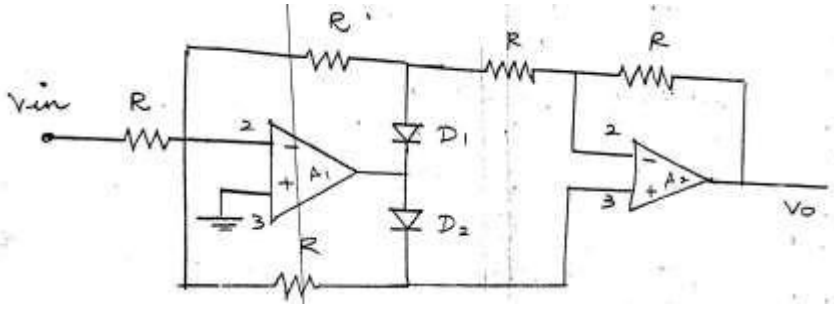
$$\frac{-V_o}{R_f I_S} = e^{\frac{V_i}{\eta V_T}}$$

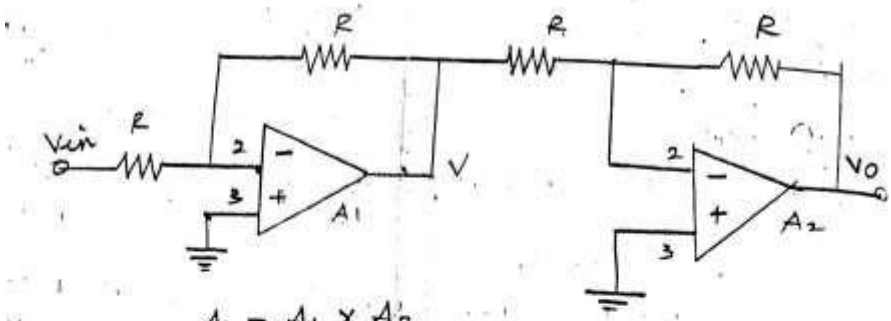
$$\ln\left(\frac{-V_o}{R_f I_S}\right) = \frac{V_i}{\eta V_T}$$

$$\ln \ln^{-1}\left(\frac{-V_o}{R_f I_S}\right) = \ln^{-1}\left(\frac{V_i}{\eta V_T}\right)$$

$$V_o = -R_f I_S \ln^{-1}\left(\frac{V_i}{\eta V_T}\right)$$

7. Write short notes on Precision rectifier. (Nov 2015)





$$A = A_1 \times A_2$$

$$A_1 = \frac{V_o}{V_{in}} \qquad A_1 = \frac{V}{V_{in}} = -R/R = -1$$

$$V = -V_i$$

$$A_2 = \frac{V_o}{V} = -R/R = -1$$

$$A_1 \times A_2 = \frac{V}{V_{in}} \times \frac{V_o}{V}$$

$$A_1 \times A_2 = 1$$

$$= \frac{V_o}{V_i}$$

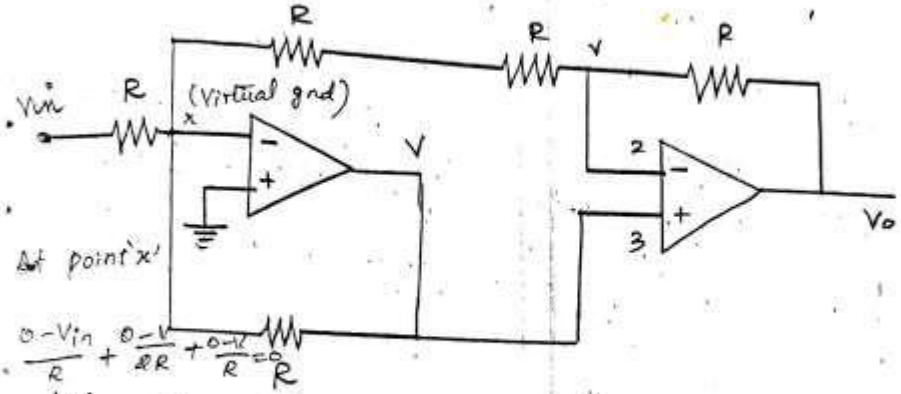
$$\frac{V_o}{V_i} = (-1)(-1)$$

$$\frac{V_o}{V_i} = 1$$

$$V_o = V_i$$

During negative half cycle, (12)

$V_i < 0$, Diode D_1 is off and D_2 is on.



$$\frac{V_i}{R} + \frac{V}{R} + \frac{V}{2R} = 0$$

$$\left(V_i + \frac{3V}{2}\right)\frac{1}{R} = 0$$

$$\frac{V_i}{R} + \frac{3V}{2R} = 0$$

$$V_i + \frac{3}{2}V = 0$$

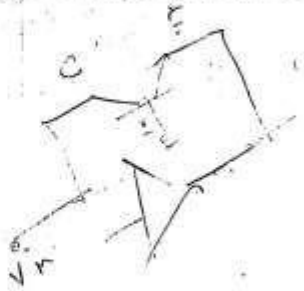
$$V = -\frac{2}{3}V_i$$

$$V = -2/3\,V_i$$

$$V_o = \left(1 + \frac{R}{2R}\right)V$$

$$V_o = \left(\frac{2R+R}{2R}\right)V$$

$$V_o = \left(\frac{3R}{2R}\right)V$$



$$V_o = 3/2\,V$$

$$V_o = 3/2\left(-2/3\right)V_i \Rightarrow V_o = -V_i$$

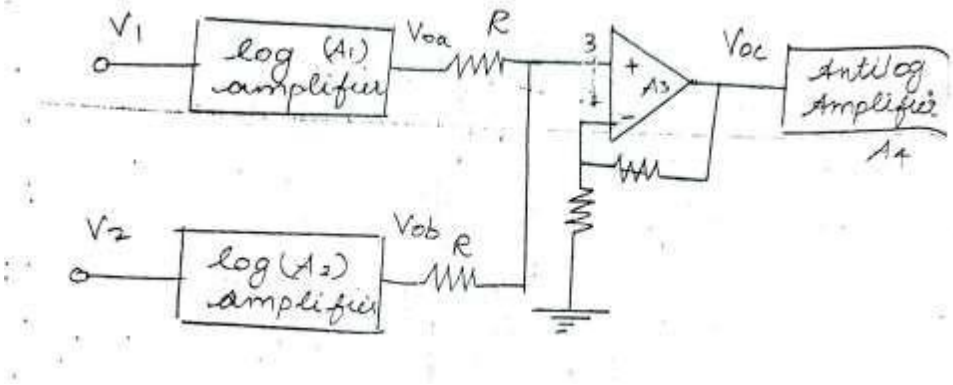
$$V_o = 3/2 \times \left(-2/3\right)V_i$$

$$V_o = -V_i$$

8. Draw the circuit and explain about an OP-AMP used as a Multiplier (Nov 2016)

Multiplier

Log and anti log amplifiers are used in this circuits. The output voltage is proportional to the product of the two input voltages. It is called analog voltage multipliers.



Applying Superposition theorem,

$V_{oa} \propto \ln V_1$

$V_{ob} \propto \ln V_2$

A_3 is an non inverting amplifier with unity gain

$V_{oc} \propto (V_{oa} + V_{ob})$

$V_{oc} \propto C \ln V_1 + \ln V_2$

$V_{oc} \propto (\ln V_1 + \ln V_2)$

V_{oc} is applied to input of antilog amplifier.

$V_o \propto \ln^{-1} (V_{oc})$

$V_o \propto \ln^{-1} (\ln V_1 V_2)$

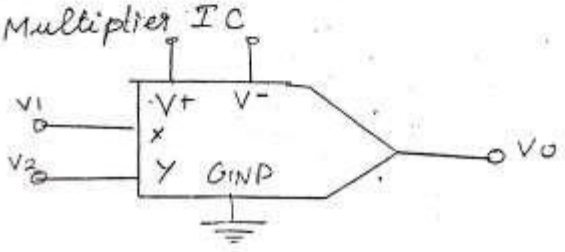
$V_o \propto V_1 V_2$

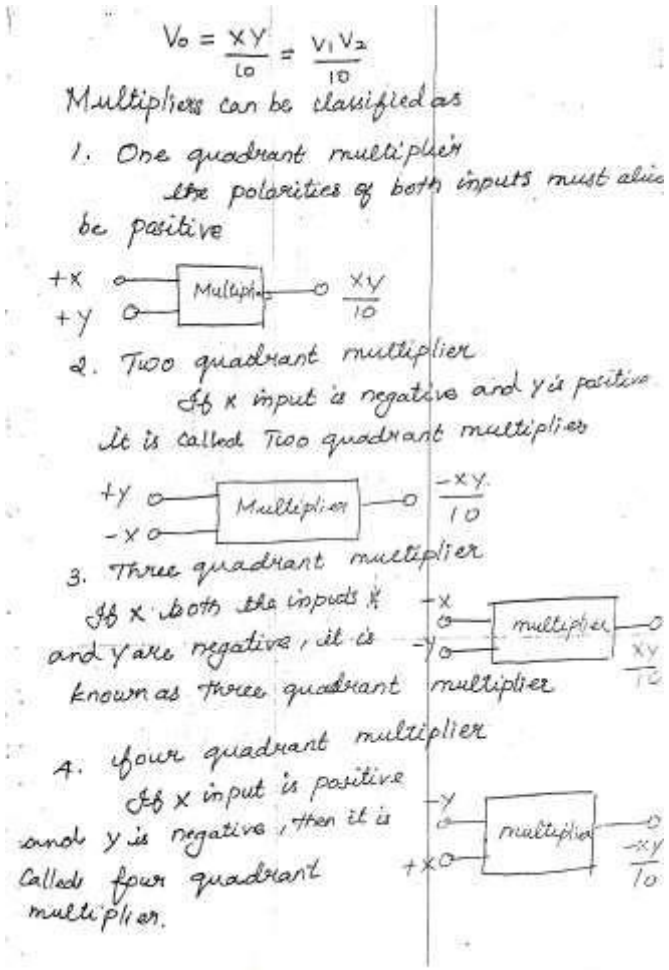
$V_o = k V_1 V_2$

$k = 1/\text{volt}$

Output is proportional to the product of two analog inputs V_1 and V_2.

Multiplier IC





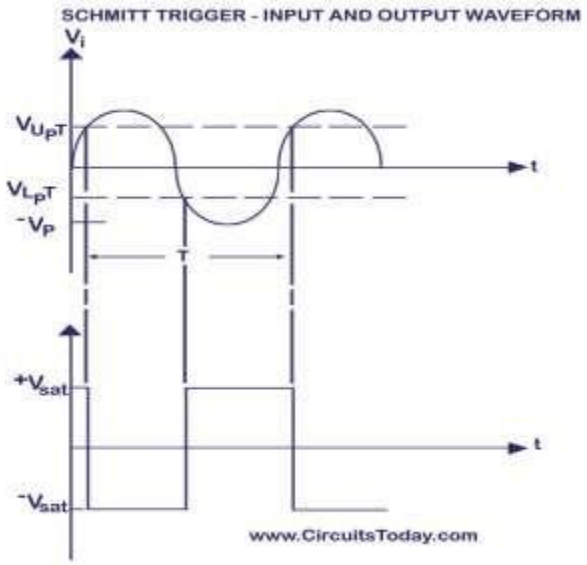
Applications

- Voltage divider
- Squaring circuit
- Square rooting circuit
- Frequency double
- Phase angle detection

9. Explain the working of Schmitt trigger using op amp in detail (May 2017, May 2018, Nov 2018)

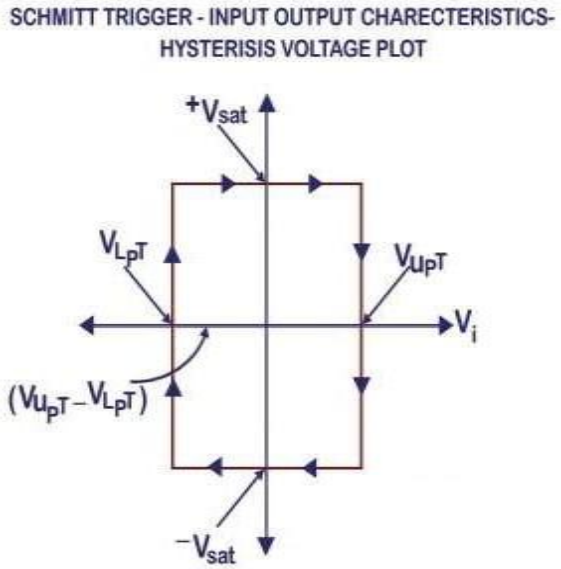
Schmitt trigger 741

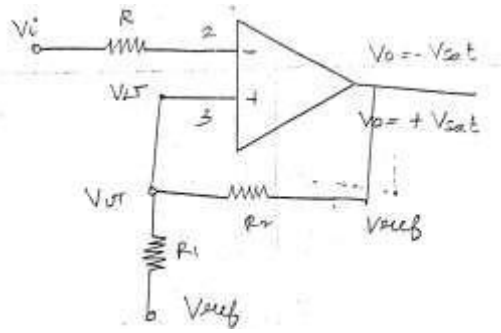
It converts sinusoidal input to square wave output. The output of Schmitt trigger swings between upper threshold voltage and lower threshold voltage and the reference voltage of the input waveform.



The difference in voltage between Vut and Vlt is called hysteresis voltage. The curve looking like hysteria curve of magnetic materials.

VH = Vut – Vlt





During positive cycle

$$\frac{V_{UT} - V_{ref}}{R_1} + \frac{V_{UT} - V_{sat}}{R_2} = 0$$

$$\frac{V_{UT}}{R_1} + \frac{V_{UT}}{R_2} + \left(- \frac{V_{ref}}{R_2} - \frac{V_{sat}}{R_2} \right) = 0$$

$$\frac{1}{R_1} + \frac{1}{R_2} (V_{UT}) = \frac{V_{ref}}{R_1} + \frac{V_{sat}}{R_2}$$

$$V_{UT} = \frac{R_2 V_{ref} + V_{sat} R_1}{R_1 R_2} \times \frac{R_2 R_1}{R_1 + R_2}$$

$$V_{UT} = \frac{R_2 V_{ref} + V_{sat} R_1}{R_1 + R_2}$$

During negative cycle

$$\frac{V_{LT} - V_{ref}}{R_1} + \frac{V_{LT} + V_{sat}}{R_2} = 0$$

$$V_{LT} \left(1/R_1 + 1/R_2 \right) = \frac{V_{ref}}{R_1} - \frac{V_{sat}}{R_2}$$

$$V_{LT} \left(1/R_1 + 1/R_2 \right) = \frac{R_2 V_{ref} - R_1 V_{sat}}{R_1 R_2}$$

$$V_{LT} = \frac{R_2 V_{ref} - R_1 V_{sat}}{R_1 R_2} \times \frac{R_1 R_2}{R_1 + R_2}$$

$$V_{LT} = \frac{R_2 V_{ref} - V_{sat} R_1}{R_1 + R_2}$$

$$V_H = V_{UT} - V_{LT}$$

$$V_H = \left[\frac{R_2 V_{ref} + V_{sat} R_1}{R_1 + R_2} \right] - \left[\frac{R_2 V_{ref} - V_{sat} R_1}{R_1 + R_2} \right]$$

$$= \frac{R_2 V_{ref} + V_{sat} R_1 - R_2 V_{ref} + V_{sat} R_1}{R_1 + R_2}$$

$$\boxed{V_H = \frac{2 V_{sat} R_1}{R_1 + R_2}}$$

10. Explain about comparator (Inverting and Non inverting comparator). (May 2017, Nov 2017)

Comparator

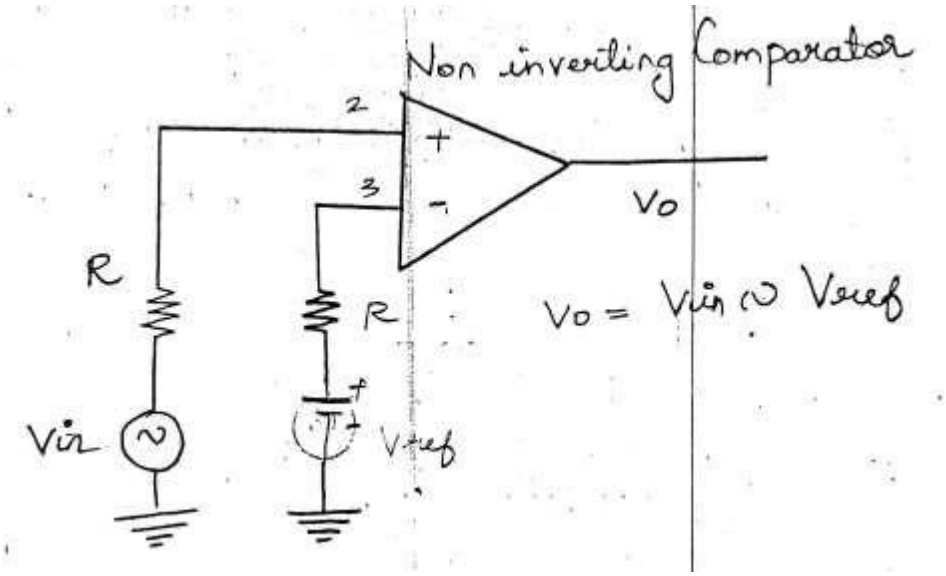
A comparator is a circuit which compares a signal voltage applied at input of an opamp with a known reference voltage at the other input. The comparator is a type of analog to digital converter. Vin is greater or less than Vref. The comparator is sometimes called a voltage level detector.

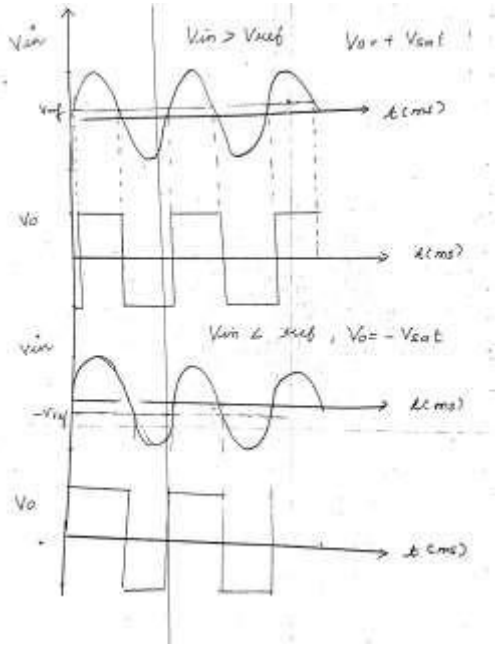
Comparator characteristics

- Response time
- Accuracy
- Logic threshold

Types

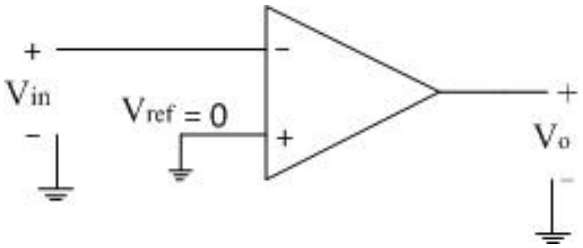
- Inverting comparator
- Non Inverting comparator



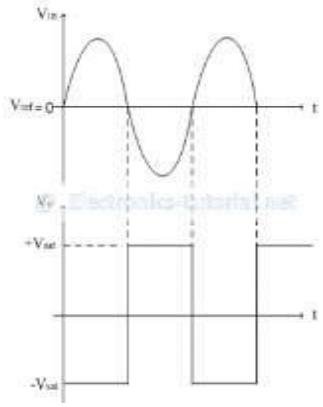


Inverting Comparator

The following figure shows the inverting configuration of comparator. The input signal is applied at inverting terminal of op-amp. The reference voltage Vref = 0V.



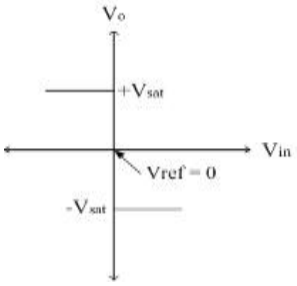
Due to open loop configuration of op-amp, the output goes into saturation.
The operation of the comparator is explained with the following two equations
1. If Vin> Vref then Vo= – Vsat
Thus for the positive half cycle of the input signal the above condition is true. So for the positive half cycle of input signal, the output goes into negative saturation i.e. –Vsat. The input and output waveforms are shown below.



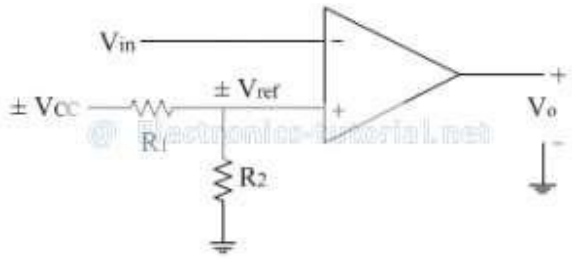
2. If Vin<Vref then Vo= +V_sat

Thus for the negative half cycle of the input signal the above condition is true. So for the negative half cycle of input signal, the output goes into positive saturation i.e. +Vsat.

The transfer characteristics are shown in figure below.



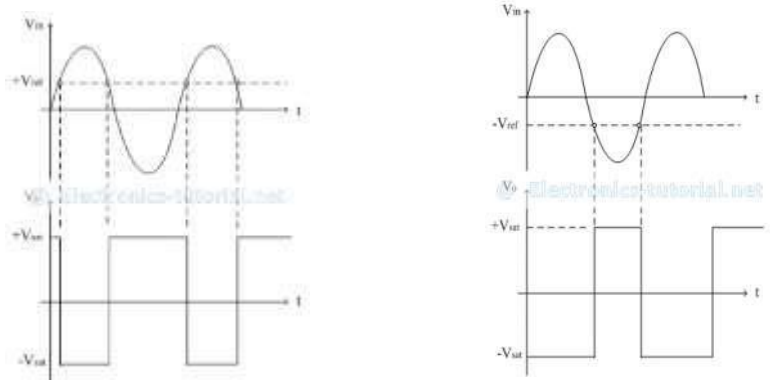
The reference voltage is zero here and hence the circuit is also called as inverting zero crossing detector. The reference voltage can be changed externally with the help of potential divider arrangement. This reference voltage can be either positive or negative as shown in circuit diagram below.



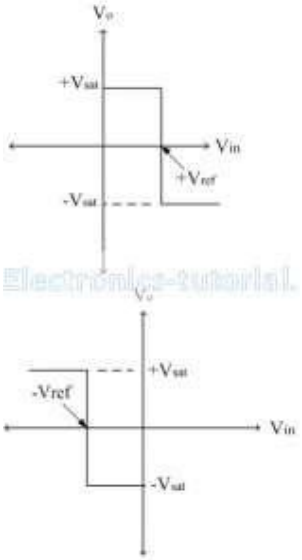
If the supply voltage is positive, the reference voltage is also positive. If the supply voltage is negative, the reference voltage is also negative.

$$\pm V_{ref} = \frac{R_2}{(R_1+R_2)}(\pm V_{CC})$$

The following figure shows the input and output waveforms for positive reference and negative reference.



The transfer characteristics of both positive as well as negative reference are shown below.



The transfer characteristics are basically a graph of output voltage versus input voltage. From the above characteristics, it is observed that the reference voltage (or reference point) is the point at which the state change occurs i.e. the transition from one state to other state. In other words, the circuit is triggered at the reference point hence it is also called as triggering point. The reference voltage can be changed externally and also can be either positive or negative as discussed above. Thus the reference point can have a trip on input axis anywhere, and hence it is also referred as trip point or trip voltage. Also at the reference point the state change occurs at the output when input signal crosses the reference voltage. Thus reference voltage is also called as threshold voltage at which the comparator is changing its output state.

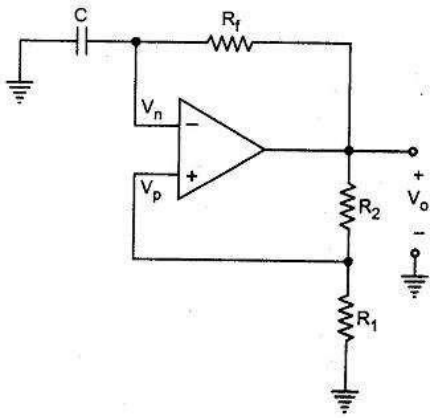
Application

- Zero crossing detector
- Window detector
- Time marker generator
- Phase meter

11. Write short notes on Square wave generator (May 2018)

Square Wave Generator Using Op amp:

The Square Wave Generator Using Op amp means the astable multivibrator circuit using op-amp, which generates the square wave of required frequency. The Fig shows the square wave generator using op amp.



It looks like a comparator with hysteresis (schmitt trigger), except that the input voltage is replaced by a capacitor. The circuit has a time dependent elements such as resistance and capacitor to set the frequency of oscillation.

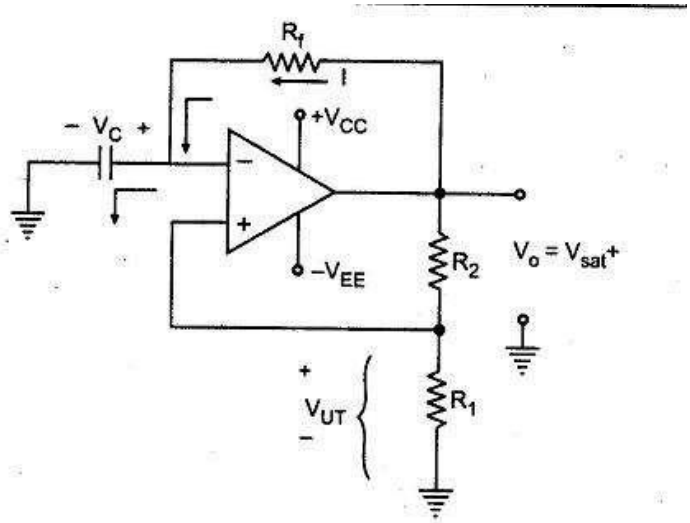
As shown in the Fig the comparator and positive feedback resistors R_1 and R_2 form an inverting schmitt trigger.

When V_o is at $+V_{sat}$, the feedback voltage is called the upper threshold voltage V_{UT} and is given as

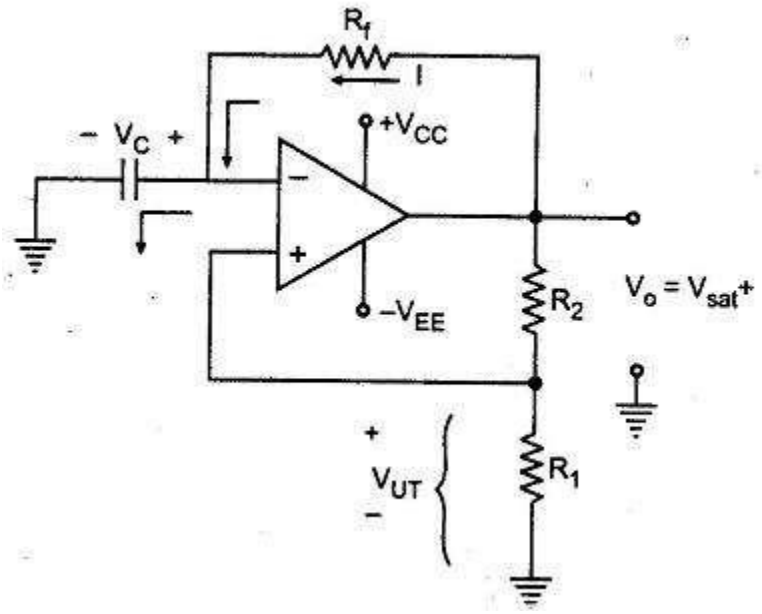
$$V_{UT} = \frac{R_1 \cdot +V_{sat}}{R_1 + R_2} \quad \ldots (1)$$

When V_o is at $-V_{sat}$, the feedback voltage is called the lower-threshold voltage V_{LT} and is given as

$$V_{LT} = \frac{R_1 \cdot -V_{sat}}{R_1 + R_2} \quad \ldots (2)$$

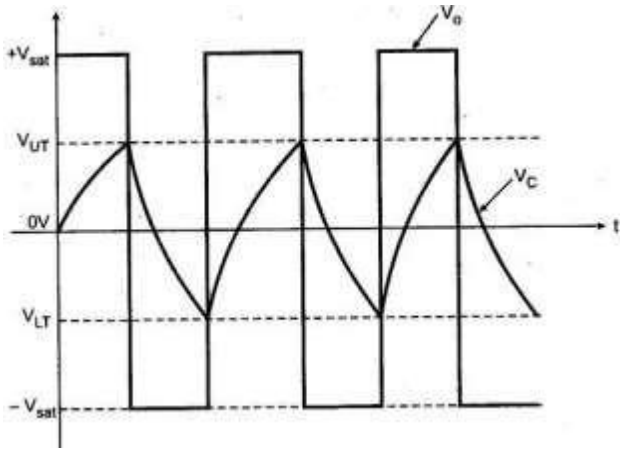


When power is turn ON, V_o automatically swings either to $+V_{sat}$ or to $-V_{sat}$ since these are the only stable states allowed by the schmitt trigger. Assume it swings to $+V_{sat}$. With $V_o = +V_{sat}$ we have $-V_p = V_{UT}$ and capacitor starts charging towards $+V_{sat}$ through the feedback path provided by the resistor R_f to the inverting (-) input. As long as the capacitor voltage V_C is less than V_{UT}, the output voltage remains at $+V_{sat}$.



As soon as V_C charges to a value slightly greater than V_{UT}, the (-) input goes positive with respect to the (+) input. This switches the output voltage from $+V_{sat}$ to $-V_{sat}$ and we have $V_p = V_{LT}$, which is negative with respect to ground. As V_o switches to $-V_{sat}$, capacitor starts discharging via R_f, as shown in the Fig.

The current I – discharges capacitor to 0 V and recharges capacitor to V_{LT}. When V_C becomes slightly more negative than the feedback voltage V_{LT}, output voltage V_o switches back to $+V_{sat}$. As a result, the condition in Fig. 2.84(a) is reestablished except that capacitor now has a initial charge equal to V_{LT}. The capacitor will discharge from V_{LT} to 0V and then recharge to V_{UT}, and the process is repeating. Once the, initial cycle is completed, the waveform become periodic, as shown in the Fig. 2.84(c).



Frequency of Oscillation:

The frequency of oscillation of Square Wave Generator Using Op amp is determined by the time it takes the capacitor to charge from V_{UT} to V_{LT} and vice versa. The voltage across the capacitor as a function of time is given as

$$V_C(t) = V_{max} + (V_{initial} - V_{max})\, e^{(-t/T)} \qquad \ldots (3)$$

where

$V_C(t)$ is the instantaneous voltage across the capacitor.

$V_{initial}$ is the initial voltage

V_{max} is the voltage toward which the capacitor is charging.

Let us consider the charging of capacitor from V_{LT} to V_{UT}, where V_{LT} is the initial voltage, V_{UT} is the instantaneous voltage and $+V_{sat}$ is the maximum voltage. At $t = T_1$, voltage across capacitor reaches V_{UT} and therefore equation (3) becomes

$$V_{UT} = +V_{sat} + (V_{LT} - +V_{sat})\, e^{(-T_1/R_f C)} \qquad \ldots (4)$$

$$\therefore -(V_{LT} - +V_{sat})\, e^{(-T_1/R_f C)} = +V_{sat} - V_{UT}$$

$$\therefore \quad e^{(-T_1/R_f C)} = \frac{(+V_{sat} - V_{UT})}{(+V_{sat} - V_{LT})}$$

$$\frac{-T_1}{R_f C} = ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$T_1 = -R_f C\, ln\left(\frac{+V_{sat} - V_{UT}}{+V_{sat} - V_{LT}}\right)$$

$$= R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \qquad \ldots (5)$$

The time taken by capacitor to charge from V_{UT} to V_{LT} is same as time required for charging capacitor from V_{LT} to V_{UT} . Therefore, total time required for one oscillation is given as

$$T = 2T_1 \qquad \ldots (6)$$

$$= 2R_f C\, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right) \qquad \ldots (7)$$

The frequency of oscillation can be determined as $f_o = 1/T$, where T represents the time required for one oscillation.

Substituting the value of T we get,

$$f_o = \frac{1}{2 R_f C \, ln\left(\frac{+V_{sat} - V_{LT}}{+V_{sat} - V_{UT}}\right)} \quad \ldots (8)$$

12. Write short notes about Peak detector. (May 2019)

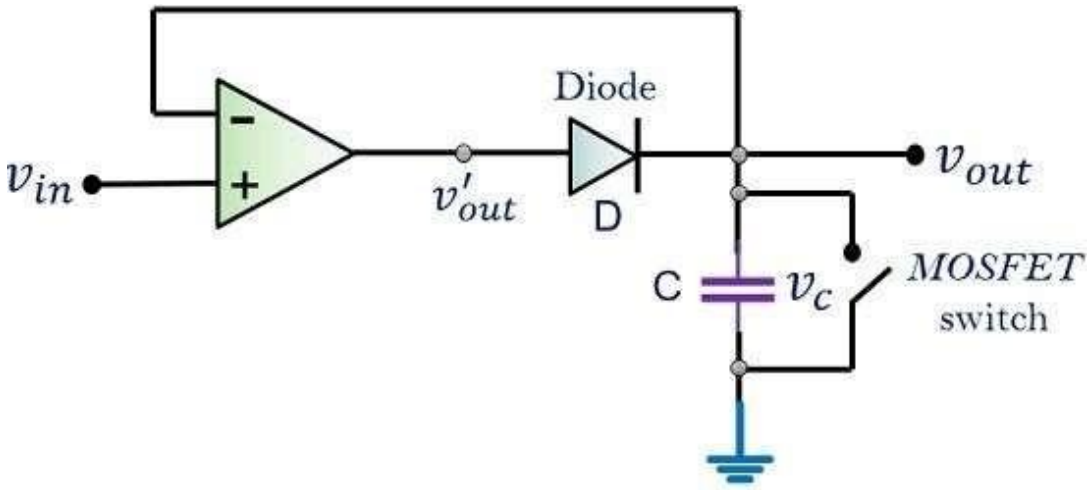
Peak detector circuits are used to determine the peak (maximum) value of an input signal. It stores the peak value of input voltages for infinite time duration until it comes to reset condition. The peak detector circuit utilizes its property of following the highest value of an input signal and storing it.

Rectifier circuits usually provide an output in proportion to the average value of the input. However, some application requires measurement of the peak value of the signal. Thus, peak detectors are used.

Usually, the peak of non-sinusoidal waveforms is measured using a peak detector. As traditional ac voltmeter cannot measure the peak of such signals.

Circuit Working of Peak detector

The figure below shows the circuit of a basic positive peak detector-



Peak detector circuit

Electronics Coach

It consists of a diode and capacitor along with an op-amp as shown above. The circuit does not require any complex component in order to determine the peak of the input waveform.

Working Principle

The working principle of the circuit is such that, the peak of the input waveform is followed and stored in terms of voltage in the capacitor.

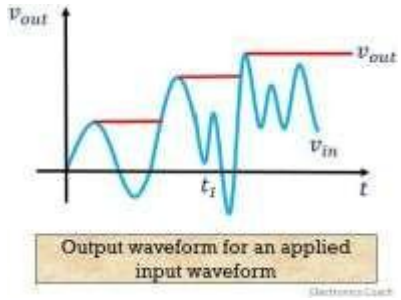
By the time on moving further, if the circuit detects a higher peak, the new peak value is stored in the capacitor until it is discharged.

The capacitor employed in the circuit is charged through the diode by the applied input signal. The small voltage drop across the diode is ignored and the capacitor is charged up to the highest peak of the applied input signal.

Let us consider initially the capacitor is charged to voltage V_c. The diode employed in the circuit gets forward biased when the applied input voltage V_{in} exceeds the capacitor voltage V_c. Thereby allowing the circuit to behave as a voltage follower. The output voltage follows the applied input voltage until V_{in} is more than V_c.

As the input voltage V_{in} reduces below the value of capacitive voltage V_c, it causes the diode to get reverse biased. In such condition, the capacitor retains the value until the input again exceeds the value stored in the capacitor.

The figure below shows the output voltage waveform for an applied input signal.



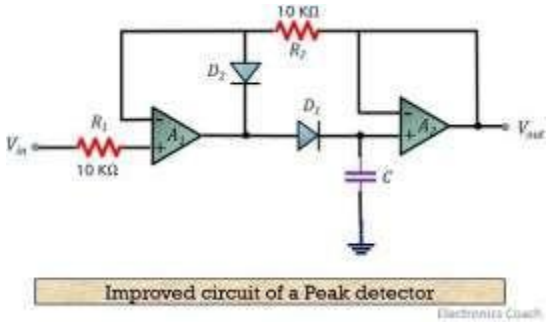
Output waveform for an applied input waveform

As we can see in the waveform shown above, at time t_1, the circuit misses the peak of the input signal as it is less than the previous peak of the input signal. Thereby allowing the capacitor to hold the value of the previously occurred peak.

As it is a positive peak detector, one can also construct a negative peak detector circuit, that will hold the lowest or most negative signal voltage. This is basically done by reversing the polarities of the diode in the circuit.

Improvement in peak detector circuit

The figure below shows the circuit of an improved peak detector. It is used to buffer the source of the signal from that of the capacitor.



Improved circuit of a Peak detector

As we can see the circuit is comprised of 2 Op-amps. However, the basic circuit of the peak detector contains only one Op-amp. A high impedance load is offered by the op-amp A_1 to the source. While op-amp A_2 performs buffering action in between the load and capacitor.

The same basic principle is applied in this circuit also. The voltage at the output side is the similar as the peak of the input signal stored in the capacitor.

Its working is such that, as the input voltage becomes higher than the charge stored on the capacitor, it charges itself with the new higher value of input signal.

However, for a smaller value of the input, the capacitor sticks to the previous higher value. The diode D_2 employed here restricts the output of op-amp A_1 from reaching negative saturation.

This basically provides an improvement in the recovery time of op-amp A_1 at the condition of attaining a higher peak than the previous. The two resistances serve as the path for the bias current of input to A_1.

To prevent the effect of the offset voltage, the value of the two resistances R_1 and R_2 are kept equal.

The necessary frequency compensation must be given to op-amp A_1 in order to have stability against oscillations.

Applications of Peak detector

1. It is used in the analysis of spectral and mass spectrometer.
2. Peak detector finds its application in destructive testing.
3. It is used for instrumentation measurement, mostly in amplitude modulated wave communication.
4. It widely finds applications in sound measuring instruments.

BM T45 – LINEAR INTEGRATED CIRCUITS

UNIT- 3

PART-A

1. (a) What are the limitations of three terminal regulator? (May 2014)

(b) Enumerate the limitations of three terminal voltage regulators. (Nov 2018)

- Limited power dissipation in available packages
- Limited current ranges
- Fixed voltage versions
- Dropout voltage

2. Discuss the advantages and disadvantages of SMPS. (May 2014)

Advantages

- The switch mode power supply has a smaller in size.
- The SMPS has light weight. SMPS has wide output range.
- Low heat generation in SMPS.
- SMPS has wide output range.
- Low heat generation in SMPS.

Disadvantages

- It can be used only as a step down regulator.
- It has only one output voltage.
- It has high frequency electrical noise.
- SMPS also cause harmonic distortion.

3. Give some applications of comparators. (Nov 2014)

- Zero crossing detector
- Window detector
- Time marker generator
- Phase detector

4. What is the function of voltage regulators? (Nov 2014, May 2017, Nov 2017)

- A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature, and ac line voltage variations.

5. State the important features of an instrumentation amplifier. Nov 2015)

- High common mode rejection ratio (CMRR)
- High open loop gain
- Low DC offset
- Low drift
- Low input impedance

- Low noise.

6. Define voltage to frequency conversion factor of VCO. (Nov 2015)

- Voltage to Frequency conversion factor is defined as,

Kv = fo / Vc= 8fo /Vcc

- Vc is the modulation voltage, fo-frequency shift

7. Define pass band of a filter. (Nov 2016)

- A band pass filter is an electronic circuit or device which allows only signals between specific frequencies to pass through and attenuates/rejects frequencies outside the range.
- Band pass filters are largely used in wireless receivers and transmitters.

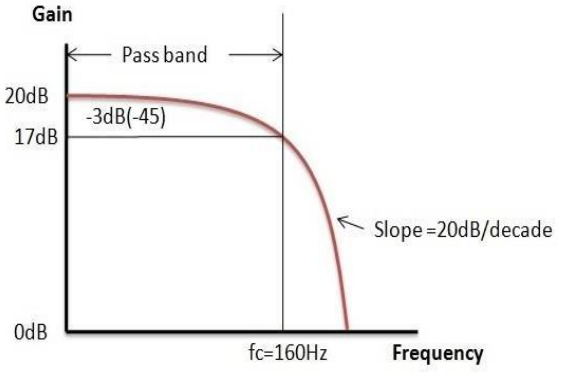
8. State the two conditions of oscillations. (Nov 2016)

- The total phase shift around the loop must be zero at the desired frequency of oscillation.
- The magnitude of the loop gain |Aβ | should be equal to unity.

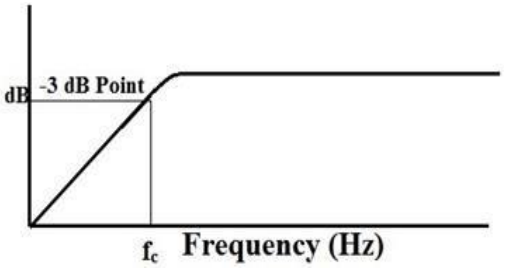
9. What is the principle of switch mode power supplies? (May 2017)

- SMPS circuit is operated by switching and hence the voltages vary continuously.
- The switching device is operated in saturation or cut off mode.
- The output voltage is controlled by the switching time of the feedback circuitry.
- Switching time is adjusted by adjusting the duty cycle.

10. Give the graphical representation of frequency response of LPF and HPF. (Nov 2017)



LPF



HPF

11. What are the applications of oscillator? (May 2018)

- Used in various audio systems and video systems
- Used in various radio, TV, and other communication devices
- Used in alarms and buzzes
- Used in metal detectors, stun guns, inverters, and ultrasonic

12. In what way VCO is different from other oscillators? (May 2018)

- A VCO is a Voltage Controlled Oscillators i.e. it is an electronic oscillator whose oscillating/output frequency can be controlled by a DC voltage.
- The oscillating/output frequency of the VCO can be modified by changing the DC voltage applied to it.

13. How do we get a notch filter from a band pass filter? (May 2019)

- A notch filter is a narrow band stop filter.
- If the stop band of Band stop filter is very narrow and highly attenuated over a few hertz, then that special type of band stop filter is known as Notch Filter.

14. Why VCO is called voltage to frequency converter? (May 2019, Sep 2020)

- The VCO provides the linear relationship between the applied voltage & the output frequency.
- So it is known as voltage to frequency converter.

15. How current boosting is achieved in a 723 regulator? (Sep 2020)

- The 723 voltage regulator is commonly used for series voltage regulator applications.
- It can be used as both positive and negative voltage regulator.
- It has an ability to provide up to 150 mA of current to the load, but this can be increased more than 10A by using power transistors.

PART-B

1. a) Explain the operation of SMPS in detail. (May 2014, Nov 2015)

b) With neat circuit diagrams and waveforms, explain the operation of SMPS. (Nov 2017, May 2018)

c) Explain about switching regulator. (Nov 2016)

d) Explain the working principle of switched mode power supply. Discuss its advantage and disadvantages. (Sep 2020)

Switched Mode Power Supply (SMPS)

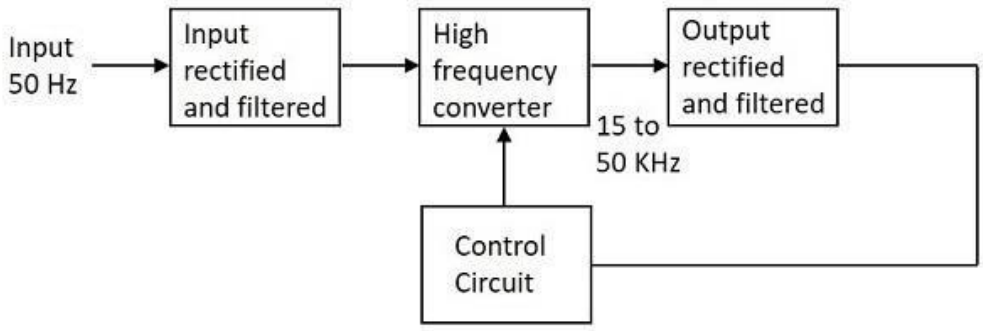
The disadvantages of LPS such as lower efficiency, the need for large value of capacitors to

reduce ripples and heavy and costly transformers etc. are overcome by the implementation of Switched Mode Power Supplies.

The working of SMPS is simply understood by knowing that the transistor used in LPS is used to control the voltage drop while the transistor in SMPS is used as a controlled switch.

Working

The working of SMPS can be understood by the following figure.



Input Stage

The AC input supply signal 50 Hz is given directly to the rectifier and filter circuit combination without using any transformer. This output will have many variations and the capacitance value of the capacitor should be higher to handle the input fluctuations. This unregulated dc is given to the central switching section of SMPS.

Switching Section

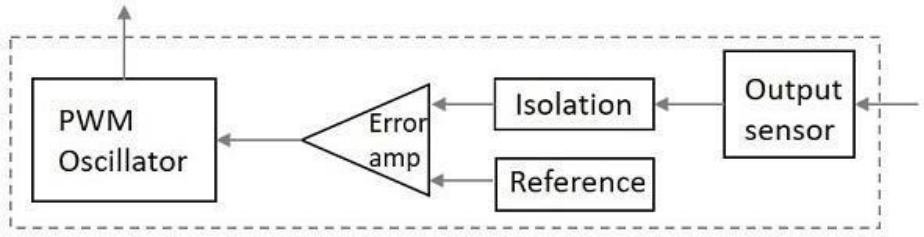
A fast switching device such as a Power transistor or a MOSFET is employed in this section, which switches ON and OFF according to the variations and this output is given to the primary of the transformer present in this section. The transformer used here are much smaller and lighter ones unlike the ones used for 60 Hz supply. These are much efficient and hence the power conversion ratio is higher.

Output Stage

The output signal from the switching section is again rectified and filtered, to get the required DC voltage. This is a regulated output voltage which is then given to the control circuit, which is a feedback circuit. The final output is obtained after considering the feedback signal.

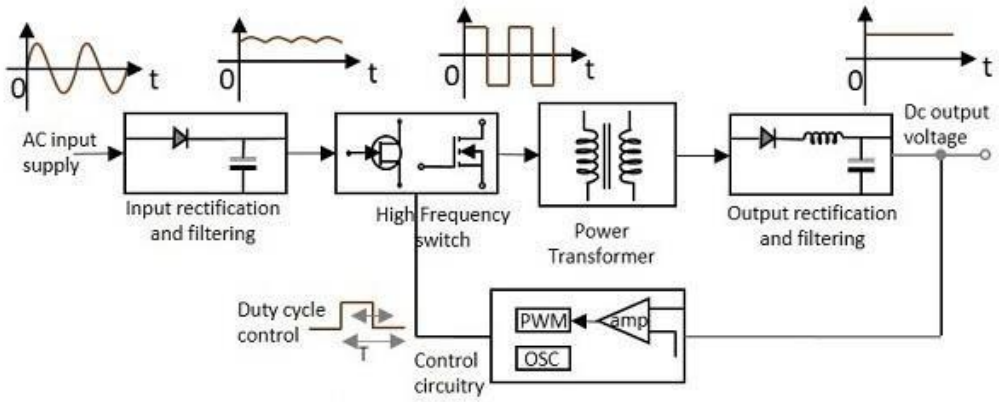
Control Unit

This unit is the feedback circuit which has many sections. Let us have a clear understanding about this from the following figure.



The above figure explains the inner parts of a control unit. The output sensor senses the signal and joins it to the control unit. The signal is isolated from the other section so that any sudden spikes should not affect the circuitry. A reference voltage is given as one input along with the signal to the error amplifier which is a comparator that compares the signal with the required signal level.

By controlling the chopping frequency the final voltage level is maintained. This is controlled by comparing the inputs given to the error amplifier, whose output helps to decide whether to increase or decrease the chopping frequency. The PWM oscillator produces a standard PWM wave fixed frequency.



Functional block diagram of SMPS

The SMPS is mostly used where switching of voltages is not at all a problem and where efficiency of the system really matters.

- SMPS circuit is operated by switching and hence the voltages vary continuously.
- The switching device is operated in saturation or cut off mode.
- The output voltage is controlled by the switching time of the feedback circuitry.
- Switching time is adjusted by adjusting the duty cycle.
- The efficiency of SMPS is high because, instead of dissipating excess power as heat, it continuously switches its input to control the output.

Disadvantages

- The noise is present due to high frequency switching.

- The circuit is complex.
- It produces electromagnetic interference.

Advantages

- The efficiency is as high as 80 to 90%
- Less heat generation; less power wastage.
- Reduced harmonic feedback into the supply mains.
- The device is compact and small in size.
- The manufacturing cost is reduced.
- Provision for providing the required number of voltages.

Applications

They are used in the motherboard of computers, mobile phone chargers, HVDC measurements, battery chargers, central power distribution, motor vehicles, consumer electronics, laptops, security systems, space stations, etc.

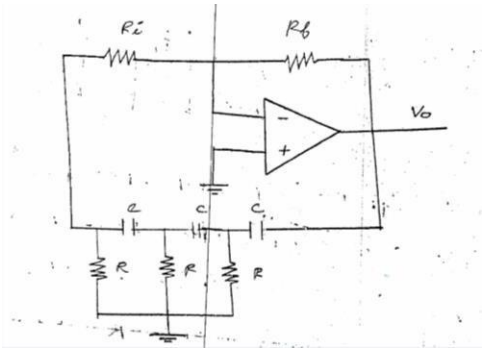
Types of SMPS

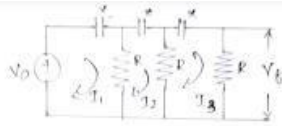
SMPS is the Switched Mode Power Supply circuit which is designed for obtaining the regulated DC output voltage from an unregulated DC or AC voltage. There are four main types of SMPS such as

- DC to DC Converter
- AC to DC Converter
- Fly back Converter
- Forward Converter

2. a) Explain in detail phase shift oscillator. (May 2014, May 2019)

b) Briefly explain the Barkhausen criterion for oscillation. With neat circuit diagram explain the construction and operation of RC phase shift oscillator using op-amp. Also derive the expression for frequency of oscillation. (Nov 2018)





$$\begin{bmatrix} R+x & -R & 0 \\ -R & 2R+x & -R \\ 0 & -R & 2R+x \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} V_0 \\ 0 \\ 0 \end{bmatrix}$$

$$\Delta = (R+x)\left((2R+x)^2 - R^2\right) + R(-R)(2R+x)$$
$$= (R+x)\left(x^2 + 4R^2 + 4Rx - R^2\right) - 2R^2 - xR$$
$$= (R+x)\left(3R^2 + x^2 + 4Rx\right) - 2R^2 - xR$$
$$= 3R^3 + x^2R + 4R^2x + 3R^2x + R^3 + 4Rx^2 - 2R^2 - xR$$
$$= 6R^2x + R^3 + 5Rx^2 + x^3$$

$$I_3 = \frac{\Delta I_3}{\Delta} = \frac{V_0R^2}{\Delta}$$

$$\Delta I_3 = \begin{pmatrix} R+x & -R & V_0 \\ -R & 2R+x & 0 \\ 0 & -R & 0 \end{pmatrix}$$
$$= V_0(-R)(-R)$$

$$I_3 = \frac{V_0R^2}{\Delta}$$

Multiplying both sides by R

$$RI_3 = \frac{V_0R^3}{\Delta} \qquad \therefore V_f = RI_3$$

$$\frac{V_f}{V_0} = \frac{R^3}{6R^2x + R^3 + 5Rx^2 + x^3}$$

$$\frac{V_f}{V_0} = \frac{1}{1 + 6/R\,x + \frac{5x^2}{R^2} + \frac{x^3}{R^3}}$$

$$x = \frac{1}{j\omega C}$$

$$\frac{V_f}{V_0} = \frac{1}{1 + \frac{6}{j\omega CR} - \frac{5}{\omega^2C^2R^2} + \frac{1}{j(\omega^3C^3R^3)}}$$

$$\alpha = \frac{1}{\omega RC}$$

$$\frac{1}{j} = -j, \quad \frac{1}{j^2} = -1, \quad \frac{1}{j^3} = j$$

$$\frac{V_f}{V_0} = \frac{1}{1 - j6\alpha - 5\alpha^2 + j\alpha^3}$$
$$= \frac{1}{(1-5\alpha^2) - j(6\alpha - \alpha^3)}$$

$$A\beta = \frac{A}{a+jb} \qquad a = 1 - 5\alpha^2, \quad b = \alpha^3 - 6\alpha$$
$$= \frac{A}{a+jb} \times \frac{a-jb}{a-jb}$$
$$= \frac{Aa}{a^2+b^2} - \frac{jAb}{a^2+b^2}$$

Condition for oscillation

$$A\beta = 1$$
$$A\beta = 1 + j0$$

$$\frac{A\alpha}{\alpha^2+b^2} = 1 \qquad \frac{jA\beta}{\alpha^2+b^2} = 0$$

$$A = -R_f/R_1$$

$$\frac{-jA\beta}{\alpha^2+b^2} = 0$$

$$b = 0 \quad \alpha^3 - b\alpha = 0$$

$$\alpha^3 = b\alpha$$

$$\alpha^2 = b \Rightarrow \alpha = \sqrt{b}$$

$$\alpha = \frac{1}{\omega CR}$$

$$\sqrt{b} = \frac{1}{\omega CR}$$

$$2\pi f = \frac{1}{\sqrt{b}\,CR}$$

$$f = \frac{1}{2\pi\sqrt{4}\,CR}$$

Real part is one

$$\frac{A}{1-5\alpha^2} = |A\beta|$$

$$\beta = \frac{1}{1-5\alpha^2}$$

$$\beta = \frac{1}{1-5(\sqrt{4})^2} = \frac{1}{-29}$$

$$|\beta| = \frac{1}{29}$$

$$A\beta = 1$$

$$A\left(\tfrac{1}{29}\right) = 1 \Rightarrow A = 29 \Rightarrow A\left|\frac{R_f}{R_1}\right| = 29$$

3. Derive the voltage gain and transfer function of second order active filter. (Nov 2014)

7.2.2 Second Order Active Filter

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two *RC* pairs and has a roll-off rate of −40 dB/decade. A general second order filter (Sallen-Key filter) is shown in Fig. 7.3. The results derived here can be used for analysing low pass and high pass filters.

The op-amp is connected as non-inverting amplifier and hence,

$$v_o = \left(1 + \frac{R_f}{R_1}\right) v_B = A_o v_B \tag{7.13}$$

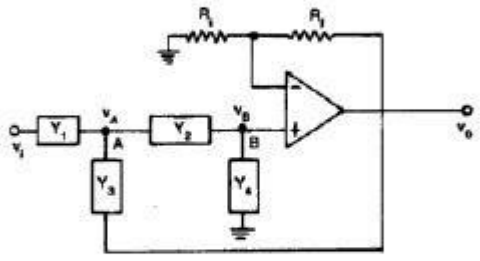


Fig. 7.3 Sallen-Key filter (General second order filter)

where $$A_o = 1 + \frac{R_f}{R_1} \tag{7.14}$$

and v_B is the voltage at node *B*.

Kirchhoff's current law (KCL) at node A gives

$$v_i Y_1 = v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - v_B Y_2$$

$$= v_A (Y_1 + Y_2 + Y_3) - v_o Y_3 - \frac{v_o Y_2}{A_o} \tag{7.15}$$

where v_A is the voltage at node *A*.

KCL at node B gives,

$$v_A Y_2 = v_B(Y_2 + Y_4) = \frac{v_b(Y_2 + Y_4)}{A_o}$$

$$v_A = \frac{v_b(Y_2 + Y_4)}{A_o Y_2} \tag{7.16}$$

Substituting Eq. (7.16) in Eq. (7.15) and after simplification, we get the voltage gain as

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \tag{7.17}$$

To make a low pass filter, choose, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = sC$ as shown in Fig. 7.4. For simplicity, equal components have been used.

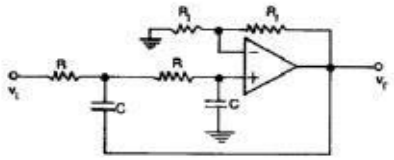


Fig. 7.4 Second order low-pass filter

From Eq. (7.17), we get the transfer function $H(s)$ of a low pass filter as,

$$H(s) = \frac{A_o}{s^2 C^2 R^2 + sCR(3 - A_o) + 1} \tag{7.18}$$

This is to note that from Eq. (7.18), $H(0) = A_o$ for $s = 0$ and $H(\infty) = 0$ for $s = \infty$ and obviously the configuration is for low pass active filter. It may be noted that for minimum dc offset $R_i R_f/(R_f + R_i) = R + R = 2R$ should be satisfied.

Second order physical systems have been studied extensively since long back and their step response, damping coefficient and its cause and effect relationship are known. We shall exploit those ideas in case of second order RC active filter. The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as,

$$H(s) = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2} \tag{7.19}$$

coefficient of 1.73. This gives better pulse response, however, causes attenuation in the upper end of the pass band.

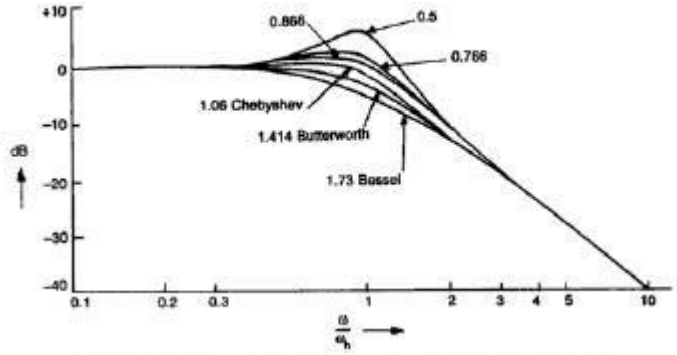


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_o = 1$)

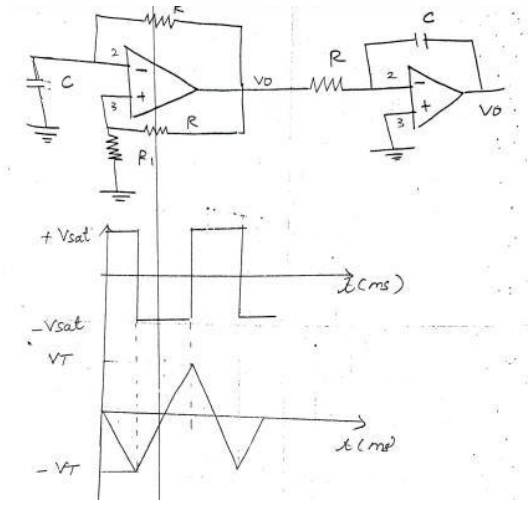
We shall discuss only Butterworth filter in this text as it has maximally flat response with damping coefficient $\alpha = 1.414$. From Eq. (7.24), with $\alpha = 1.414$, we get

$$20 \log |H(j\omega)| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^4}} \tag{7.25}$$

Hence for n-th order generalized low-pass Butterworth filter, the normalized transfer function for maximally flat filter can be written as

$$\left| \frac{H(j\omega)}{A_o} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h}\right)^{2n}}} \tag{7.26}$$

4. Explain the working of Triangular wave generator using operational amplifier. (Nov 2014)

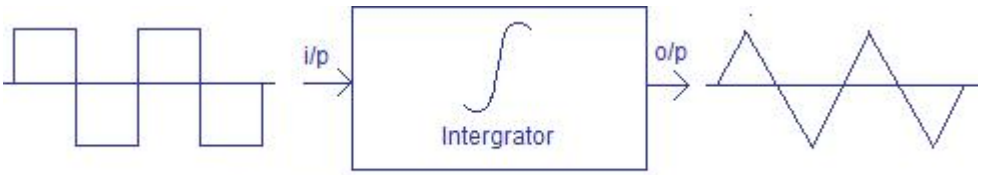


Triangular wave generator using op amp

There are many methods for generating triangular waves but here we focus on the method using op amps. This circuit is based on the fact that a square wave on integration gives a triangular wave.

Triangular waves

Triangular waves are a periodic, non-sinusoidal waveform with a triangular shape.



Generating triangular wave from a square wave

To generate triangular waves we need an input wave. Like triangular waves, square waves have equal rise and fall times so they are more convenient to be converted to a triangular waveform.

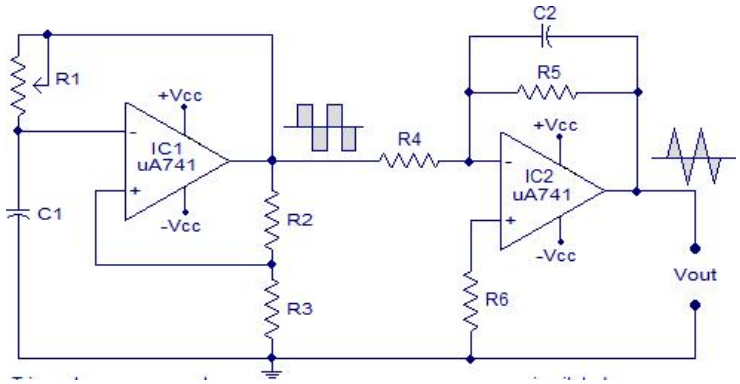
The main parts are

1. A square wave generator

2. An integrator which converts square waves to triangular waves.

The circuit uses an op-amp based square wave generator for producing the square wave and an op-amp based integrator for integrating the square wave. The circuit diagram is shown in the figure below.

Circuit diagram



The square wave generator section and the integrator section of the circuit are explained in detail below.

Square wave generator

The square wave generator is based on a uA741 op amp (IC1). Resistor R1 and capacitor C1 determines the frequency of the square wave. Resistor R2 and R3 forms a voltage divider setup which feedbacks a fixed fraction of the output to the non-inverting input of the IC.

Initially, when power is not applied the voltage across the capacitor C1 is 0. When the power supply is switched ON, the C1 starts charging through the resistor R1 and the output of the op amp will be high (+Vcc). A fraction of this high voltage is fed back to the non- inverting pin by the resistor network R2, R3. When the voltage across the charging capacitor is increased to a point the voltage at the inverting pin is higher than the non-inverting pin, the output of the op amp swings to negative saturation (-Vcc).

The capacitor quickly discharges through R1 and starts charging in the negative direction again through R1. Now a fraction of the negative high output (-Vcc) is fed back to the non-inverting pin by the feedback network R2, R3. When the voltage across the capacitor has become so negative that the voltage at the inverting pin is less than the voltage at the non-inverting pin, the output of the opamp swings back to the positive saturation. Now the capacitor discharges trough R1 and starts charging in positive direction. This cycle is repeated over time and the result is a square wave swinging between +Vcc and -Vcc at the output of the op amp.

If the values of R2 and R3 are made equal, then the frequency of the square wave can be expressed using the following equation

F=1 / (2.1976 R1C1)

Applications:

The applications of triangular wave include sampling circuits, thyristor firing circuits, frequency generator circuits, tone generator circuits etc.

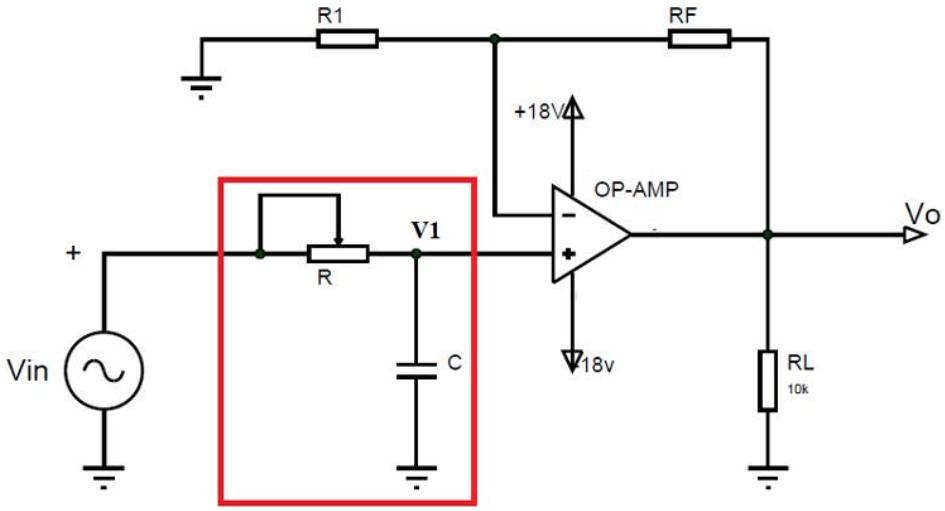
5. Explain the design procedure of first order and second order Butterworth low pass filter. (Nov 2015)

The main features of the Butterworth filter are:

- It is an R-C(Resistor, Capacitor) & Op-amp (operational amplifier) based filter
- It is an active filter so the gain can be adjusted if needed
- The key characteristic of Butterworth is that it has a flat passband and flat stopband. This is the reason it is usually called 'flat-flat filter'.

First Order Low Pass Butterworth Filter

The figure shows the circuit model of the first-order low-pass Butter worth filter.



In the circuit we have:

- Voltage 'Vin' as an input voltage signal which is analog in nature.
- Voltage 'Vo' is the output voltage of the operational amplifier.
- Resistors 'RF' and 'R1' are the negative feedback resistors of the operational amplifier.
- There is a single R-C network (marked in the red square) present in the circuit hence the filter is a first-order low pass filter

- 'RL' is the load resistance connected at the op-amp output.

If we use the voltage divider rule at point 'V1'then we can get the voltage across the capacitor as,

$$V1 = [\ -jXc / (R-jXc)\ ]\ Vin \quad \text{Here } -jXc = 1/2\pi fc$$

After substitution this equation we will have something like below

$$V1 = Vin / (1+j2\pi fRC)$$

Now the op-amp here used in negative feedback configuration and for such a case the output voltage equation is given as,

$$V0 = (\ 1 + RF / R1\ )\ V1\ .$$

If we substitute V1 equation into Vo we will have,

$$V0 = (1 + RF/ R1)\ [Vin / (1 + j2\pi fRC)\ ]$$

After rewriting this equation we can have,

$$V0 / Vin = AF / (\ 1 + j(f/fL)\ )$$

In this equation,

- V0 / Vin = gain of the filter as a function of frequency
- AF = (1+RF / R1) = passband gain of the filter
- f = frequency of the input signal
- fL = 1 / 2πRC = cutoff frequency of the filter. We can use this equation to choose appropriate resistor and capacitor values to select the cutoff frequency of the circuit.

If we convert the above equation into a polar form we will have,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_L}\right)^2}} \quad and \quad \theta = -\tan^{-1}\left(\frac{f}{f_L}\right)$$

Case1: f<<fL. So let us consider input frequency is very less than the cutoff frequency of the filter then,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(0)^2}} = A_F$$

Case2: f = fL. If the input frequency is equal to the cutoff frequency of the filter then,

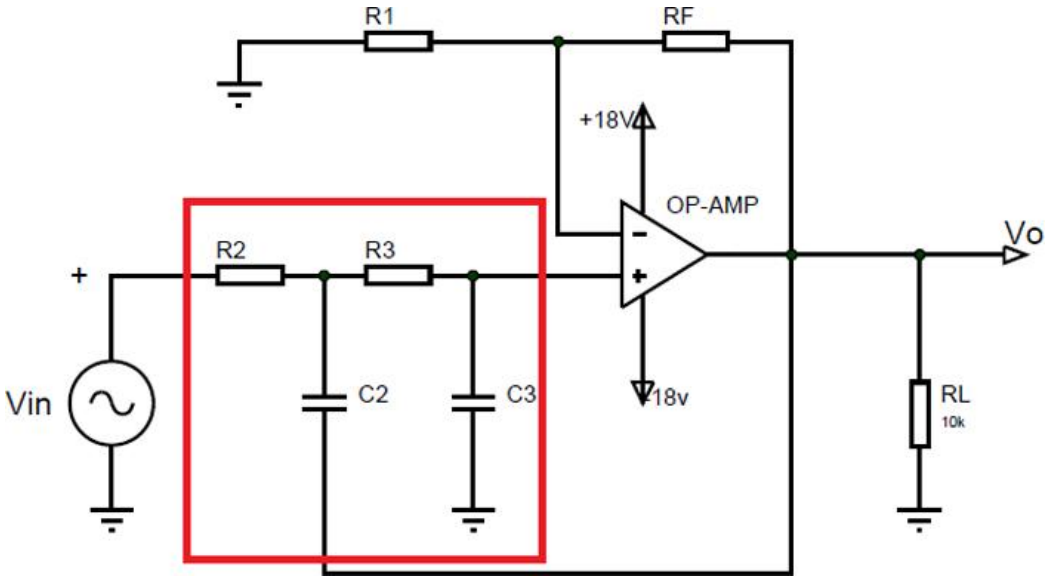
$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(1)^2}} = \frac{A_F}{\sqrt{2}} = 0.707 A_F$$

Case3: f >fL. If the input frequency is higher than the cutoff frequency of the filter then,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

Second-Order Butterworth Low Pass Filter

The figure shows the circuit model of the 2nd order Butterworth low pass filter.



In the circuit we have:

- Voltage ‘Vin’ as an input voltage signal which is analog in nature.
- Voltage ‘Vo’ is the output voltage of the operational amplifier.

- Resistors 'RF' and 'R1' are the negative feedback resistors of the operational amplifier.
- There is a double R-C network (marked in a red square) present in the circuit hence the filter is a second-order low pass filter.
- 'RL' is the load resistance connected at the op-amp output.

Second Order Low Pass Butterworth Filter Derivation

Second-order filters are important because higher-order filters are designed using them. The gain of the second-order filter is set by R1 and RF, while the cutoff frequency **fH** is determined by R2, R3, C2 & C3 values. The derivation for the cutoff frequency is given as follows,

fH = 1 / 2л(R2R3C2C3)1/2

The voltage gain equation for this circuit can also be found in a similar way as before and this equation is given below,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+\left(\frac{f}{f_H}\right)^4}}$$

In this equation,

- V0 / Vin = gain of the filter as a function of frequency
- AF = (1 + RF/R1) passband gain of the filter
- f = frequency of the input signal
- fH = 1 / 2л(R2R3C2C3)1/2 = cutoff frequency of the filter. We can use this equation to choose appropriate resistor and capacitor values to select the cutoff frequency of the circuit. Also if we choose the same resistor and capacitor in the R-C network then the equation becomes,

$$f_H = \frac{1}{2\pi\sqrt{R_2\,R_2C_2C_2}} = \frac{1}{2\pi\sqrt{R^2C^2}} = \frac{1}{2\pi RC}$$

Case1: f<<fH. So let us consider input frequency is very less than the cutoff frequency of the filter then,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(0)^4}} = A_F$$

Case2: f = fH. If the input frequency is equal to the cutoff frequency of the filter then,

$$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1+(1)^4}} = \frac{A_F}{\sqrt{2}} = 0.707A_F$$

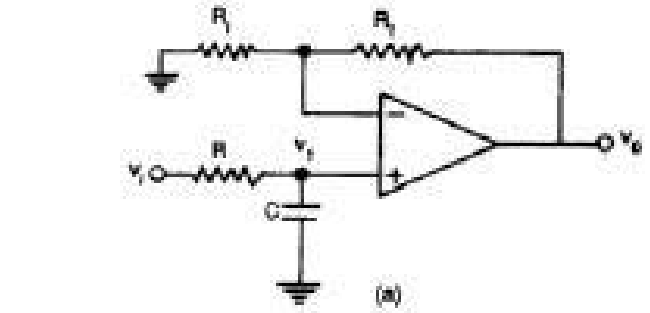
Case3: f >fH. If the input frequency is really higher than the cutoff frequency of the filter then,

$$\left|\frac{V_o}{V_{in}}\right| < A_F$$

6. Derive the transfer function and draw the frequency response of first order LPF. (Nov 2016, May 2017)

7.2.1 First Order Low Pass Filter

Active filters may be of different orders and types. A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier and is shown in Fig. 7.2 (a). Resistors R_i and R_f determine the gain of the filter in the pass band.



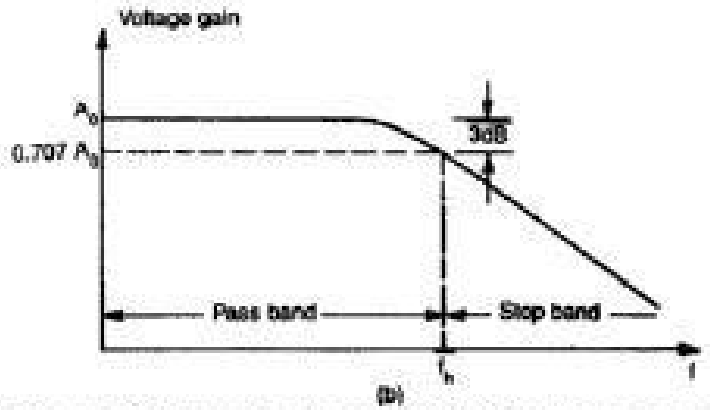


Fig. 7.2 (a) First order low-pass filter (b) Frequency response

The voltage v_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

so, $$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1} \quad (7.4)$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_0 of the op-amp is,

$$A_0 = \frac{V_0(s)}{V_1(s)} = \left(1 + \frac{R_f}{R_i}\right) \quad (7.5)$$

So, the overall transfer function from Eq. (7.4) and (7.5) is

$$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{V_0(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_0}{RCs + 1} \quad (7.6)$$

Let $$\omega_h = \frac{1}{RC} \quad (7.7)$$

Therefore, $$H(s) = \frac{V_0(s)}{V_i(s)} = \frac{A_0}{\frac{s}{\omega_h} + 1} = \frac{A_0 \omega_h}{s + \omega_h} \quad (7.8)$$

This is the standard form of the transfer function of a first order low-pass system.

To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H(j\omega) = \frac{A_0}{1 + j\omega RC} = \frac{A_0}{1 + j(f/f_h)} \quad (7.9)$$

where $$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H(j\omega)| \approx A_0 \quad (7.10)$$

At $f = f_h$,

$$|H(j\omega)| = \frac{A_0}{\sqrt{2}} = 0.707 A_0 \quad (7.11)$$

At very high frequency i.e. $f >> f_h$

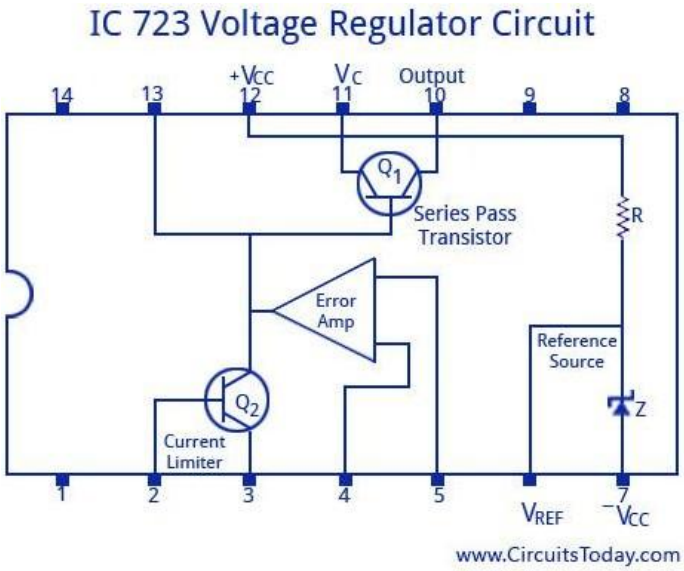
$$|H(j\omega)| << A_0 \approx 0 \quad (7.12)$$

The frequency response of the first order low pass filter is shown in Fig. 7.2 (b). It has the maximum gain, A_0 at $f = 0$ Hz. At f_h the gain falls to 0.707 time (i.e. –3 dB down) the maximum gain (A_0). The frequency range from 0 to f_h is called the pass band. For $f > f_h$ the gain decreases at a constant rate of –20 dB/decade. That is, when the frequency is increased ten times (one decade), the voltage gain is divided by ten or in terms of dBs, the gain decreases by 20 dB (= 20 log 10). Hence, gain rolls off at the rate of 20 dB/decade or 6 dB/octave after frequency, f_h. The frequency range $f > f_h$ is called the stop band. Obviously, the low pass filter characteristics obtained is not an ideal one as the rate of decay is small for the first order filter.

7. Draw and explain the functional diagram of 723 general purpose regulator. (May 2017)

The functional diagram of the voltage regulator is shown below. It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both positive and negative voltage regulators with an

output voltage ranging from 2 V to 37 V, and output current levels upto 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.



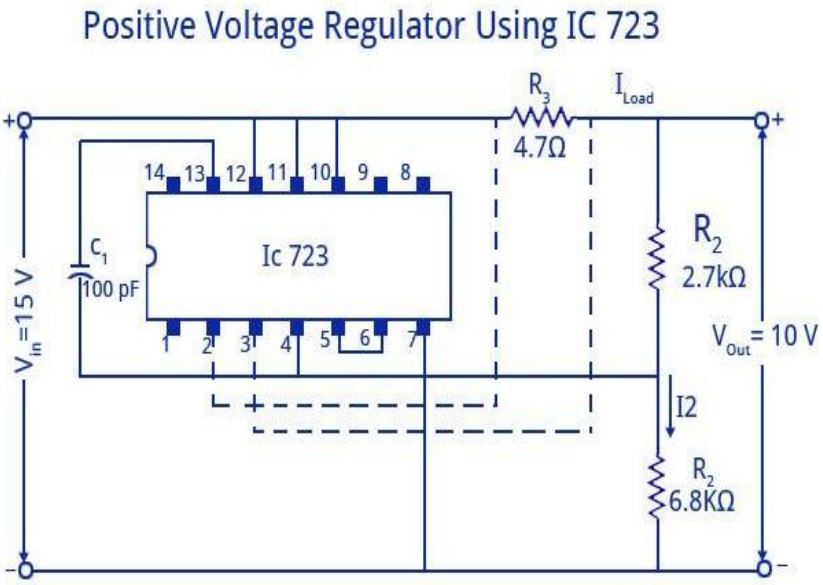
IC 723 Voltage Regulator Circuit

The functional diagram of the voltage regulator is shown below. It consists of a voltage reference source (Pin 6), an error amplifier with its inverting input on pin 4 and non-inverting input on pin 5, a series pass transistor (pins 10 and 11), and a current limiting transistor on pins 2 and 3. The device can be set to work as both positive and negative voltage regulators with an output voltage ranging from 2 V to 37 V, and output current levels upto 150 m A. The maximum supply voltage is 40 V, and the line and load regulations are each specified as 0.01%.

The figure shown below is a positive voltage regulator with an IC 723. The output voltage can be set to any desired positive voltage between (7-37) volts. 7 volts is the reference starting voltage. All these variations are brought with the change of values in resistors R1 and R2 with the help of a potentiometer.

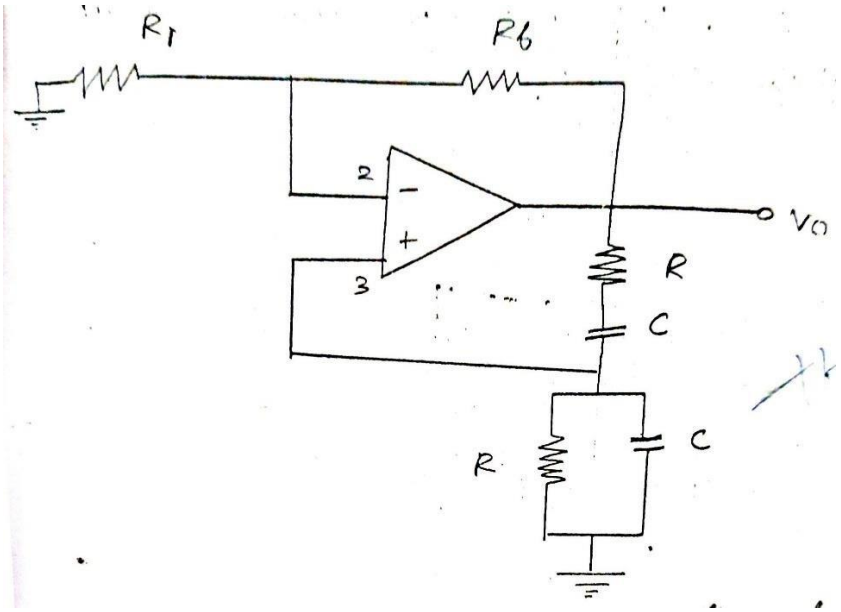
A darlington connection is made by the transistor to Q1 to handle large load current. The broken lines in the image indicate the internal connections for current limiting. Even foldback current limiting is possible in this IC. A regulator output voltage less than the 7 V reference level can be obtained by using a voltage divider across the reference source. The potentially divided reference voltage is then connected to terminal 5.

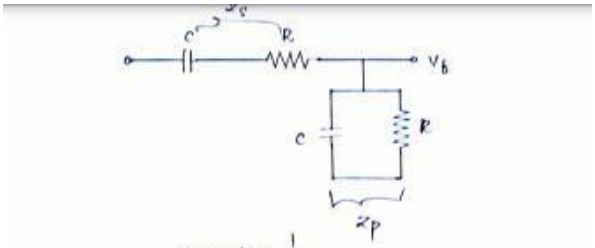
Another important point to note about this IC is that the supply voltage at the lowest point on the ripple waveform, should be at least 3 V greater than the output of the regulator and greater than Vref. If it is not so a high-amplitude output ripple is possible to occur.



Positive Voltage Regulator Using IC 723

8. Explain about Wein Bridge oscillator with necessary circuit diagrams and expressions. (Nov 2017)





$$Z_S = R + \frac{1}{j\omega C}$$

$$= \frac{j\omega CR + 1}{j\omega C}$$

$$\frac{1}{Z_p} = \frac{1}{R} + j\omega C = \frac{1 + j\omega CR}{R}$$

$$Z_p = \frac{R}{1 + j\omega CR}$$

Voltage division,

$$V_o = \frac{V_f Z_p}{Z_S + Z_p}$$

$$V_o = \frac{V_f \left(\frac{R}{1+j\omega CR}\right)}{\frac{1+j\omega CR}{j\omega C} + \frac{R}{1+j\omega CR}}$$

$$\frac{V_o}{V_f} = \frac{\frac{R}{1+j\omega CR}}{\frac{(1+j\omega CR)(1+j\omega CR) + j\omega CR}{j\omega C\,(1+j\omega CR)}}$$

$$\frac{V_o}{V_f} = \frac{\cancel{R}}{\frac{\cancel{(1+j\omega CR)}}{1 + j\omega CR + j\omega CR(j\omega CR) + j\omega CR}{j\omega C\,(\cancel{1+j\omega CR})}}$$

$$\frac{V_o}{V_f} = \frac{R(j\omega C)}{1 + 3j\omega CR + j^2\omega^2 C^2 R^2}$$

$$\frac{V_o}{V_f} = \frac{j\omega CR}{(1 - \omega^2 C^2 R^2) + 3j\omega CR}$$

$$= \frac{Rj\omega C}{1 - \omega^2 C^2 R^2 + 3j\omega CR} \times \frac{(1 - \omega^2 C^2 R^2) - 3j\omega CR}{(1 - \omega^2 C^2 R^2) - 3j\omega CR}$$

$$\beta = \frac{j\omega RC(1 - \omega^2 C^2 R^2) + 3\omega^2 R^2 C^2}{(1 - \omega^2 C^2 R^2) + 9\omega^2 C^2 R^2}$$

Condition for oscillation

$$A\beta = 1 + j0$$

$$A\beta = 1$$

$$\frac{A\left(j\omega RC(1 - \omega^2 C^2 R^2) + 3\omega^2 R^2 C^2\right)}{(1 - \omega^2 C^2 R^2)^2 + 9\omega^2 C^2 R^2} = 1 \angle$$

Equating Real part

$$\frac{A(3\omega^2 R^2 C^2)}{(1 - \omega^2 C^2 R^2)^2 + 9\omega^2 C^2 R^2} = 1 \angle$$

$$\omega^2 = 1/R^2 C^2$$

$$\frac{A\left(3\left(\omega^2 \times \frac{1}{\omega^2}\right)\right)}{\left(1-\omega^2 \times \frac{1}{\omega^2}\right)^2 + 9\omega^2 \times \frac{1}{\omega^2}} = 1$$

$$\frac{3A}{0+9} = 1$$

$$3A = 9$$

$$A = 9/3$$

$$\left(1+\frac{R_f}{R_i}\right) = 9/3$$

$1+R_f/R_i = 3$ gain of the amplifier

$$\frac{R_f}{R_i} = 3-1$$

$$\frac{R_f}{R_i} = 2$$

$\boxed{R_f = 2R_i}$ is the required condition

Equating imaginary part,

$$\frac{j\omega RC\left(1-\omega^2R^2C^2\right)}{\left(1-\omega^2C^2R^2\right)^2 + 9\omega^2C^2R^2} = 0$$

$$1-\omega^2R^2C^2 = 0$$

$$\omega^2R^2C^2 = 1$$

$$\omega^2 = \frac{1}{R^2C^2}$$

$$(2\pi f)^2 = \frac{1}{R^2C^2}$$

$$f^2 = \frac{1}{4\pi^2R^2C^2}$$

$$f = 1/4\pi RC$$

9. Design a second order Butterworth low pass filter having upper cut-off frequency 1 kHz. These determine its frequency response. (May 2018)

$$K = 3 - \frac{1}{Q} = 3 - \frac{1}{0.707} = 1.586$$

and $$R_F = (K-1)R_1 = (1.586-1) \times 15{,}916 = 9327\ \Omega$$

$$R_a = \frac{RK}{3-K} = \frac{15{,}916 \times 1.586}{3-1.586} = 17{,}852\ \Omega$$

$$R_b = \frac{RK}{2K-3} = \frac{15{,}916 \times 1.586}{2 \times 1.586 - 3} = 146{,}760\ \Omega$$

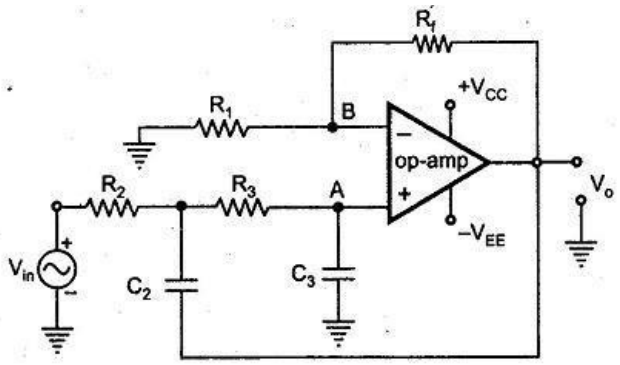
$$|H(j0)| = 3 - K = 3 - 1.586 = 1.414$$

10. Draw circuit of II order Butterworth active low pass filter and derive its transfer function. (May 2019, Sep 2020)

Second Order Low Pass Butterworth Filter:

The practical response of Second Order Low Pass Butterworth Filter must be very close to an

ideal one. In case of low pass filter, it is always desirable that the gain rolls off very fast after the cut off frequency, in the stop band. In case of first order filter, it rolls off at a rate of 20 dB/decade. In case of second order filter, the gain rolls. off at a rate of 40 dB/decade. Thus, the slope of the frequency response after $f = f_H$ is — 40 dB/decade, for a second order low pass filter.



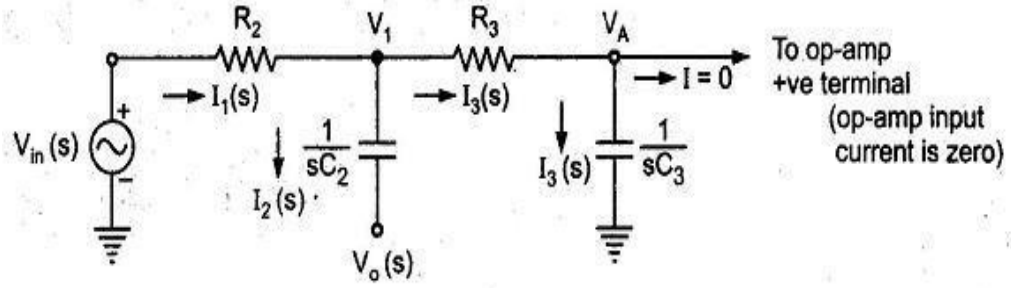
A first order filter can be converted to second order type by using an additional RC network as shown in the Fig.

The cut off frequency f_H for the filter is now decided by R_2, C_2, R_3 and C_3. The gain of the filter is as usual decided by op-amp i.e. the resistance R_1 and R_f.

Analysis of the Filter Circuit:

For deriving the expression for the cut off frequency, let us use the Laplace transform method.

The input RC network can be represented in the Laplace domain as shown in Fig.



$$I_1 = I_2 + I_3$$

$$\frac{V_{in} - V_1}{R_2} = \frac{V_1 - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_1 - V_A}{R_3}$$

Using potential divider rule, we can Write

$$V_A = V_1 \left[\frac{\frac{1}{sC_3}}{R_3 + \frac{1}{sC_3}} \right]$$

$$V_A = \frac{V_1}{1 + sR_3 C_3}$$

$$V_1 = V_A (1 + s R_3 C_3)$$

Substituting in (1) and solving for VA, we get

$$\frac{V_{in} - V_A (1+sR_3 C_3)}{R_2} = \frac{V_A (1+s R_3 C_3) - V_o}{\left(\frac{1}{sC_2}\right)} + \frac{V_A (1+s R_3 C_3) - V_A}{R_3}$$

$$\frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{(1+s R_3 C_3)}{R_2} + s C_2 (1+s R_3 C_3) + \frac{(1+s R_3 C_3)}{R_3} - \frac{1}{R_3} \right]$$

$$\therefore \frac{V_{in}}{R_2} + V_o (s C_2) = V_A \left[\frac{R_3 (1+s R_3 C_3) + R_2 R_3 s C_2 (1+s R_3 C_3) + R_2 (1+s R_3 C_3) - R_2}{R_2 R_3} \right]$$

$$\therefore (R_3 V_{in} + V_o s R_2 R_3 C_2) = V_A [(1 + s R_3 C_3) (R_3 + R_2 R_3 s C_2 + R_2) - R_2]$$

$$V_A = \frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{[(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2]}$$

Now, for op-amp in noninverting configuration,

$$V_o = A_F V_A$$

where $A_F = 1 + \frac{R_f}{R_1}$

and V_A = the voltage at the noninverting terminal

$$\therefore V_o = A_F \left[\frac{R_3 V_{in} + V_o s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} \right]$$

$$\therefore \frac{A_F R_3 V_{in}}{(1+s R_3 C_3)(R_3 + R_2 R_3 C_2 s + R_2) - R_2} = V_o \left[1 - \frac{s R_2 R_3 C_2}{(1+s R_3 C_3)(R_3 + R_3 R_2 C_2 s + R_2) - R_2} \right]$$

$$\therefore A_F R_3 V_{in} = V_o [(1 + s R_3 C_3) (R_3 + R_3 R_2 C_2 s + R_2) - R_2 - s R_2 R_3 C_2]$$

$$\therefore \frac{V_o}{V_{in}} = \frac{A_F}{s^2 + \frac{(R_3 C_3 + R_2 C_3 + R_2 C_2 - A_F R_2 C_2) s}{R_2 R_3 C_2 C_3} + \frac{1}{R_2 R_3 C_2 C_3}}$$

As the order of s in the gain expression is two, the filter is called Second Order Low Pass Butterworth Filter.

Second Order Butterworth Filter Transfer Function:

The standard form of Second Order Butterworth Filter Transfer Function of any second order system is

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

A = overall gain

ξ = damping of system

ω_n = natural frequency of oscillations

$$\omega_n^2 = \frac{1}{R_2 R_3 C_2 C_3}$$

In case of Second Order Low Pass Butterworth Filter, this frequency is nothing but the cut-off frequency, ω_H .

$$\therefore \quad \omega_H^2 = \frac{1}{R_2 R_3 C_2 C_3}$$

$$\therefore \quad (2\pi f_H)^2 = \frac{1}{R_2 R_3 C_2 C_3}$$

$$\therefore \quad f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}}$$

This is the required cut off frequency.

Replacing s by jω, the transfer function can be written in the frequency domain and hence, finally, can be expressed in the polar form as,

$$\frac{V_o}{V_{in}} = \left|\frac{V_o}{V_{in}}\right| \angle \phi$$

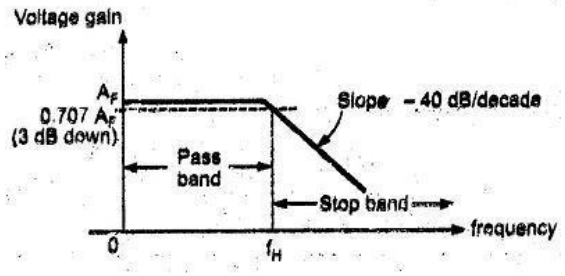
where $$\left|\frac{V_o}{V_{in}}\right| = \frac{A_F}{\sqrt{1 + \left(\frac{f}{f_H}\right)^4}}$$

and A_F = gain of filter in pass band

f = input frequency in Hz

f_H = high cut-off frequency in Hz

The frequency response is shown in Fig.



At the cut off frequency f_H, the gain is 0,707 A_f i,e. 3 dB down from its 0 Hz level. After, f_H ($f > f_H$) the gain rolls off at a frequency rate of 40 dB/decade,. Hence, the slope of the 'responseafter, f_H is – 40 dB/decade.

Design Steps:

The design steps for Second Order Low Pass Butterworth Filter are

1) Choose the cut-off frequency f_H,

2) The design can be simplified by selecting $R_2 = R_3 = R$ and $C_2 = C_3 = C$ And choose a value of C less than or equal to 1 μF.

3) Calculate the value of R from the equation,

$$f_H = \frac{1}{2\pi\sqrt{R_2 R_3 C_2 C_3}} = \frac{1}{2\pi RC}$$

4) As

$R_2 = R_3 = R$ and $C_2 = C_3 = C$, the pass band voltage gain $A_F = (1 + R_f / R_1)$ of the second order low pass filter has to be equal to 1.586.

Note : For $R_2 = R_3 = R$ and $C_2 = C_3 = C$, the transfer function takes the form

$$\frac{V_o(s)}{V_{in}(s)} = \frac{A_F}{s^2 + \frac{3 - A_F}{RC}s + \frac{1}{R^2C^2}}$$

From this we can write that,

$$\xi = \text{damping factor} = \frac{3 - A_F}{2}$$

Now, for Second Order Low Pass Butterworth Filter, the damping factor required is 0.707, from the normalised Butterworth polynomial.

$$0.707 = \frac{3 - A_F}{2}$$

$$A_F = 1.586$$

Thus, to ensure the Butterworth response, it is necessary that the gain A_f is 1.586.

$$1.586 = 1 + \frac{R_f}{R_1}$$

$$R_f = 0.586\ R_1$$

Hence, choose a value of $R_1 \leq 100\ k\Omega$ and calculate the corresponding value of

The frequency scaling method discussed earlier for first order filter is equally applicable to the Second Order Low Pass Butterworth Filter

11. a) Explain the operation of NE 566 voltage controlled oscillator with its block diagram and obtain the expression for its output frequency. (Nov 2018)

b) Explain IC 566 VCO operation and detail any two applications. (May 2019)

VCO (Voltage controlled oscillator)

Voltage controlled oscillator is a type of oscillator where the frequency of the output oscillations can be varied by varying the amplitude of an input voltage signal. Voltage controlled oscillators are commonly used in frequency (FM), pulse (PM) modulators and phase locked loops (PLL).

The block diagram of a typical voltage controlled oscillator is shown.

Voltage controlled oscillators can be broadly classified into a linear voltage controlled oscillators and relaxation type voltage controlled oscillators. Linear voltage controlled oscillators are generally used to produce a sine wave. In such oscillators, an LC tank circuit is used for producing oscillations. An active element like a transistor is used for amplifying the output of the LC tank circuit, compensating the energy lost in the tank circuit and for establishing the necessary feedback conditions. Here a varactor (varicap) diode is used in place of the capacitor in the tank circuit. A varactor diode is a type of semiconductor diode whose capacitance across the junction can be varied by varying the voltage across the junction. Thus by varying the voltage across the varicap diode in the tank circuit, the output frequency of the VCO can be varied.

Relaxation-type voltage controlled oscillators are used to produce a saw-tooth or triangular waveform. This is achieved by the gradual charging and sudden discharge of a capacitor connected appropriately to an active element (UJT, PUT etc) or a monolithic IC (LM566 etc). Nowadays relaxation type VCOs are generally realized using monolithic ICs.

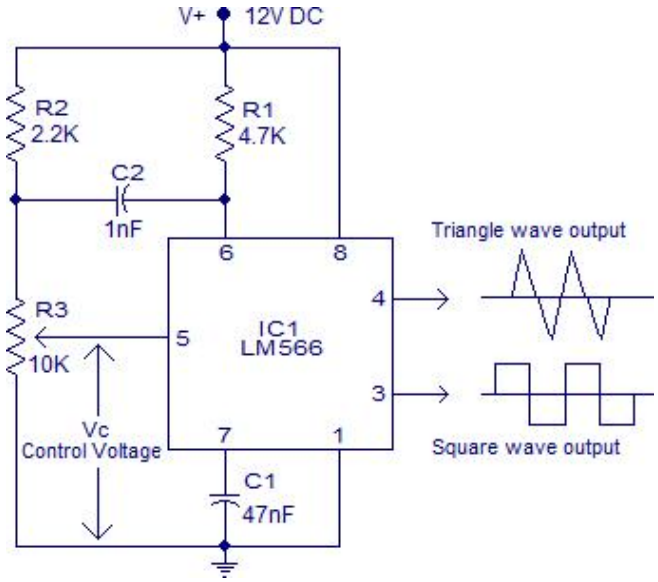
Voltage controlled oscillator using LM566 IC

LM566 is a monolithic voltage controlled oscillator from National Semiconductors. It can be

used to generates square and triangle waveforms simultaneously. The frequency of the output waveform can be adjusted using an external control voltage. The output frequency can be also programmed using a set of external resistor and capacitor.

Typical applications of LM566 IC are signal generators, FM modulators, FSK modulators, tone generators etc. The LM566 IC can be operated from a single supply or dual supply. While using a single supply, the supply voltage range is from 10V to 24V. The IC has a very linear modulation characteristic and has excellent thermal stability. The circuit diagram of a voltage controlled oscillator using LM566 is shown in the figure below.

Circuit Diagram



Working

Resistor R1 and capacitor C1 form the timing components. Capacitor C2 is used to prevent the parasitic oscillations during VCO switching. Resistor R3 is used to provide the control voltage Vc. Triangle and square wave outputs are obtained from pins 4 and 3 respectively. The output frequency of the VCO can be obtained using the following equation:

Fout = 2.4(V+-V5) /(R1C1V+) . Where Fout is the output frequency, R1 and C1 are the timing components and V+ is the supply voltage.

BM T45 – LINEAR INTEGRATED CIRCUITS

UNIT- 4

PART-A

1. Define Pull in time. (May 2014)

- The total time taken by the PLL to establish lock is called pull- in time.

2. Define Settling time. (May 2014)

- It represents the time it takes for the output to settle within a specified band ±½LSB of its final value following a code change at the input (usually a full scale change).
- It depends upon the switching time of the logic circuitry due to internal parasitic capacitance & inductances.
- Settling time ranges from 100ns. 10μs depending on word length & type circuit used.

3. What are the applications of 555 timer in monostable mode? (Nov 2014, Nov 2017)

- Missing pulse detector.
- Linear ramp generator.
- Frequency divider.
- Pulse width modulation.

4. What is Lock in range of PLL? (Nov 2014, Nov 2016, May 2019, Sept 2020)

- When PLL is in lock, it can trap frequency changes in the incoming signal.
- The range of frequencies over which the PLL can maintain lock with the incoming signal is called as lock range.

5. Define phase transfer conversion coefficient of PLL. (Nov 2015)

- Transfer function describes how PLL responds to excess reference phase.

6. Mention the applications of Schmitt trigger. (Nov 2015)

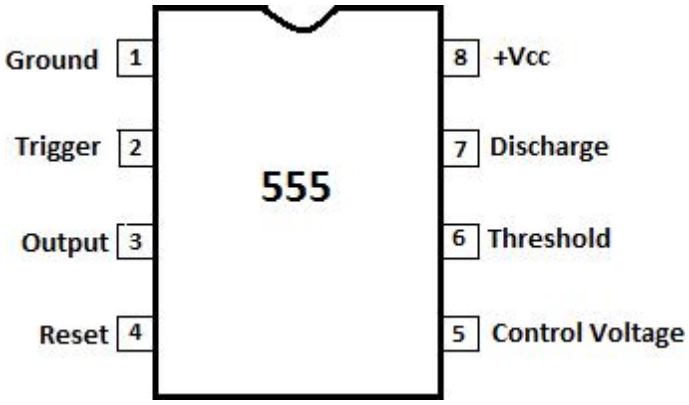
- To convert sine into square waves these circuits are used.
- It can be used as simple switches and use it as ON or OFF controllers.
- In the signal conditioning to eliminate the noise from the signals and use it in digital circuits, these triggering circuits are used.

- The negative feedback in closed-loop configurations of these circuits can be used as Relaxation Oscillators, Function Generators, and also used in power supplies switching.
- Schmitt triggers are used as level detectors.

7. What are the modes of operations of a timer. (Nov 2016)

- Monostable
- Astable
- Bistable.

8. Draw the pin diagram of IC 555 timer. (May 2017, Sept 2020)



9. What are the essential parts of PLL? (May 2017, Nov 2018)

- Phase detector
- Low-pass filter
- Voltage controlled oscillator
- Feedback path

10. Define 'capture range' of PLL. (Nov 2017)

- The range of frequencies over which the PLL can acquire lock with the input signal is called as capture range.

11. Enlist the important features of 555 timer circuit. (May 2018)

- It has two basic operating modes: monostable and astable
- It is available in three packages. 8 pin metal can, 8 pin dip, 14 pin dip.
- It has very high temperature stability.

12. Mention the applications of 565 PLL. (May 2018)

- Frequency multiplier
- Frequency synthesizer
- FM detector

13. Define duty cycle. (Nov 2018)

- The ratio of high output and low output period is given by a mathematical parameter called duty cycle.
- It is defined as the ratio of ON Time to total time.

14. List the applications of 555 timer IC. (May 2019)

- Astable multivibrator.
- Monostable multivibrator.
- Pulse position modulator.
- Schmitt trigger.

PART-B

1. a) Explain in detail the monostable multivibrator using 555 timer. (April/May 2014)

b) Explain monostable multivibrator using 555 IC. (Nov 2015)

c) Describe the monostable operation of 555 timer with required functional diagram, timing pulses and graph. (Nov/ Dec 2017}

Figure 8.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 8.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{cc}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH ($= V_{cc}$). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{cc} with a time constant RC

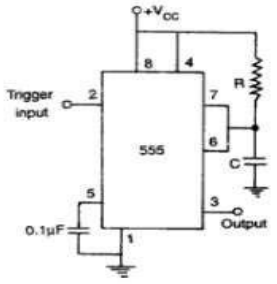


Fig. 8.3 Monostable multivibrator

as in Fig. 8.5(b). After a time period T (calculated later) the capacitor voltage is just greater than (2/3) V_{cc} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\overline{Q} = 1$, transistor Q_1 goes ***on*** (i.e. saturates), thereby

discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 8.5 (c).

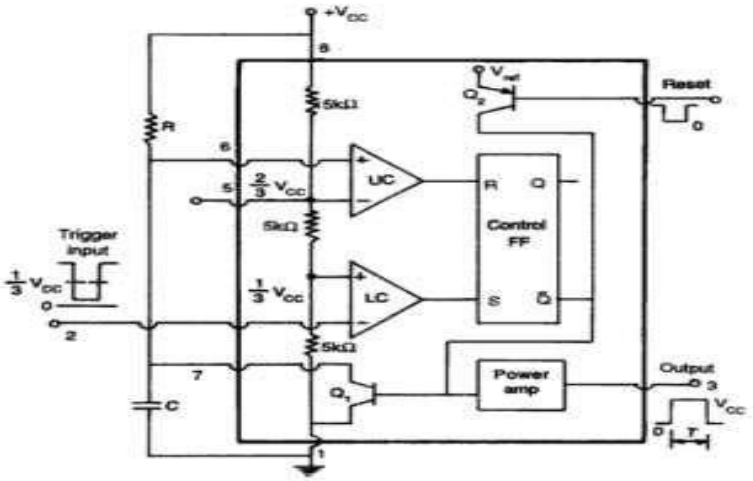


Fig. 8.4 Timer in monostable operation with functional diagram

The voltage across the capacitor as in Fig. 8.5(b) is given by

$$v_c = V_{cc}\,(1 - e^{-t/RC}) \qquad (8.1)$$

At $t = T$, $v_c = (2/3)\,V_{cc}$

Therefore, $\frac{2}{3}V_{cc} = V_{cc}\,(1 - e^{-T/RC})$

or, $T = RC \ln (1/3)$

or, $T = 1.1\ RC$ (seconds) (8.2)

It is evident from Eq. (8.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 8.5(d) is applied to the reset terminal (pin-4)

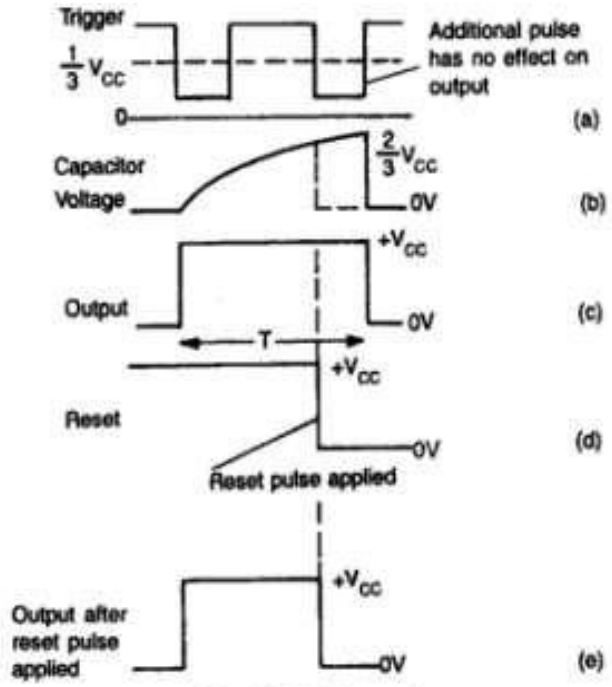


Fig. 8.5 Timing pulses

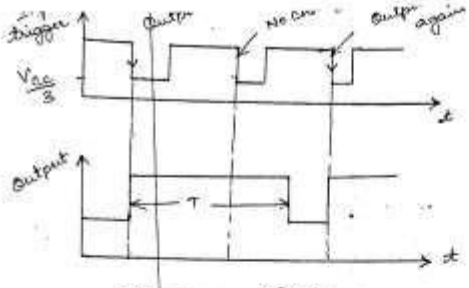
2. a) What are the applications of timer? Explain in detail any three. (April/May 2014)

b) Explain in detail about any 3 applications of a 555 timer with relevant circuit diagrams and waveforms. (Nov 2016)

c) Describe any 2 applications of IC 555 timer when it is working in monostable and astable modes. (May 2017)

Frequency Divider :

* A continuously triggered monostable circuit when triggered by a square wave generator can be used as frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal.
* The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH for next negative going edge of the input square wave.



Frequency divider

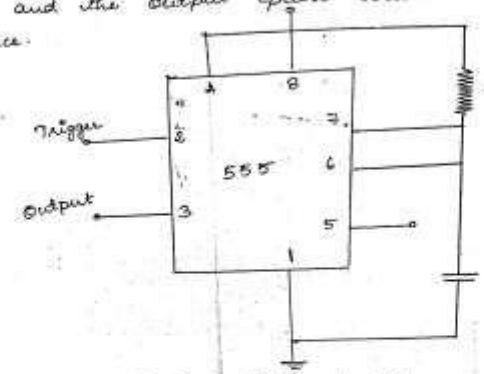
* The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay.
* In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

Pulse Width Modulation :

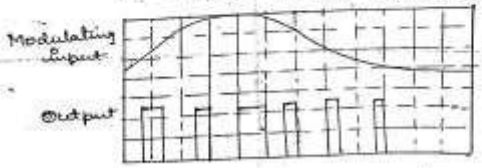
* This is basically a monostable multivibrator with a modulating input signal applied at pin 5
* By the applications of the continuous trigge at pin-2, a series of output pulses are obtained, the duration of which depends of whic depends on the modulation input at pin-5.
* The modulating signal applied at pin-5 gets superimposed upon the already existing

Voltage $(\frac{2}{3})V_{cc}$ at the inverting input of UC.

* This in turn changes the threshold level of UC and the output pulse width modulation takes place.



Pulse width modulator

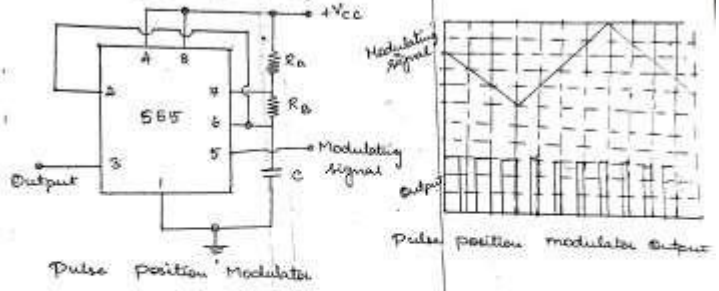


* It may be noted from the output waveform that the pulse duration, that is the duty cycle only varies, keeping the frequency same as that of the continuous input pulse at trigger.

Pulse position Modulator

* The pulse-position Modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation.

* The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.



Pulse position modulator output

Pulse position Modulator

* It may be noted from the output waveform that the frequency is varying leading to pulse position modulation.

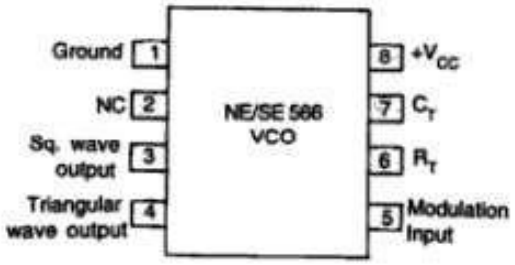
* The typical practical component values may be noted as $R_A = 3.9\ k\Omega$; $R_B = 3\ k\Omega$, $C = 0.01\ \mu F$, $V_{cc} = 5V$.

3. a) Explain the principle of VCO. (Nov 2014)

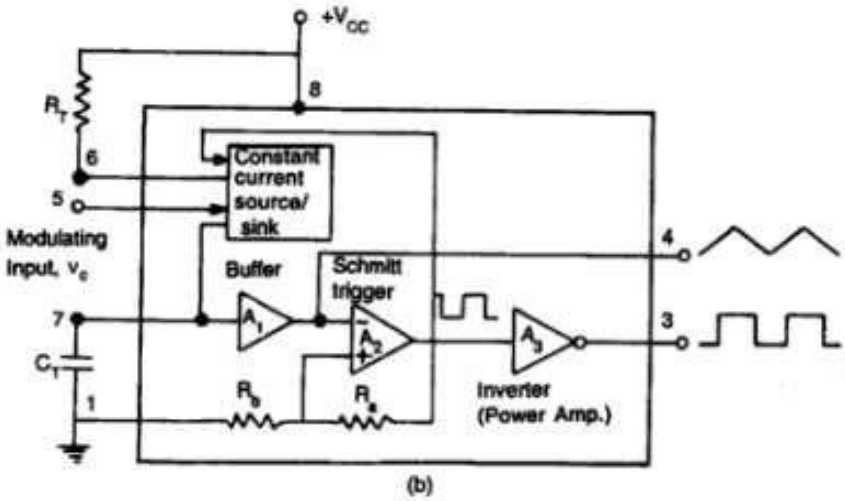
b) Discuss in detail about the working of VCO. (Nov/ Dec 2017)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 9.7(a, b). Referring to Fig. 9.7(b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 9.7(c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt



(a)



(b)

Fig. 9.7 Voltage controlled oscillator (a) Pin configuration (b) Block diagram

trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 9.7(c).

The output frequency of the VCO can be calculated as follows:

The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

So $$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

or, $$\frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or, $$\Delta t = \frac{0.25\ V_{cc} C_T}{i} \qquad (9.8)$$

4. Explain the working principle of 555 timer with its functional diagram. How 555 timer is used as a monostable multivibrator. (Nov 2014)

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8–pin circular style, TO–99 can or 8–pin mini DIP or as 14–pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

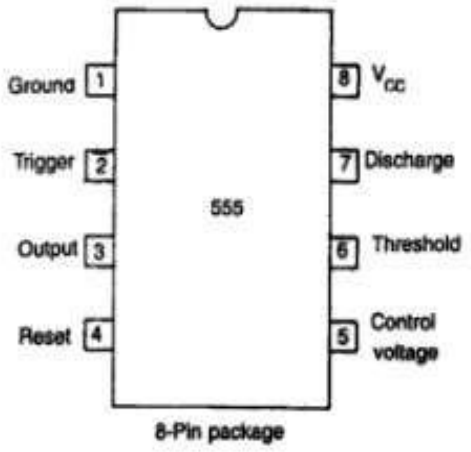


Fig. 8.1 Pin diagram

Figure 8.1 gives the pin diagram and Fig. 8.2 gives the functional diagram for 555 IC timer. Referring to Fig. 8.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{cc} to the upper comparator (UC) and (1/3) V_{cc} to the lower comparator (LC), where V_{cc} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

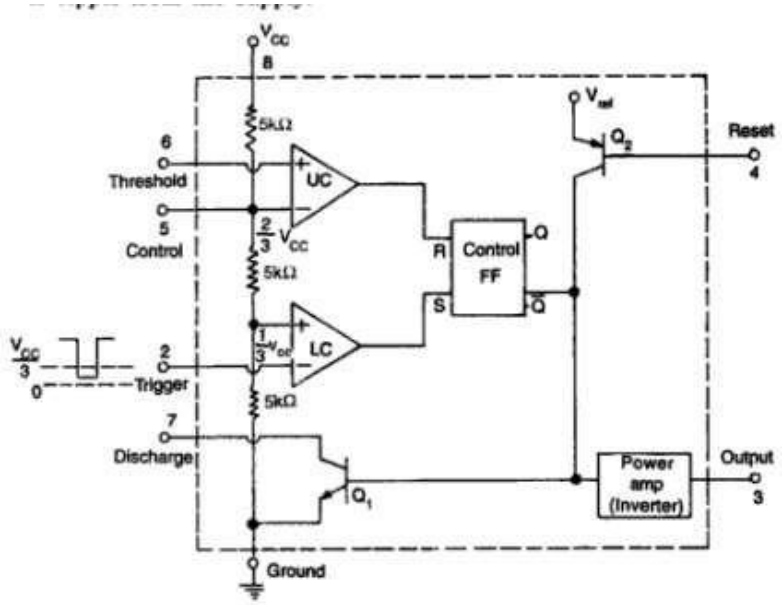


Fig. 8.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of the lower comparator (i.e. $V_{cc}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{cc}/3$), the output of the lower comparator goes HIGH and sets the FF (Q = 1, $\overline{Q}$ = 0). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{cc}, the output of the upper comparator goes HIGH and resets the FF (Q = 0, $\overline{Q}$ = 1).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{cc}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

5. a) With a block diagram explain the operation of PLL. (Nov 2015)

b) Describe the working of PLL using neat block diagram and explain any one application of the same. (April/May 2018)

c) Explain the working of PLL using appropriate block diagram and explain any one application of same. (May 2019, Sept 2020)

The basic block schematic of the PLL is shown in Fig. 9.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency f_0 called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_0 of the VCO. If the two signals differ in frequency

and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_0)$ and difference $(f_s - f_0)$ components at its output. The high frequency component $(f_s + f_0)$ is removed by the low pass filter and the difference frequency

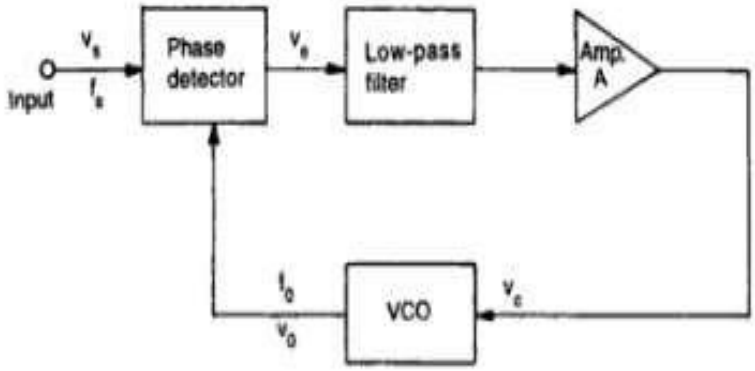


Fig. 9.1 Block schematic of the PLL

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which

the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_0, the VCO frequency.

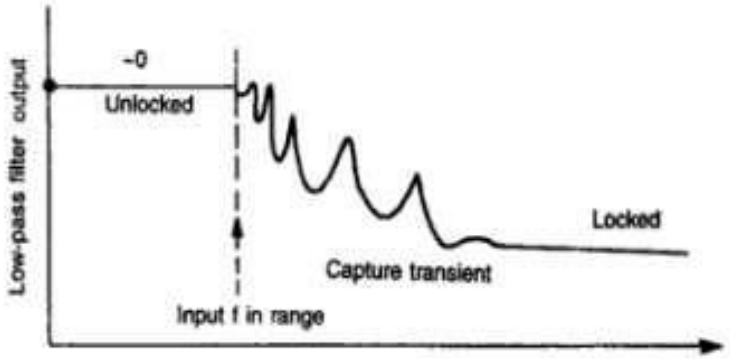


Fig. 9.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

6. Explain the principle and operation of digital phase detector LPF available in PLL. (Nov 2016)

Figure 9.5(a) shows the digital type XOR (Exclusive-OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_0 is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_0$ are shown in Fig. 9.5(b). In this figure, f_s is leading f_0 by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in Fig. 9.5(c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ration K_ϕ for a supply voltage $V_{cc} = 5V$ is,

$$K_\phi = \frac{5}{\pi} = 1.59\ V/\text{rad} \qquad (9.7)$$

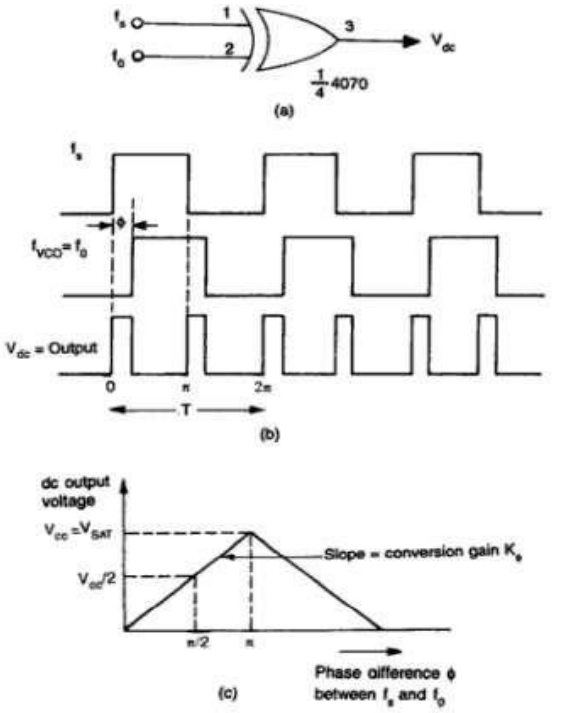


Fig. 9.5 (a) Exclusive-OR phase detector (b) Input and output waveforms (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an edge-triggered phase detector as shown in Fig. 9.6(a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_0 (VCO output) are both pulse waveforms with duty cycle less than 50 percent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_0 as shown in Fig. 9.6(b). The variation of dc output voltage vs phase difference between f_s and f_0 is shown in Fig. 9.6(c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

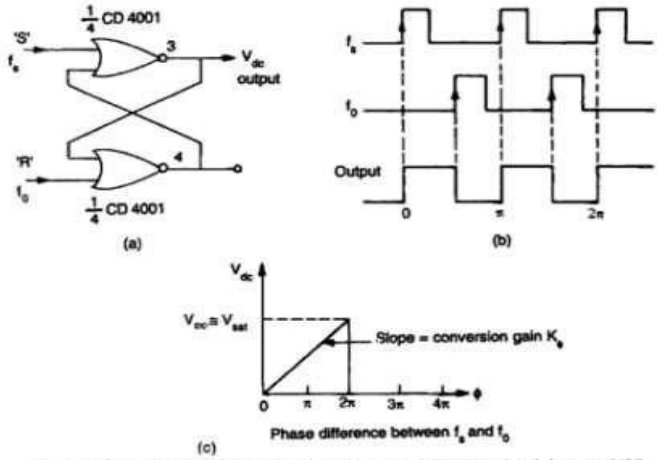


Fig. 9.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate (b) Input and output waveforms (c) dc output voltage vs phase difference ϕ

7. Explain any 2 applications of PLL. (May 2017)

AM MODULATOR

The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

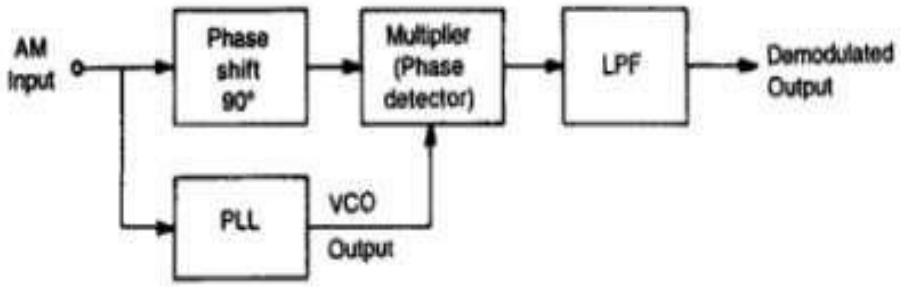


Fig. 9.14 PLL used as AM demodulator

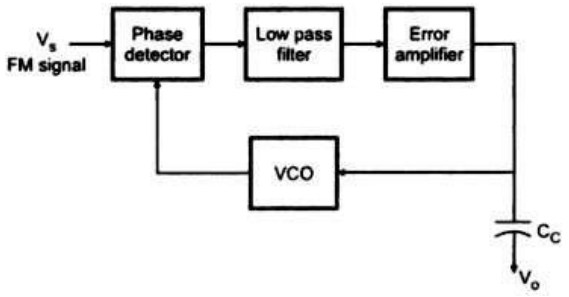
FSK Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 9.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

FM Demodulation

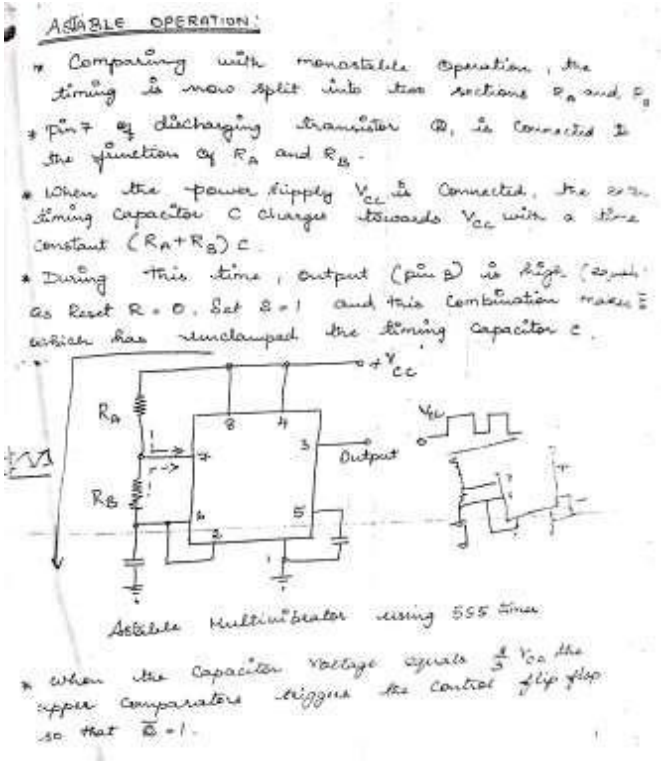
The PLL can be very easily used as an FM detector or demodulator. When the PLL is locked in on the FM signal the VCO frequency follows the instantaneous frequency of the FM signal and the error voltage or VCO control voltage is proportional to the deviation of the input

frequency from center frequency. Therefore the ac component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage that is applied to the FM carrier at the transmitter. The faithful reproduction of modulating voltage depends on the linearity will represent a true replica of the modulating voltage depends on the linearity between the instantaneous frequency deviation and the control voltage of VCO. It is also important to note that the FM frequency deviation and modulating frequency should remain in the locking range of PLL to get the faithful replica of the modulating signal. If the product of the modulation frequency fm and the frequency deviation exceeds the $(\Delta f_C)2$, the VCO will not be able to follow the instantaneous frequency of the FM signal.



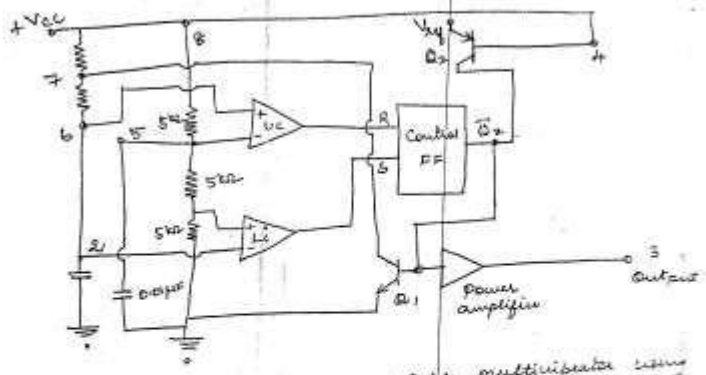
8. a) Explain the operation of 555 timer in astable mode with neat circuit and waveforms. Derive the expression for frequency of output voltage in it. (May 2018)

b) With the circuit diagram and functional block diagram of astable multivibrator using 555 timer, explain its operation. Also develop an equation for Frequency of square wave output. (Nov 2018)



(16)

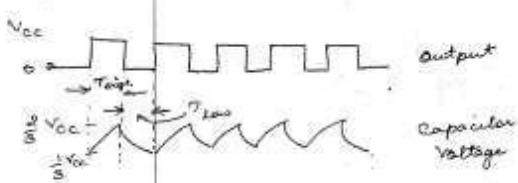
* This is the time makes transistor Q_1 on and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant $R_B C$.



Functional diagram of astable multivibrator using 555 timer

* Current also flows into transistor Q_1 through R_A. Resistor R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1.
* The minimum value of R_A is approximately equal to $V_{cc}/0.2$ where 0.2 A is the maximum current through the on transistor Q_1.

* During the discharge of the timing capacitor as it reaches $\frac{V_{cc}}{3}$, the lower comparator triggered. at this stage $S=1$, $R=0$ which turns $\bar{Q}=0$.
* Now $\bar{Q}=0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between $(\frac{2}{3})V_{cc}$ and $(\frac{1}{3})V_{cc}$.



* The length of time that the output remains HIGH is the time for the capacitor to charge from $(\frac{1}{3})V_{cc}$ to $(\frac{2}{3})V_{cc}$.
* The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$V_c = V_{cc}(1 - e^{-t/Rc})$$

The time t_1 taken by the circuit to charge from 0 to $(\frac{2}{3})V_{cc}$ is:

$$(\frac{2}{3})V_{cc} = V_{cc}(1 - e^{-t_1/Rc}) \quad \text{——} (1)$$

or $t_1 = 1.09\,Rc$

and the time t_2 to charge from 0 to $(\frac{1}{3})V_{cc}$, is

$$(\frac{1}{3})V_{cc} = V_{cc}(1 - e^{-t_2/Rc}) \quad \text{——} (2)$$

(a) $t_2 = 0.405\ RC$

So the time t_2 to charge from $(\frac{1}{3})V_{cc}$ to $(\frac{2}{3})V_{cc}$

is $t_{HIGH} = t_1 - t_2$

$t_{HIGH} = 1.09\ RC - 0.405\ RC = 0.69\ RC$

So, for the given circuit,

$t_{HIGH} = 0.69\ (R_A + R_B)C$ ——— (3)

* The output is low while the capacitor discharges from $(\frac{2}{3})V_{cc}$ to $(\frac{1}{3})V_{cc}$ and the voltage across the capacitor is given by

$$(\frac{1}{3})V_{cc} = (\frac{2}{3})V_{cc}\ e^{-t/RC}$$

Solving, we get $t = 0.69 \cdot RC$

So, for the given circuit, $t_{LOW} = 0.69\ R_B C$ ———

Notice that both R_A and R_B are in the charge path but only R_B is in the discharge path.

Therefore, total time

$T = t_{HIGH} + t_{LOW}$

or $T = 0.69\ (R_A + 2R_B)C$ ----------

So, $f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$ ——— (5)

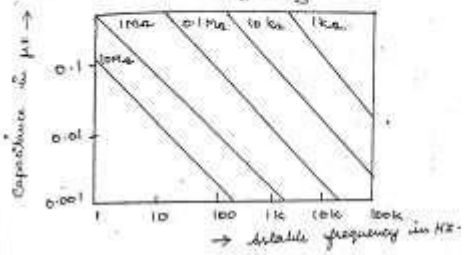
* The graph shows the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given output frequency.
* The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$.

(17)

* In this circuit, when the transistor Q_1 is ON, the output goes low. Hence

$$D\% = \frac{t_{LOW}}{T} \times 100$$

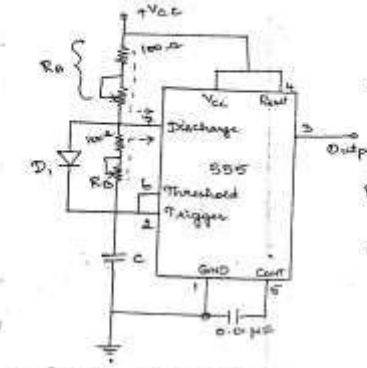
$$= \frac{R_B}{R_A + 2R_B} \times 100$$



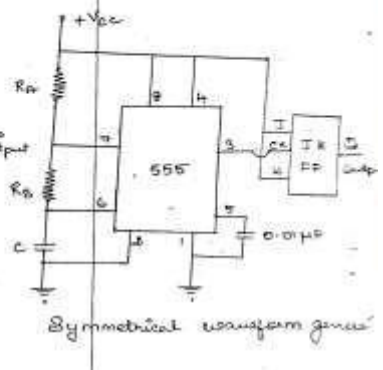
* With a circuit configuration, it is not possible to have a duty cycle more than 50%, since t_{HIGH} will always be greater than $t_{LOW} = 0.69\ R_B C$.
* In order a symmetrical squarewave (i.e) D = 50%, the resistance R_A must be reduced to zero.
* However, now pin 7 is connected directly to V_{cc} and extra current will flow through Q_1 when it is switched ON.
* This may damage Q_1 and hence the timer.
* An alternative circuit which will allow duty cycle to be set at practically any level is shown.
* During the charging portion of the cycle, ~~the~~ diode D_1 is forward biased

(a) effectively short circuiting R_B so that

$t_{HIGH} = 0.69 R_A C$



Adjustable duty cycle Rectangular wave generator



Symmetrical waveform gene

* However, during the discharging portion of the cycle, transistor Q_1 becomes ON thereby grounding pin 7 and hence the diode D_1 is reverse biased

So $t_{LOW} = 0.69 R_B C$ — (6)

$T = t_{HIGH} + t_{LOW} = 0.69 (R_A + R_B) C$ — (7)

or $f = \frac{1.45}{(R_A + R_B) C}$ — (8)

and duty cycle $D = \frac{R_B}{R_A + R_B}$

* Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width.
* However, a series resistor of atleast 100Ω should be added to each R_A and R_B.
* This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value.
* And if R_A is made equal to R_B, then 50% duty cycle is achieved.
* Symmetrical square wave generated by adding a clocked JK flip-flop to the output of the asymmetrical square wave generator is shown.
* The clocked flip-flop acts as a binary divider to the timer output.
* The output frequency in this case will be one half that of the timer.
* The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

9. Derive the expression for lock-in-range and capture range of LM565 PLL. (Nov 2018)

$$v_c = AK_\phi(\phi - \pi/2) \quad (9.19)$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_o + K_v v_c \quad (9.20)$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \quad (9.21)$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \quad (9.22)$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \quad (9.23)$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 9.4(c) and v_c (max) $= \pm K_\phi \pi/2$ from Eq. (9.6). The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2) K_\phi A \quad (9.24)$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A (\pi/2) \quad (9.25)$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max} = f_o \pm K_v K_\phi (\pi/2) A = f_o \pm \Delta f_L \quad (9.26)$$

where $2\Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2\Delta f_L = K_v K_\phi A \pi \quad (9.27)$$

or, $$\Delta f_L = \pm K_v K_\phi A (\pi/2) \quad (9.28)$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. (9.15))}$$

where $$V = +V_{cc} - (-V_{cc})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. (9.17))}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. (9.28) becomes,

$$\Delta f_L = \pm 7.8 f_o/V \quad (9.29)$$

Derivation of Capture Range

When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \quad (9.30)$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \quad (9.31)$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta_c$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \quad (9.32)$$

where $f_1 = 1/2\pi RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) = \frac{f_1}{jf} \quad (9.33)$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) = f_1/\Delta f = f_1/(f_s - f_o) \quad (9.34)$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \quad (9.35)$$

or, $$v_{c(max)} = v_{e(max)} \times T(f) \times A$$

$$= \pm K_\phi (\pi/2) A (f_1/\Delta f). \text{ (from Eq. (9.24))} \quad (9.36)$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v v_{c(max)} = \pm K_v K_\phi (\pi/2) A (f_1/\Delta f) \quad (9.37)$$

For the acquisition of signal frequency, we should put $f = f_s$ so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi (\pi/2) A (f_1/\Delta f_c) \quad (9.38)$$

Now $$\Delta f_c = (f_s - f_o)_{max}$$

so, $$(\Delta f_c)^2 = K_v K_\phi (\pi/2) A f_1 \text{ (from Eq. (9.38))}$$

10. List the important features of the 555 timer. Also write about the two basic modes in which the 555 timer operates. (May 2019, Sept 2020)

Some important features of the 555 timer:

- It operates from a wide range of power ranging from +5 Volts to +18 Volts supply voltage.
- Sinking or sourcing 200 mA of load current.
- The external components should be selected properly so that the timing intervals can be made into several minutes along with the frequencies exceeding several hundred kilohertz.
- The output of a 555 timer can drive a transistor-transistor logic (TTL) due to its high current output.
- It has a temperature stability of 50 parts per million (ppm) per degree Celsius change in temperature which is equivalent to 0.005 %/ °C.
- The duty cycle of the timer is adjustable.
- Also, the maximum power dissipation per package is 600 mW and its trigger and reset inputs has logic compatibility.

Astable Mode:

In this mode, there will be no stable level at the output and the output will keep swinging between high and low. i.e.- It doesn't have any stable state and keeps switching between high and low without application of any external trigger.

Working of 555 timer in A-stable mode:

The trigger and threshold pin are connected together so, there is no need of external trigger pulse. The comparator will output 1 while charging the trigger because the input voltage at trigger pin is still lower than 1/3 of supplied voltage. This time, the output of timer is high. Once the voltage across reaches 1/3 of the supplied voltage, the trigger comparator will output 0,keeping the situation unchanged as both R and S input of flip flop are 0.Once the voltage across the capacitor reaches 3/7 of applied voltage, the threshold comparator will output 1 to R input of the flip-flop. Now, the capacitor will start discharging through resistor R_2 and discharging transistor. The output of 555 Timer is low at this point. Once the voltage across capacitor drops to 1/3 of the supplied voltage, the trigger comparator will output 1.

High Time:

$T_H = 0.693 \text{ x } (R_1 \text{ x } R_2) \text{ X} C_1$

Low Time:

$T_L = 0.693 \text{ x } (R_2) \text{ X } (C_1)$

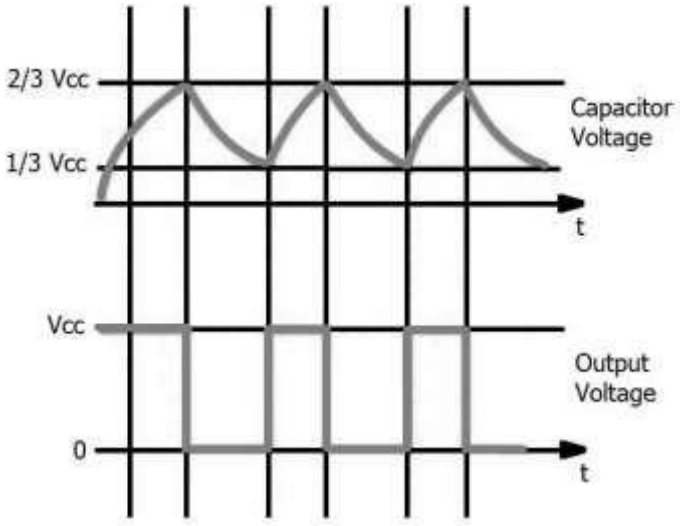
Period for one cycle:

$T = TH + TL \times (R_1 + 2R_2) C1$

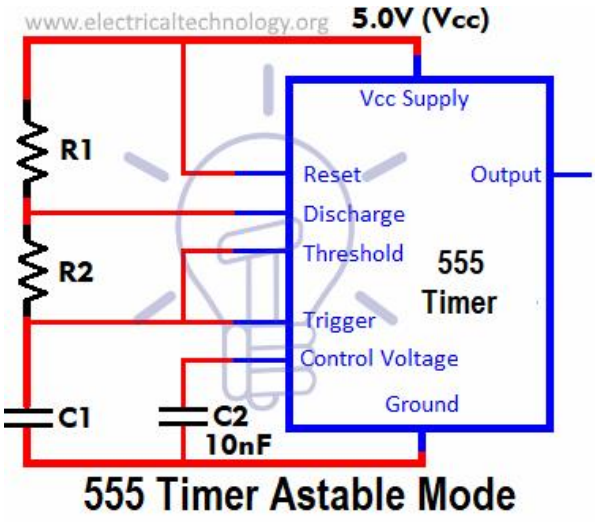
Frequency:

$f = 1.44 / (R_1 + R_2) C_1) HZ$

It is also known as self-triggering mode, the Timer is used in this mode as **clock pulse generator** or **oscillator**. The Timer switches between two quasi stable states and without any external trigger input.



Given below is 555 Timer circuit in Astable mode.



As the Timer is switched ON, i.e. the output is HIGH, the transistor Q_2 will be in cut off region on receiving a LOW input signal. The capacitor charges through both the resistors R_1 and R_2 toward Vcc. The capacitor charging time being

$$\tau_1 = 0.693\ (R_1 + R_2)*C.$$

This capacitor voltage is the threshold voltage to the upper comparator.

As the voltage exceeds **2/3 Vcc**, the upper comparator output resets the Flip-Flop, which turns the Timer output to OFF state (provided reset pin is in LOW state) The transistor τ will in saturation region, i.e. will be turned ON, providing a discharge path for the capacitor through resistor R_2, the discharge time being $-0.693\ R_2*C$.

As the capacitor voltage falls below **-1/3Vcc**, the second comparator output sets the Flip-Flop, which makes the Timer output LOW and the whole process starts again. Thus the Timer output oscillates between HIGH and LOW state, generating oscillations.

***Monostable Mode**:*

This configuration consists of one stable and unstable state. If the stable output is set at high then the output of timer is high.

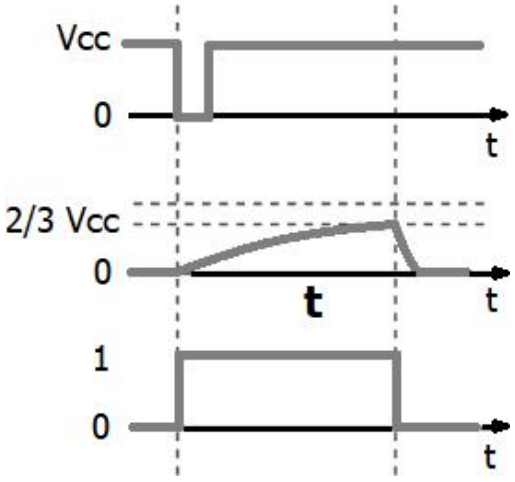
Working Of 555 Timer In Mono-Stable Mode

The trigger input is held high by connecting it to VCC through resistor. Threshold pin is low making the threshold comparator out 0. IN result, voltage coming from source is going to ground through the transistor. Press the pushbutton on trigger to change the 555 timer output to high. At the same time, capacitor C_1 will start charging through resistor R_1. The 555 timer will remain in this position until the voltage across capacitor reaches 2/3 of the supplied voltage. Comparator will output 1 to R input of the flip flop bringing the circuit into initial state. The amount of time the timer output will remain high; depend entirely on value of both the capacitor C_1 and resistor R_1.

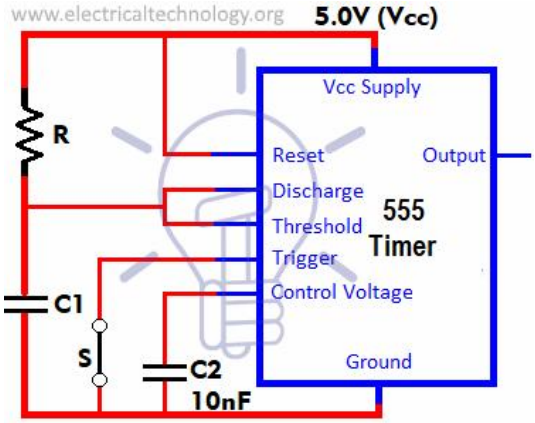
To calculate the time, use the below formula:

$T = 1.1 * C_1 * R_1$

It is also known as single shot mode or pulse generating mode. In this state, the 555 Timer is normally in a stable state until triggered, after which it jumps to the quasi stable state.



Given below is 555 Timer circuit in a monostable mode.



555 Timer in Monostable Mode

Initially the Timer output is LOW and the transistor Q_2 is in saturation mode, i.e. Fully ON. As a negative trigger pulse, more negative than -1/3 Vcc, is applied to the second comparator, the Flip Flop sets to HIGH, turning the Timer output to HIGH state and the Transistor τ is turned OFF.

The output remains HIGH for time Tout i.e τ = 1.1 RC, i.e. the time taken for Capacitor C to charge (Also known as Time Constant RC). As Capacitor voltage exceeds 2/3 Vcc, output from the upper comparator resets the Flip-Flop to zero and the discharge transistor Q_2 gets again saturated, providing a discharge path to the capacitor. As the capacitor voltage comes back to zero volts, the circuit comes back to its normal state.

BM T45 – LINEAR INTEGRATED CIRCUITS

UNIT-V

2 MARKS

1. List various techniques of ADC. (May 2014)

An ADC converts a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal. The conversion involves quantization of the input, so it necessarily introduces a small amount of error or noise.

Types of ADC: 1. Flash (comparator) type converter 2. Counter type converter 3. Tracking or servo converter 4. Successive approximation type converter

2. What are the applications of PLL. (May 2014)

- In radio transmitters, a **PLL** is used to synthesize new frequencies which are a multiple of a reference frequency, with the same stability as the reference frequency.
- Demodulation of frequency modulation (FM): If **PLL** is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal.

3. What is absolute accuracy? (Nov 2014)

- **Absolute accuracy** is the closeness of an estimated, measured, or computed value to a standard, accepted, or true value of a particular quantity.
- In mapping, a statement of **absolute accuracy** is made with respect to a datum, which is, in fact, also an adjustment of many measurements and has some inherent error.

4. Give the mathematical expression for D/A converter. (Nov 2014, May 2018)

Mathematically it is described as
Vo =KVFS(d12-1+d22-2+….dn2-n) where, K -scaling factor, VFS-full scale output voltage.

5. What are the advantages and disadvantages of R-2R ladder DAC? (Nov 2015)

Advantages:

- Easier to build accurately as only two precision metal film resistors are required.
- Number of bits can be expanded by adding more sections of same **R/2R** values.

- In inverted **R/2R ladder DAC**, node voltages remain constant with changing input binary words.

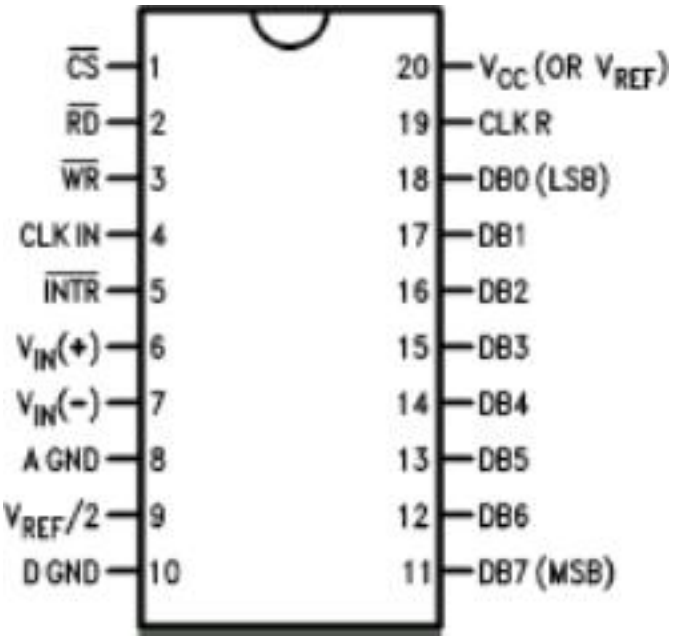
Disadvantages:

- This type requires large range of resistors with necessary high precision for low resistors.
- Requires low switch resistances in transistors.

6. What is meant by resolution of an ADC? (Nov 2015, May 2018)

- The resolution of the ADC is the number of bits it uses to digitize the input samples.
- For an n bit ADC the number of discrete digital levels that can be produced is 2n.
- Thus, a 12 bit digitizer can resolve 212 or 4096 levels.

7. Draw the pin diagram of ADC 0804. (Nov 2016)



8. Give any two specifications for a D/A converter. (Nov 2016)

Digital to Analog Converter (DAC) Specifications:

- D/A converters are available with wide range of specifications specified by manufacturer.
- Some of the important specifications are Resolution, Accuracy, linearity, monotonicity, conversion time, settling time and stability.

9. Define the terms settling time and conversion time related to DAC's. (May 2017, May 2019)

- DAC settling time is the elapsed time from input code application until the output arrives at and remains within a specified error band around the final value.
- It is usually specified for a full-scale 10V transition.

10. How many resistors are required in a 12-bit weighted resistor DAC? (May 2017)

- As the number of bit increases, the range of resistance value increases.
- The largest resistor value for 12-bit DAC= $2^n \times R = 2^{12} \times 2.5k\Omega = 4096 \times 2.5k\Omega = 10.24M\Omega$.

11. Mathematically express the D/A converter, for the output voltage. (Nov 2017)

The input is an n-bit binary word D and is combined with the reference voltage VR to give on analog output signal. Mathematically it is described as
Vo =KVFS(d12-1+d22-2+….dn2-n) where, K -scaling factor, VFS-full scale output voltage.

12. Write about linearity error of a converter. (Nov 2017)

- Linearity error is the maximum deviation in step size from the ideal step size. Some D/A converters are having a linearity error as low as 0.001% of full scale.
- The linearity of a D/A converter is defined as the precision or exactness with which the digital input is converted into analog output.

13. State the principle of single slope A/D converter. (May 2019)

- A single-slope ADC, particularly suitable for use in a massive-parallel ADC architecture in a readout circuit of a CMOS imager. A plurality of ramp signals are generated which define non-overlapping sub-ranges of the full input range.
- For each ADC channel, the sub-range in which the voltage of the input signal falls is determined, and the corresponding ramp signal is selected for use in the A/D conversion.
- Thus, the speed of the A/D conversion process can be increased and the power consumption decreased.

14. What is the drawback in a weighted resistor DAC? (Sept 2020)

- The input current is proportional to the binary weights and the output voltage is proportional to the sum of the binary weights.
- This is because the sum of all the input current is through Rf.
- The disadvantage of the weighted resistor DAC is the numerous resistor values.

15. Give the conversion time for

a) Counting ADC

The **conversion time** can be as (2n−1) clock periods depending upon the magnitude of input voltage VI. For instance, a 12-bit system with 1MHz clock frequency, the counter will take (212−1)μs= 4.095ms to convert a full scale input.

b) Successive approximation ADC

The device that makes **conversions** of analog signals to a digital form is the analog-to-digital converter (**ADC**). Every **ADC** requires a certain amount of **time** to perform the A/D **conversion**. A typical **ADC** device is characterized by a maximum **conversion time** of 40 μs.

c) Dual slope ADC

Dual-slope converter. As an example, to obtain 10-bit resolution, you would integrate for 1024 (2^{10}) clock cycles, then deintegrate for up to 1024 clock cycles (giving a maximum **conversion** of 2×2^{10} cycles). For more resolution, increase the number of clock cycles.

16. The basic step of a 9-bit digital to analog converter is 10.3v. If 000000000 represents 0v. What is the output voltage produced if the digital input is 101101111? (Nov 2018)

The output voltage for input of 101101111 is

= 10.3 V (1*28+0*27+1*26+1*25+0*24+1*23+1*22+1*21+1*20)

= 10.3 * 10-3 * 367 = 3.78 V

17. List out the various classification of analog to digital converters. Among them which is the fastest one. (Nov 2018)

- The most common types of ADCs are flash, successive approximation, and sigma-delta.
- The flash ADC is the fastest type available.
- A flash ADC uses comparators, one per voltage step, and a string of resistors.

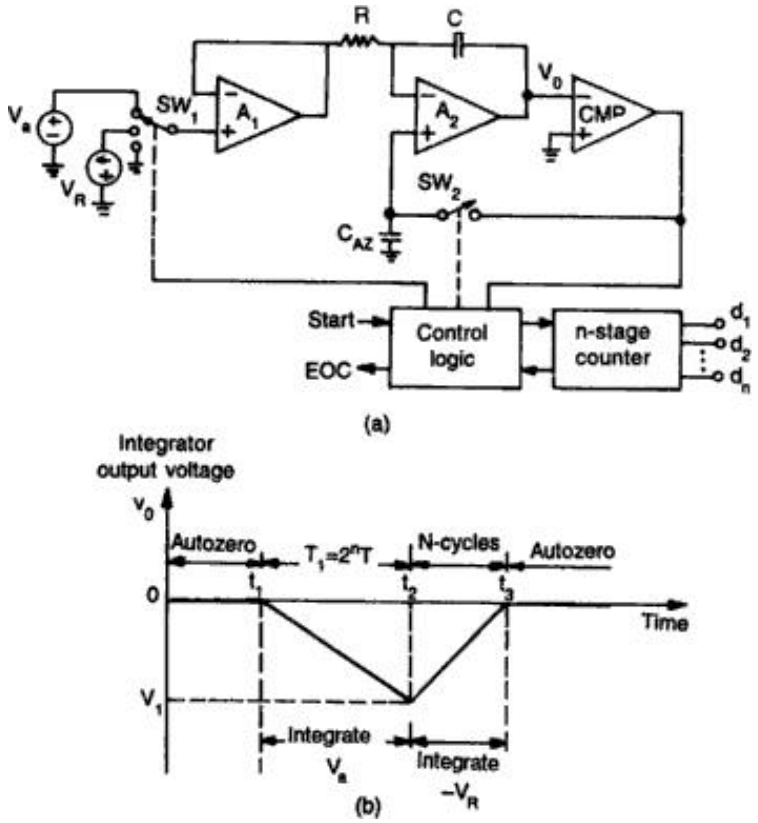
11 MARKS

1.How analog to digital conversion takes place using dual slope technique? (May 2014, Nov 2014)

A **dual slope ADC** produces an equivalent digital output for a corresponding analog input by using two (dual) slope technique.

Figure (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A_1, precision integrator A_2 and a voltage comparator.

The converted first integrates the analog input signal V_a for a fixed duration of 2^n clock periods as shown in figure (b).Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional too the value of Va averaged over the integration period. Hence N represents the desired output code.



a) Functional diagram of the dual slope ADC b)Integrated output waveform for the dual slope ADC

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}}$$

$$t_3 - t_2 = \frac{\text{digital count } N}{\text{clock rate}}$$

For an integrator,

$$\Delta v_o = (-1/RC)\ V(\Delta t)$$

The voltage v_0 will be equal to v_1 at the instant t_2 and can be written as

$$v_1 = (-1/RC)\ V_a(t_2 - t_1)$$

The voltage v_1 is also given by,

$$v_1 = (-1/RC)\ (-V_R)\ (t_2 - t_3)$$
$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get

$$V_a(2^n) = (V_R)N$$
$$V_a = (V_R)\ (N/2^n)$$

The dual slope ADC mainly consists of 5 blocks: Integrator, Comparator, Clock signal generator, Control logic and Counter.

The **working** of a dual slope ADC is as follows −

The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it is received the start commanding signal.

Control logic pushes the switch **sw** to connect to the **external analog input voltage** Vi, when it is received the start commanding signal. This input voltage is applied to an integrator.

The output of the **integrator** is connected to one of the two inputs of the comparator and the other input of comparator is connected to ground.

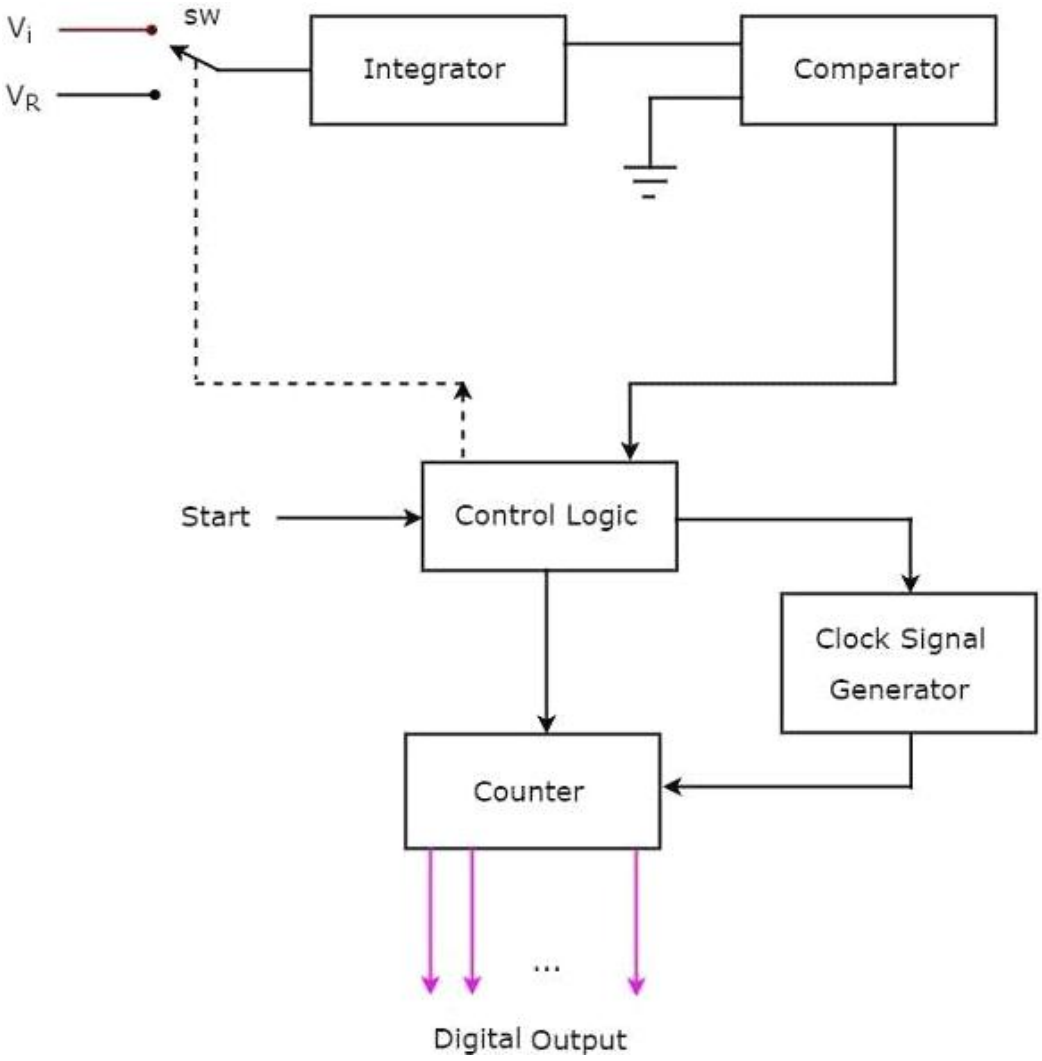
Comparator compares the output of the integrator with zero volts (ground) and produces an output, which is applied to the control logic.

The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. It produces an overflow signal to the control logic, when it is incremented after reaching the maximum count value. At this instant, all the bits of counter will be having zeros only.

Now, the control logic pushes the switch **sw** to connect to the **negative reference** voltage −Vref. This negative reference voltage is applied to an integrator. It removes the charge stored in the capacitor until it becomes zero.

At this instant, both the inputs of a comparator are having zero volts. So, comparator sends a signal to the control logic. Now, the control logic disables the clock signal generator and retains (holds) the counter value. The **counter value** is proportional to the external analog input voltage.

Block diagram:

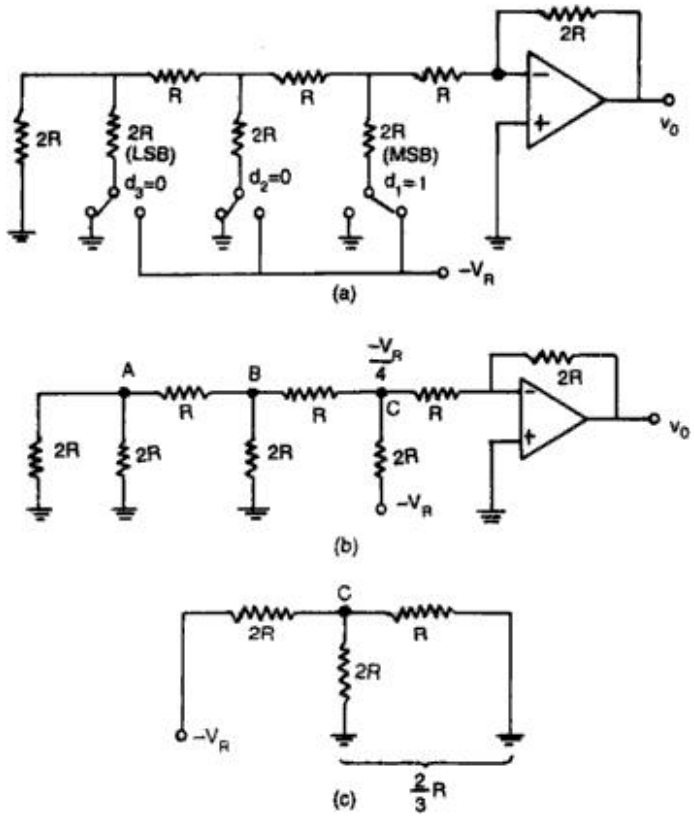


At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi.

The dual slope ADC is used in the applications, where **accuracy** is more important while converting analog input into its equivalent digital (binary) data.

2. What is the working of R-2R ladder network digital to analog conversion? (May 2014, Nov 2014, Nov 2016, May 2017, May 2019, Sept 2020)

The R-2R Ladder DAC overcomes the disadvantages of a binary weighted resistor DAC. As the name suggests, R-2R Ladder DAC produces an analog output, which is almost equal to the digital (binary) input by using a **R-2R ladder network** in the inverting adder circuit.



The digital switches shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in above figure will be connected to the negative reference voltage, −VR−VR when the corresponding input bits are equal to '1'.

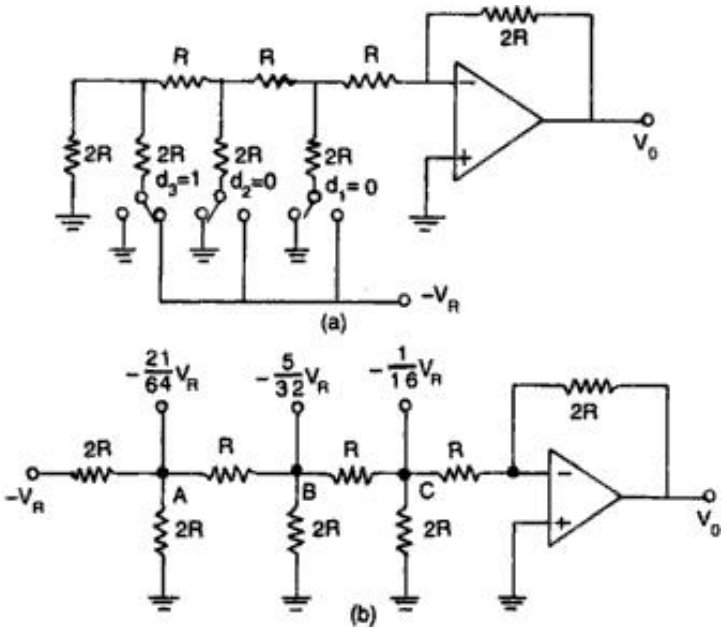
It is difficult to get the generalized output voltage equation of a R-2R Ladder DAC. But, we can find the analog output voltage values of R-2R Ladder DAC for individual binary input combinations easily.

The **advantages** of a R-2R Ladder DAC are as follows −

R-2R Ladder DAC contains only two values of resistor: R and 2R. So, it is easy to select and design more accurate resistors.

If more number of bits are present in the digital input, then we have to include required number of R-2R sections additionally.

Due to the above advantages, R-2R Ladder DAC is preferable over binary weighted resistor DAC.



Now, the above circuit diagram looks like an **inverting amplifier**. It is having an input voltage of −VR2−VR2 volts, input resistance of 2RΩ2RΩ and feedback resistance of 2RΩ2RΩ.

The **output voltage** of the circuit shown above will be −

$$V0=-2R/2R(-VR/2)$$

$$V0=VR/2$$

Therefore, the **output voltage** of 3-bit R-2R Ladder DAC is VR2VR2 volts

3.Calculate the values of LSB, MSB and full scale output of an 8-bit DAC for the (0-10 V) range. (Nov 2014)

The values of LSB, MSB and full scale output of an 8-bit DAC for the 0-10V range is given below.

$$\text{LSB} = \frac{1}{2^8} = \frac{1}{256}$$

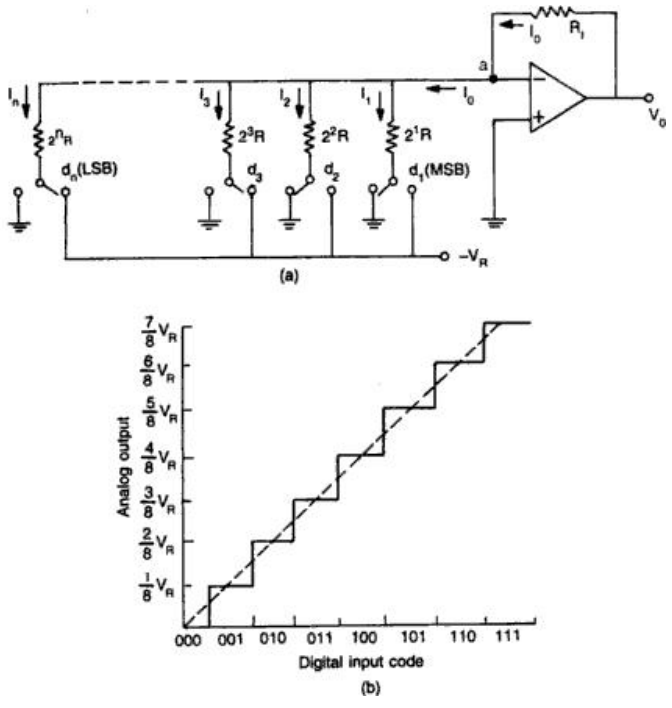
$$\text{For 10 V range,} \qquad \text{LSB} = \frac{10\text{ V}}{256} = 39\text{ mV}$$

$$\text{and} \qquad \text{MSB} = \left(\frac{1}{2}\right) \text{full scale} = 5\text{ V}$$

$$\text{Full scale output} = (\text{Full scale voltage} - 1\text{ LSB})$$
$$= 10\text{ V} - 0.039\text{ V} = 9.961\text{ V}$$

4.Explain 4 bit weighted resistor DAC with a neat diagram. (Nov 2015, Nov 2016, May 2019)

A weighted resistor DAC produces an analog output, which is almost equal to the digital (binary) input by using **binary weighted resistors** in the inverting adder circuit. In short, a binary weighted resistor DAC is called as weighted resistor DAC.



The **digital switches** shown in the above figure will be connected to ground, when the corresponding input bits are equal to '0'. Similarly, the digital switches shown in the above figure will be connected to the negative reference voltage, −VR−VR when the corresponding input bits are equal to '1'.

In the above circuit, the non-inverting input terminal of an op-amp is connected to ground. That means zero volts is applied at the non-inverting input terminal of op-amp.

According to the **virtual short concept**, the voltage at the inverting input terminal of opamp is same as that of the voltage present at its non-inverting input terminal. So, the voltage at the inverting input terminal's node will be zero volts.

$$\frac{0+V_R b_2}{2^0 R}+\frac{0+V_R b_1}{2^1 R}+\frac{0+V_R b_0}{2^2 R}+\frac{0-V_0}{R_f}=0$$

$$=>\frac{V_0}{R_f}=\frac{V_R b_2}{2^0 R}+\frac{V_R b_1}{2^1 R}+\frac{V_R b_0}{2^2 R}$$

$$=>V_0=\frac{V_R R_f}{R}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

Substituting, $R=2R_f$ in above equation.

$$=>V_0=\frac{V_R R_f}{2R_f}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

$$=>V_0=\frac{V_R}{2}\left\{\frac{b_2}{2^0}+\frac{b_1}{2^1}+\frac{b_0}{2^2}\right\}$$

The above equation represents the **output voltage equation** of a 3-bit binary weighted resistor DAC. Since the number of bits are three in the binary (digital) input, we will get seven possible values of output voltage by varying the binary input from 000 to 111 for a fixed reference voltage, VRVR.

We can write the **generalized output voltage equation** of an N-bit binary weighted resistor DAC as shown below based on the output voltage equation of a 3-bit binary weighted resistor DAC.

$$=> V_0 = \frac{V_R}{2}\left\{\frac{b_{N-1}}{2^0} + \frac{b_{N-2}}{2^1} + \ldots + \frac{b_0}{2^{N-1}}\right\}$$

The **disadvantages** of a binary weighted resistor DAC are as follows −

The difference between the resistance values corresponding to LSB & MSB will increase as the number of bits present in the digital input increases.

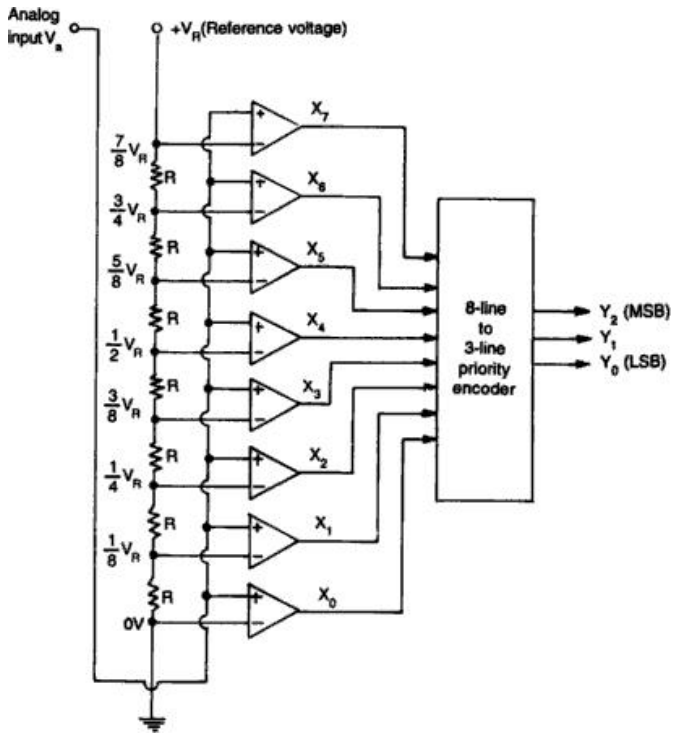
It is difficult to design more accurate resistors as the number of bits present in the digital input increases.

5. Write short notes on flash type A/D converter.(Nov 2016)

A **flash type ADC** produces an equivalent digital output for a corresponding analog input in no time. Hence, flash type ADC is the fastest ADC.The 3-bit flash type ADC consists of a voltage divider network, 7 comparators and a priority encoder.

This is the simplest possible A/D converter.It is at the same time, the fastest and most expensive technique.The circuit consist of a resistive divider network, 8 op-amp comparators and a 8-line to 3-line encoder (3-bit priority encoder).The comparator and its truth table is shown in the figure.

The **working** of a 3-bit flash type ADC is as follows. The **voltage divider network** contains 8 equal resistors. A reference voltage VR is applied across that entire network with respect to the ground. The voltage drop across each resistor from bottom to top with respect to ground will be the integer multiples (from 1 to 8) of VR / 8.

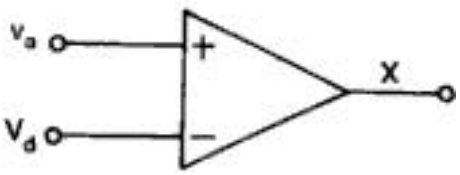


Basic circuit of a flash type A/D converter

The external **input voltage** Vi is applied to the non-inverting terminal of all comparators. The voltage drop across each resistor from bottom to top with respect to ground is applied to the inverting terminal of comparators from bottom to top.

The comparator and its truth table is shown below.

Voltage input	Logic output X
$V_a > V_d$	$X = 1$
$V_a < V_d$	$X = 0$
$V_a = V_d$	Previous value



Comparator and its truth table

The truth table for the flash type A/D converter is shown below.The circuit has the advantage of high speed as the conversion take place simultaneously rather than sequentially.Typical conversion time is 100 ns or less.Conversion time is limited only by the speed of the comparator and of the priority encoder.

Input voltage V_a	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	1	0	0	1
$V_R/4$ to 3 $V_R/8$	0	0	0	0	0	1	1	1	0	1	0
3 $V_R/8$ to $V_R/2$	0	0	0	0	1	1	1	1	0	1	1
$V_R/2$ to 5 $V_R/8$	0	0	0	1	1	1	1	1	1	0	0
5 $V_R/8$ to 3 $V_R/4$	0	0	1	1	1	1	1	1	1	0	1
3 $V_R/4$ to 7 $V_R/8$	0	1	1	1	1	1	1	1	1	1	0
7 $V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Truth table for a flash type A/D converter

At a time, all the comparators compare the external input voltage with the voltage drops present at the respective other input terminal. That means, the comparison operations take place by each comparator **parallelly**.

The **output of the comparator** will be '1' as long as Vi is greater than the voltage drop present at the respective other input terminal. Similarly, the output of comparator will be '0', when, Vi is less than or equal to the voltage drop present at the respective other input terminal.

All the outputs of comparators are connected as the inputs of **priority encoder**.This priority encoder produces a binary code (digital output), which is corresponding to the high priority input that has '1'.

Therefore, the output of priority encoder is nothing but the binary equivalent **(digital output)** of external analog input voltage, Vi.

The flash type ADC is used in the applications where the conversion speed of analog input into digital data should be very high.

The type of ADC has the disadvantage that the number of comparator required almost doubles for each added bit.A 2-bit ADC requires 3 comparators, 3-bit ADC needs 7, whereas 4-bit requires 15 comparators.

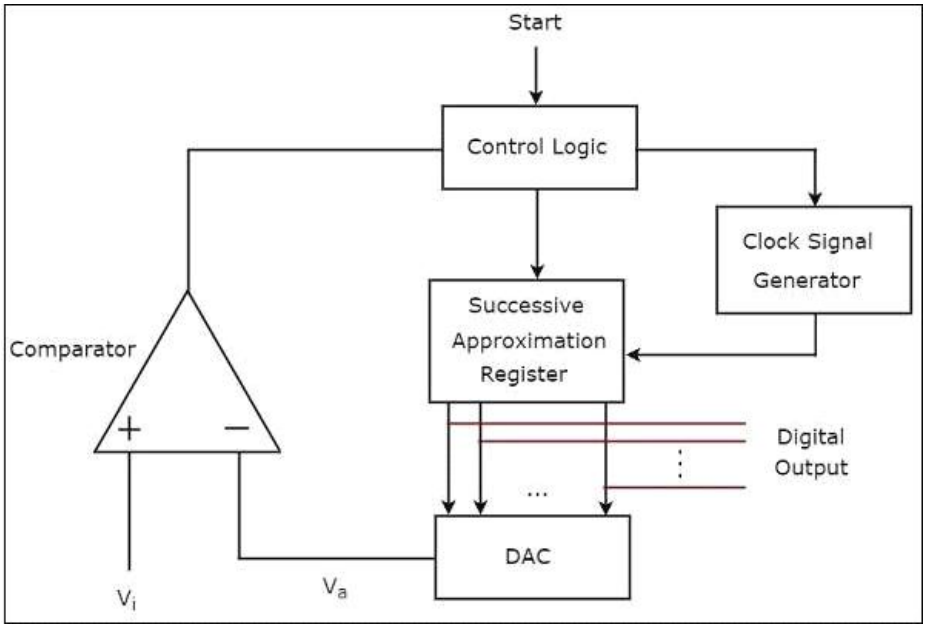
6.Write short notes on successive approximation ADC. (Nov 2016, May 2017, May 2018, Sept 2020)

A **successive approximation type ADC** produces a digital output, which is approximately equal to the analog input by using successive approximation technique internally.

The successive approximation ADC mainly consists of 5 blocks− Clock signal generator, Successive Approximation Register (SAR), DAC, comparator and Control logic.

The **block diagram** of a successive approximation ADC is shown in the following figure

Block diagram:



The **working** of a successive approximation ADC is as follows

The **control logic** resets all the bits of SAR and enables the clock signal generator in order to send the clock pulses to SAR, when it received the start commanding signal.

The binary (digital) data present in **SAR** will be updated for every clock pulse based on the output of comparator. The output of SAR is applied as an input of DAC.

DAC converts the received digital input, which is the output of SAR, into an analog output. The comparator compares this analog value Va with the external analog input value Vi.

The **output of a comparator** will be '1' as long as Vi is greater than Va Similarly, the output of comparator will be '0', when Vi is less than or equal to Va.

The operations mentioned in above steps will be continued until the digital output is a valid one.

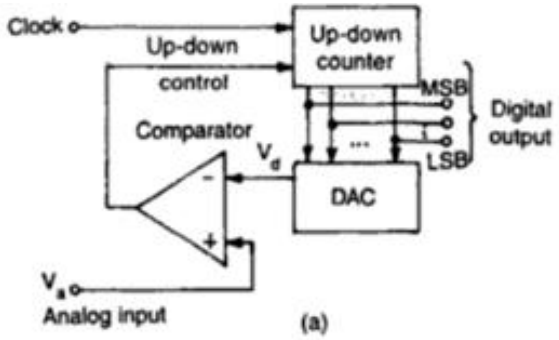
The digital output will be a valid one, when it is almost equivalent to the corresponding external analog input value Vi.

7.Explain in detail about counter type A/D converter.(Nov 2017)

A **counter type ADC** produces a digital output, which is approximately equal to the analog input by using counter operation internally.

The D to A converter can easily be turned around to provide the inverse function A to D conversion. The principle is to adjust the DAC's input code until the DAC's output comes within ± (1/2) LSB to analog input V_a which is to be converted to binary digital form.

A 3-bit counting ADC based upon the above principle s shown in the figure.The counter is reset to zero count by the reset pulse.Upon the release of RESET,the clock pulses are counted by the binary state and this can be taken as the end of conversion (EOC) command.



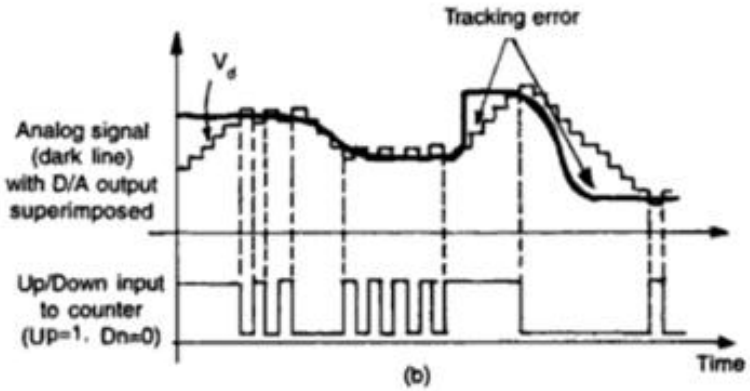


Fig. 10.12(a) A tracking A/D converter (b) Waveforms associated with a tracking A/D converter

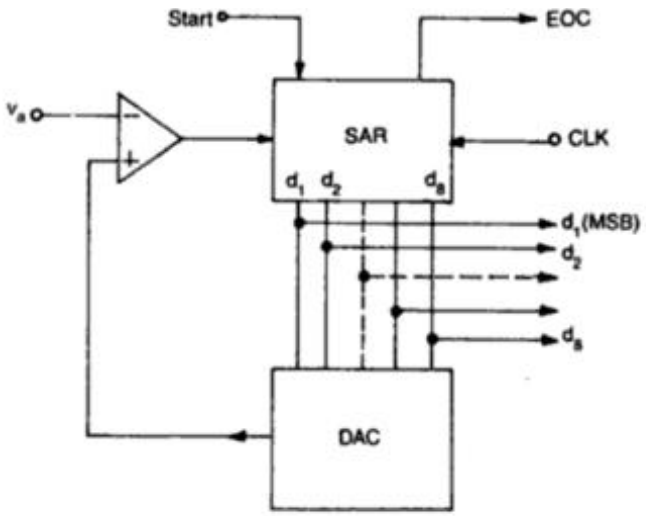
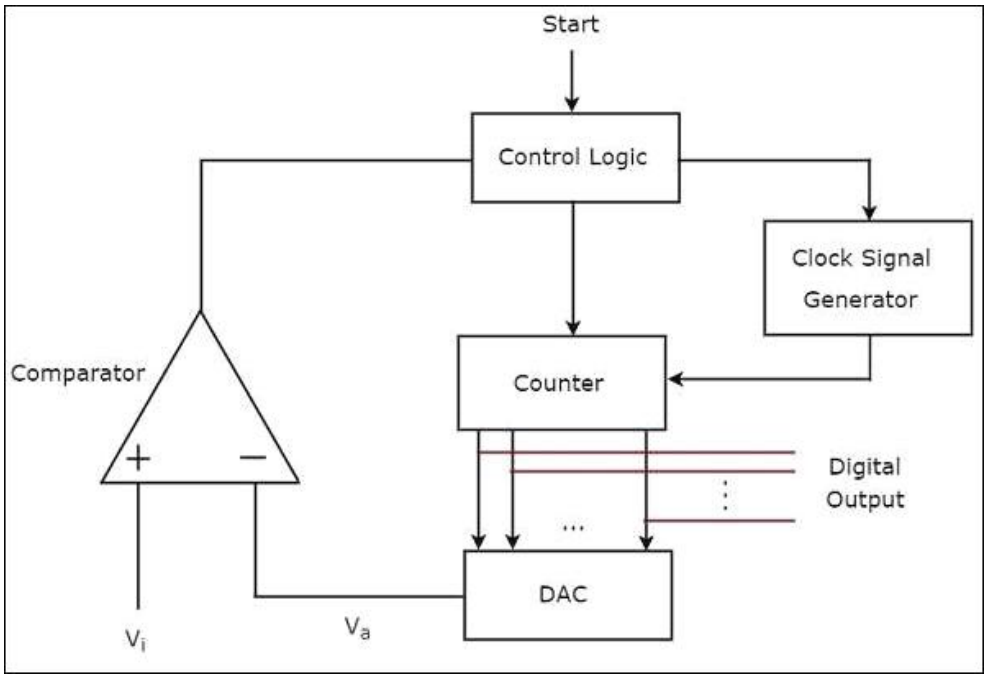


Fig. 10.13 Functional diagram of the successive approximation ADC

Block diagram:



The counter type ADC mainly consists of 5 blocks: Clock signal generator, Counter, DAC, Comparator and Control logic.

The **working** of a counter type ADC is as follows −

The **control logic** resets the counter and enables the clock signal generator in order to send the clock pulses to the counter, when it received the start commanding signal.

The **counter** gets incremented by one for every clock pulse and its value will be in binary (digital) format. This output of the counter is applied as an input of DAC.

DAC converts the received binary (digital) input, which is the output of counter, into an analog output. Comparator compares this analog value,Va with the external analog input value Vi.

The **output of comparator** will be **'1'** as long as □ is greater than. The operations mentioned in above two steps will be continued as long as the control logic receives '1' from the output of comparator.

The **output of comparator** will be **'0'** when Vi is less than or equal to Va. So, the control logic receives '0' from the output of comparator. Then, the control logic disables the clock signal generator so that it does not send any clock pulse to the counter.

At this instant, the output of the counter will be displayed as the **digital output**. It is almost equivalent to the corresponding external analog input value Vi.

8.What output voltage would be produced by a D/A converter whose output voltage range is 0 to 10 V and whose input binary number is

(i) 10 (for a 2 bit DAC) (Nov 2017, May 2018)

(ii) 0110 (for a 2 bit DAC). (Nov 2017, May 2018)

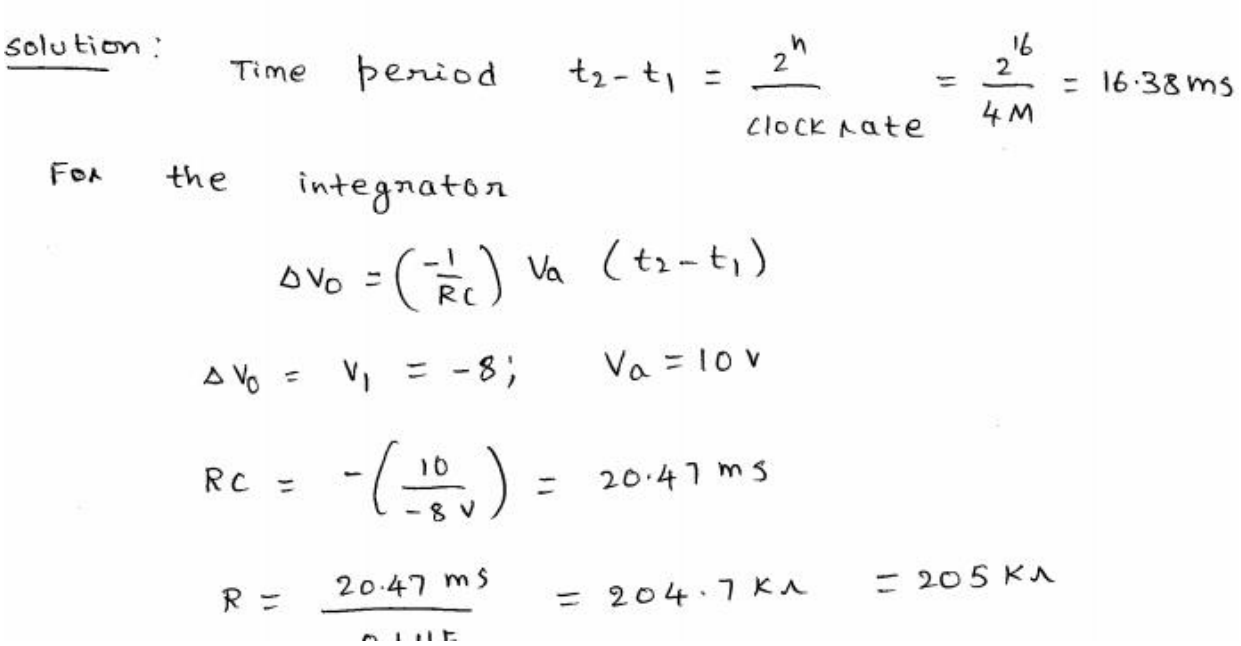
(iii) 10111100 (for a 8-bit DAC) (May 2018)

Solution: i) $V_0 = 10\left(1\times\frac{1}{2} + 0\times\frac{1}{4}\right) = 5\,V$

ii) $V_0 = 10\left(0\times\frac{1}{2} + 1\times\frac{1}{4} + 1\times\frac{1}{8} + 0\times\frac{1}{16}\right) = 3.75\,V$

iii) $V_0 = 10\left(1\times\frac{1}{2} + 0\times\frac{1}{2^2} + 1\times\frac{1}{2^3} + 1\times\frac{1}{2^4} + 1\times\frac{1}{2^5} + 1\times\frac{1}{2^6} + 0\times\frac{1}{2^7} + 0\times\frac{1}{2^8}\right) = 7.34\,V$

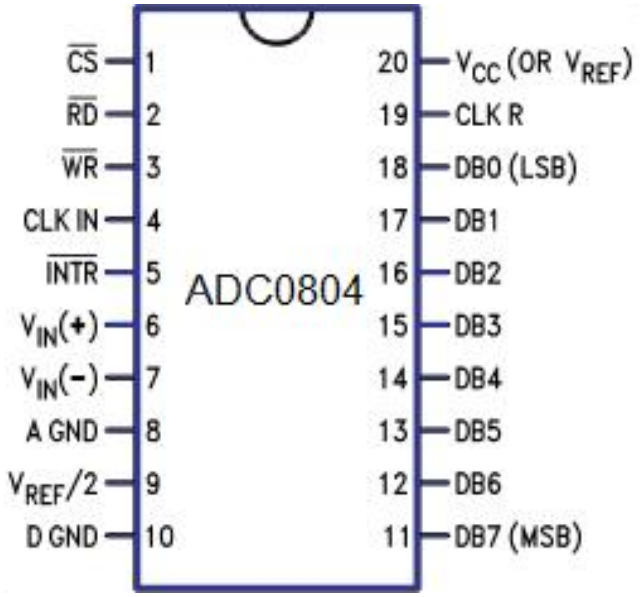
9. a) A dual slope ADC uses 16 bit counter and 4 MHz clock rate.The maximum input voltage is ± 10V.The maximum input voltage integrator output voltage should be -8V when the counter has cycled through 2^n counts.The capacitor used in the integrator is 0.1µF.Find the value of resistor R of the integrator. (May 2019)



b) Briefly discuss about ADC 0804 with block diagram. (May 2019)

ADC0804 is an 8 bit successive approximation analogue to digital converter from National semiconductors. The features of ADC0804 are differential analogue voltage inputs, 0-5V input voltage range, no zero adjustment, built in clock generator, reference voltage can be externally adjusted to convert smaller analogue voltage span to 8 bit resolution etc. The voltage at Vref/2 (pin9) of ADC0804 can be externally adjusted to convert smaller input voltage spans to full 8 bit resolution. Vref/2 (pin9) left open means input voltage span is 0-5V and step size is 5/255=19.6V. Have a look at the table below for different Vref/2 voltages and corresponding analogue input voltage spans.

The pin out diagram of ADC0804 is shown in the figure below.



Steps for converting the analogue input and reading the output from ADC0804.

- Make CS=0 and send a low to high pulse to WR pin to start the conversion.
- Now keep checking the INTR pin. INTR will be 1 if conversion is not finished and INTR will be 0 if conversion is finished.
- If conversion is not finished (INTR=1) , poll until it is finished.
- If conversion is finished (INTR=0), go to the next step.
- Make CS=0 and send a high to low pulse to RD pin to read the data from the ADC.